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A Survey on Dynamic Reconfigurable FIR Filter Design for 5-G Applications

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ABSTRACT— This paper presents a survey on the implementation of new techniques and energy efficient architectures for the fast Reconfigurable FIR filter. The approach is based on the dynamic partial reconfiguration method. The insertion and removal of partial modules and allocation of proper coefficients helps in area efficient and energy efficient Reconfigurable FIR filter implementation. These dynamic reconfigurable FIR filter banks with energy efficiency, wide band width and high speed can be greatly useful for 5-G communication applications.

Index Terms— Reconfigurable FIR Filter, Canonical Signed Digit Coefficient.

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I. INTRODUCTION

The next generations of cellular technology (5-G) needs to be an evolution that requires very high carrier frequencies. High speed data transfers needs to be possible with such networks. There is a requirement for energy efficient, wide band widths, portable and fast filter banks to implement efficient cellular technology. Because filters are key elements of the communication networks. Finite Impulse response filters (FIR Filters) plays crucial role in various signal processing applications in today's communication systems. A several aspects like spectral shaping, filtering, adjustable band width, channel equalization and noise cancellation etc. should be the features of these filters. Therefore, various methods, architectures and implementation strategies have been proposed to enhance the performance of filters in terms of fast, energy efficiency and complexity. The conventional FIR filter designs are less suitable for 5G communication needs. Therefore software reconfiguration filters has paid much attention by the researchers worldwide due to a great demand for reconfigurable communication systems capable of multi standard operations.

The dynamic partial reconfiguration(DPR) [1] method has been employed in reconfiguration FIR filter which enhances the performance in terms of area efficiency and low power allowing flexibility dynamically adding or removing the partial modules. The FIR filter with DPR method can save around 11.5% slice compared to the conventional multiplexer based reconfigurable FIR filter. It is also observed that in symmetric FIR filter one tap change requires slow configuration time. But the DPR based reconfiguration FIR filter requires 1,499 slices for one coefficient tap which increases the flexibility.

The dynamic algorithm transformations (DAT) [2] are used to implement the low power reconfigurable signal processing systems. These DAT's ensures specified level of mean squared error and also minimizes the energy dissipation. The parameters like filter taps, supply voltages, coefficient and data precisions are considered as configurable parameters. The non-stationarities in the will be taken as temporal or spatial transitions between input state space. In this method the taps are powered down starting with smallest value which results in optimal values of precisions and supply voltages.

The FIR filter design using discrete coefficients through sphere relaxation was proposed in [3]. The practice for FIR filter design using every coefficient is a sum of signed power of 2 terms, by sphere relaxation was proposed. This gives a non-convex continues optimization problem where solution can be evaluated considerably much faster and easier than earlier proposed relaxation methods. The coefficient partitioning into sub coefficients, minimax methods for bandwidth adjustment of linear FIR filters have been discussed in [4 - 7].

For wireless system applications channelization and spectrum sensing are achieved with the help of reconfigurable fast filter banks RFFB [8]. The hardware re-implementation increases the circuit complexity as well as increases the power utilization. In RFFB the bandwidth and sub-band centre frequencies can be varied with the high frequency resolution which gives frequency reallocation without hardware re-implementation. The RFFB design uses combination of Fast filter

bank (FFB) and variable digital filter (VDF).The modified frequency transformation which is of second order variable digital filter (MFT-VDF) normally offers wide cut off frequency is employed as FFB in reconfigurable fast filter bank. The RFFB gives fine control on the band width of the sub bands in the overall frequency bandwidth. The rate of activation of the second stage sensing in the RFFB can lower the dynamic power dissipation.

The variable resolution spectrum sensing [9] is achieved with the help of reconfigurable discrete Fourier transform filter bank (DFTFB). The coefficient decimation method is employed for getting the different passband widths. The variable resolution and accurate spectrum sensing is the key issue in cognitive radio and modern wireless systems.

The frequency bandwidth adjustment is also important task in communications. The minimax design technique for adjustable bandwidth linear FIR filter is implemented, where weights of the transfer function is determined directly by the bandwidth. Minimax design techniques can generate globally optimal filters with adjustable bandwidths [10]. This method also proposes how to reduce the complexity of the FIR filter with suitable values of L and N, where L is the order of the filter and N is the number of filter coefficients.

The genetic algorithm based canonical signed digit (CSD) method was introduced in [11] to design FIR filter. The hardware's efficiency can be improved with calculation speed by utilizing the characteristics of the CSD and genetic algorithm.

2. Canonical Signed Digit Based Reconfigurable FIR:

A digit based reconfigurable finite impulse response (FIR) filter architecture with a very fine granularity has been proposed in [12]. In many filters, out of all taps only very few taps uses high precision coefficients. The taps are designed to implement the term $h_i.x[n-i]$, where h_i is the i^{th} coefficient of the filter and x[n-i] is the input sample of the sequence. If all taps uses high precision coefficients that would require more hardware implementation, which leads to many problems like power hungry and silicon space. To overcome hardware complexity, one of the technique is limiting the number of allowable non-zero canonical signed digits (CSD). It causes to limit the coefficient precision there by reduces the frequency response.

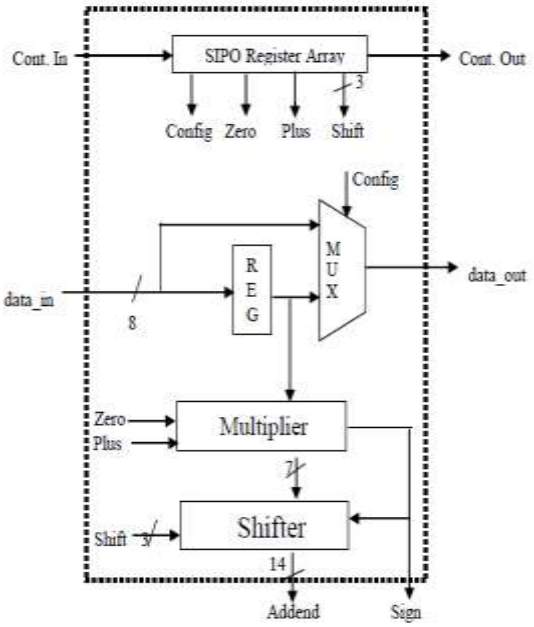

Fig. 1: Block Diagram of Digit Processing Unit (DPU)

The digit processing unit (DPU) can replace the number of taps and non-zero digits in each tap. The DPU consists of SIPO register array where the control signals such as plus, zero and shift are shifted into the register. Config control signal is used to select buffered or unbuffered data through the multiplexer. The multiplier and shifter give two outputs sign and addend corresponding to the partial product. By properly summing up the number of DPU outputs with the help of multiplexer, we can implement the FIR filter with variable number of CSDs in each tap. In the proposed reconfigurable FIR filter eight DPUs are arranged in one pipeline stage. The sign extension generator and one big adder with 9 inputs are also employed in processing element.

The cutoff frequency of the linear phase FIR filters can be varied with less number of parameters [13]. Even there are approaches with one parameter can control the cutoff frequency suggested by Schuessler and Winkelnkemper [14]. The appropriate selection of coefficients would results variable cutoff frequency, transition width etc. The first order transformations can be used to design FIR filter to vary the cutoff frequency with less number of parameters.

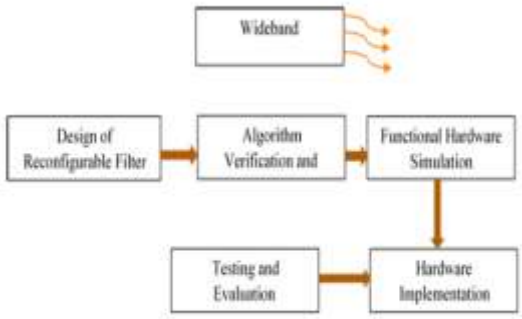

Fig 2: Block Diagram of Reconfigurable Filter Implementation Process

The design of reconfigurable FIR filter can be done using multi tap, modular design architecture and coefficient reallocation without changing the hardware. In modular design initial bitstream is generated first and later partial bitstreams are obtained for each partial reconfigurable modules. Modular designs and multi tap architectures helps the designer to generate bitstream from the HDL coding. Synthesis, simulation, mapping, routing and placement are the various steps need to be carried out to get the final hardware implementation. The dynamic reallocation of coefficients increases the utility of the hardware. The bandwidth selection can be done using proper selection of the coefficients and frequency transformations. The HDL programming can be used to implement the reconfigurable FIR filter with multi tap. Synthesis reports give the hardware utilizations. After implementing the code verification, functional simulation can be done. The timing verification is only preferred after the hardware implementation. The FPGAs are programmable logic devices which allow the implementations of digital designs, and can be used to verify the hardware for its functionality, through put as well as power. The netlist generated from the code has to import on to FPGA, to get the hardware implementation.

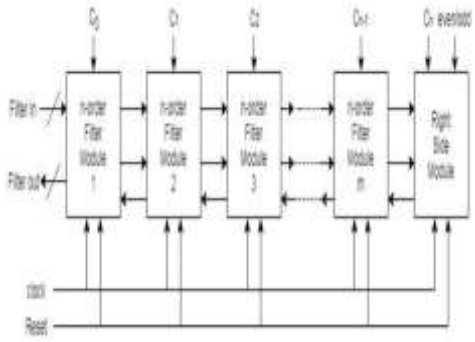

Fig. 3 Block Diagram of Reconfigurable mxn FIR Filter

The Reconfigurable mxn FIR Filter (Fig. 2) consists of n number of n-order filter modules, each module takes filter input and coefficient. There is Reconfigurable Multiply and Accumulate Block in each n-order filter module, which takes care of multiplication of inputs with coefficients and added together at the end. It also includes serial to parallel register to receive coefficient inputs serially. All the blocks are connected with reset signal, to clear all the blocks whenever required. The global clock is used to drive all the blocks simultaneously.

II. IMPLEMENTATION

The Design of an efficient VLSI architecture for an energy efficient Reconfigurable FIR filter bank architecture can be implemented in Verilog HDL or VHDL code and it can be verified through efficient simulation processes. The suitable filter bank circuit for the specified target FPGA can be obtained from the synthesis process after successful completion of the simulation process. The FPGA implementation of digital reconfigurable systems and architectures has been clearly mentioned in [15-19] and how to use different tools for various stages of implementation and verification processes. During the verification suitable test vectors should be applied to the architecture for the functional verification. The area and hardware utilization reports (i.e number of LUTs required to implement the reconfigurable FIR filter bank) can be generated through HDL editors (like Xilinx). The propagation delays can be verified after the place and route step. The best way to verify the delays is on the FPGA kit. Applying the test vector at the input of the filter on the FPGA and verify delay to produce the valid filter output. Proper selection of the coefficients and architectures should be used to implement the filters for better speed results.

III. CONCLUSION

This paper presents various ways to implement Reconfigurable FIR filter bank using partial reconfiguration, coefficient allocation and canonical signed digit based filter design. These methods produce efficient architectures for energy efficiency, area efficiency and fast reconfigurable filters. The filters having large band widths and energy efficient architectures are suitable for future communication needs. This paper gives an insight to such architecture.

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