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8 - Bit Parallel Divider using Galeor Technique to reduce Leakage Current using 45nm technology"

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ABSTRACT –In this paper we propose a new technique for implementing low leakage current of 8-bit parallel divider using galeor technique in which a n-type and a p-type gated leakage transistor (GLTs) are inserted in series between the pull-up and pull-down network, and the gate of both transistor is connected by the drain of the other. The parallel divider is designed based on series of shifting and subtraction algorithm .The implementation of 8 bit parallel divider consists of several combinational and sequential components such as 5-bit subtractor, 2:1 multiplexers, D flip-flops and 5-bit comparator ,9-bit PIPO shift left register, 6-wide MUX, 9-wide MUX . The circuit analysis is carried out in terms of performance parameters such as leakage current and power consumption. According to the estimations done, the leakage current and power consumption of the parallel divider without parasatics was found to be 40nA and 0.12 mw respectively.

KEYWORDS – galeor, divider, leakage current

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I. INTRODUCTION

In digital devices, Divider is the most commonly used circuit. Division is one of the arithmetic operations performed by divider in the various analog and digital circuits. Design targets of divider are high speed, low power consumption, regularity of layout and therefore less area required or even combination of them in one divider are required in that way making them suitable for various VLSI implementations. Division is one of the basic functions used in digital signal processing same as addition, subtraction, multiplication.

To reduce leakage current so many techniques are available sleep transistor technique, Forced stack technique, Sleepy stack technique and the latest technique named as GALEOR technique. These techniques listed above reduces the leakage by stacking leakage path using the off transistors. In GALEOR technique the gated leakage transistors are used in between pull-up and pull-down network . here, we use galeor technique to reduce leakage current of 8-bit parallel divider circuit.In this galeor technique, two gated leakage transistors (a n-type and a p-type) within the logic gate for which the gate terminal of each gated leakage transistor (GLTs) is connected to the drain of the other transistor. The operation of division in parallel divider is done by means of shifting and subtraction. Suppose we want to divide 135 by 13. So at every step, shift dividend left and compare its five MSB with current divisor if divisor is larger, shift 0 as the next bit of the quotient if divisor is smaller, subtract to get new dividend and shift 1 as the next bit of the quotient after the completion of the process at the end we get 4-bit quotient which is 10 and 5-bit remainder which is 5 in dividend register. Binary division is done in the same way. The proposed 8-bit binary

parallel divider using GALEOR technique using 45nm is implemented using Tanner EDA tool .

II. RELATED WORK

CMOS is the universally used technology to construct integrated circuits. Static CMOS is the most commonly used logic style which consists of pull down network (PDN) and pull up network (PUN). It is truly an advanced version of the static CMOS inverter with multiple inputs. There are so many methods for leakage power or leakage current control.

Shashank Gautam .et.al. [1] presents paper on "analysis of combination circuit (full adder) is perform using galeor technique" A Full Adder has been designed using these techniques and power dissipation is calculated and is compared with general CMOS logic of Full Adder. Simulation results show the validity of the proposed techniques is effective to save power dissipation and to increase the speed of operation of the circuits to a large extent. the circuit is simulated on LT Spice to reduce leakage current.

Sagar Ekade .et.al. [2] presents paper on "analysis of leakages and leakage reduction methods in USDM CMOS VLSI " circuit in which lector technique , galeor technique are shown for reduction of leakages.

Stuart F. Oberman .et.al. [3] The fundamental issues in the design of a digit recurrence divider are the radix, the choice of allowed quotient digits, and the representation of the intermediate remainder. The radix determines how many bits of quotient are retired in an iteration, which fixes the division latency. Larger radices can reduce the latency, but increase the time for each iteration. Judicious choice of the allowed quotient digits can reduce the time for each iteration, but with a corresponding increase in complexity and hardware. Similarly, different representations of the intermediate remainder can reduce iteration time, with corresponding increases in complexity.

C.P. Wang.et.al. [4] "design of a fast radix -4 SRT divider and its VLSI implementation". In which the design of a fast divider is an important issue in high-speed computing. Instead of finding the correct quotient digit, an estimated quotient digit is first speculated. The speculated quotient digit is used to simultaneously compute the two possible partial remainders for the next step while the quotient digit is being corrected. Thus, this two-step process does not influence the overall speed. Since the decision making circuits can be implemented with simple gate structures, the proposed divider offers fast speed operation. Based on the physical layout, the circuit takes 247ns for a double precision division (56 bits for fraction part), where the 2 um CMOS technology in MAGIC is employed and simulated.

Bandan kumar bhoi .et.al. [5] paper presents "novel binary divider architecture for high speed VLSI applications". In which novel binary divider architecture for high speed VLSI applications using such ancient methodology which is vedic mathematics. The functionality of the circuits was checked and performance parameters like delay and dynamic power consumption were calculated by xilinx ISE using 90nm CMOS technology. The power consumed 34mw and propagation delay 19.9ns.

III. GALEOR TECHNIQUE

Two gated leakage transistors are placed between the pull up and pull down networks of dynamic circuits which are operated with clock. Gated leakage transistors are Pmos and Nmos. Pmos GLT is placed in between output and pull up network. Nmos GLT is placed in between output and pull down network. The gate terminals of both gated leakage transistors are connected to drain terminals. Otherwise, the drain voltages are controlling the gate terminals of leakage transistors. The leakage current is reduced by the usage of GLT's . It is done by increasing the resistance from Vdd to Vss as one of the GLT's enters in to cut off region. It has a setback of low voltage swing even though it reduces the leakage current to large extent. Low logic is not perfectly zero it is larger than 0v and high logic is not exactly Vdd it is lower than Vdd. So, the voltage swing is reduced and increases the delay.

GALEOR technique uses two extra transistors (a n-type and a p-type) called gated leakage transistors (GLTs) inserted in series between pull-up network and pull- down network in each CMOS gate as shown in Fig 1. In this technique high threshold voltage used for gated leakage transistors. Transistor states and stacking effect introduced by the transistors in a GALEOR implemented gate family for all possible input combinations. When we used these technique

GALEOR then voltages of the output wave forms suffered a significant problem. That is, the low signal is very much higher than 0 volt in addition, GALEOR causes high signal much lower than the Vdd. The output wave form as the low signal is 0.2v for GALEOR and the high signal for GALEOR is 3V, rather than 0V and 1.5V, respectively. Similar troubling behaviors are consistently observed for all other gate types such as OR, AND, XOR.

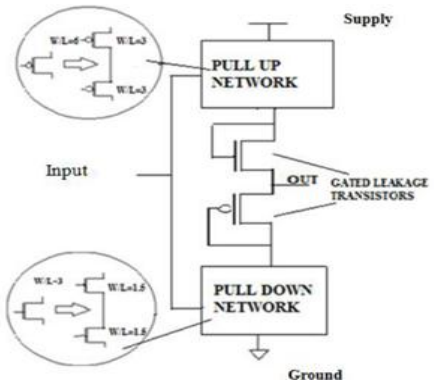

Fig. 1 Generalised structure for gated leakage transistor

IV. 8-BIT DIVIDER USING GALEOR TECHNIQUE

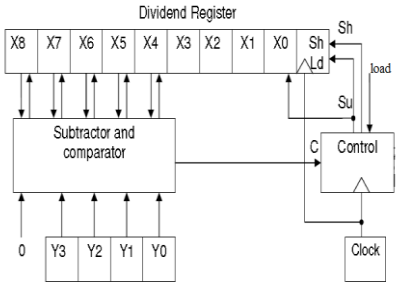

Fig.2 Block diagram of 8 bit parallel divider

The operation of divider can be explained in terms of block diagram of fig 2. A shift signal (sh) shifts the dividend one bit left. A subtract signal (su) will subtract the divisor form the five left most bit in the dividend register and set quotient bit (the rightmost dividend register) to '1'. If the divisor is greater than the 4 leftmost dividend bit , the comparator output c=0 ,otherwise c=1. The control circuit generates the required sequence of shift and subtraction signal. Whenever c=1, a subtract signal is generated which shows that dividend is greater than or equal to divisor and subtract operation takes place and set rightmost quotient bit '1'

Fig.3 shows schematic representation of 8 bit parallel using galeor technique in which the circuits are represented in a symbolic form. Therefore the output waveforms and leakage current waveforms are shown in fig.4 and fig 5 respectively. Leakage current is less in the circuit in which we use the galeor technique and therefore fig 6 shows the leakage current of the circuit in which we did not use the galeor technique. Then we can compare the result of both the circuits.

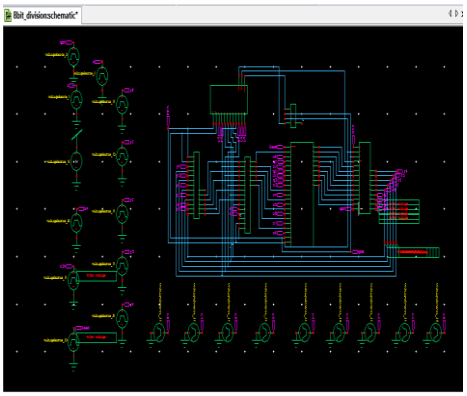

Fig.3 Schematic of 8 bit divider using galeor technique.

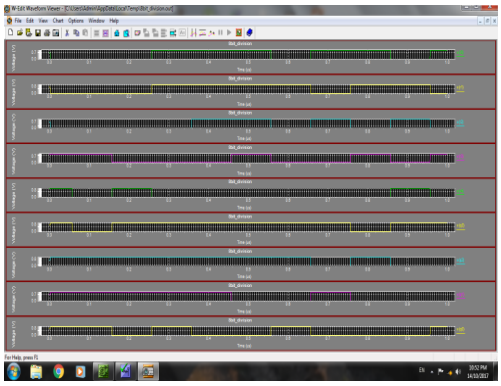

Fig.4 Output of 8-bit parallel divider (135/13)

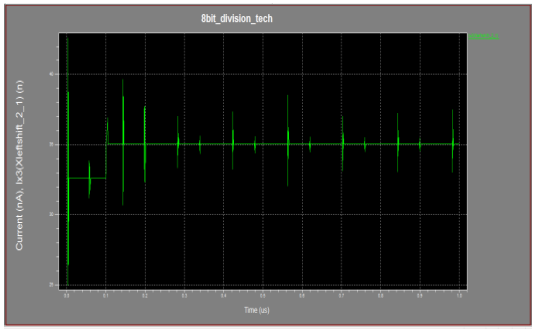

Fig 5 Leakage current waveforms of 8-bit parallel divider using galeor technique

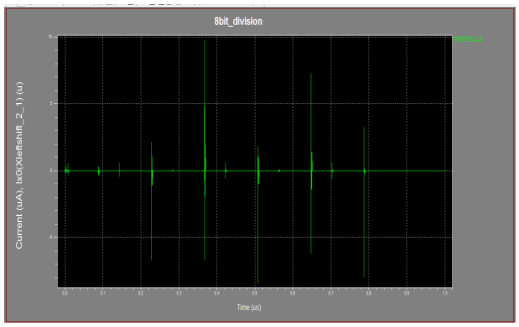

Fig 6 Leakage current waveforms of 8-bit parallel divider without galeor technique

V. RESULT

Table I. Result

Parameter	**8-bit parallel divider**	**8-bit parallel divider using galeor technique**
Leakage current(A)	10uA	40nA
Power consumption (w)	2.72mW	0.12uW
Delay(s)	0.15us	0.19us

VI. CONCLUSION

It is clear from the table that while using simple circuit, leakage current is 10uA and power consumption is 2.72mW and while using the circuit using galeor technique, leakage current is 40nA and power consumption is 0.12uW . But the circuit using galeor technique delays the output more as compared to the simple circuit as shown in the table.

FUTURE SCOPE

In future we can implement this 8-bit parallel divider on arithmetic logic unit (ALU) for the faster operation of circuit and also used in computer architecture. By using GALEOR technique the performance of circuit increases due to reduction in leakage current.

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