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Implementation of Minimum Delay Voltage Level Shifter for Multisupply Voltage Designs

Jalla Chinnari[1], varisa sasibhushanarao[2]
Department of Electronics and Communications, IIIT srikakulam ,RGUKT srikakulam, India.
Corresponding Author: Jalla Chinnari

ABSTRACT: voltage level shifters are used to convert voltage levels in low range to high range with a limit for this reason Voltage Level Shifters are frequently used in many integrated circuits these days its presence applicable in analogue computers, simulation systems and in many electronic applications as filtering, buffering and comparison of signal levels. Here addressed the various types of voltage level shifters, mainly implementation was done on minimum delay voltage level shifter for multisupply voltage designs before going to this need to have the idea about wide range modified Wilson current mirror hybrid buffer It have a ability to convert the levels in subthreshold to above-threshold signal levels. But in produce large propagation delays would be observed due to the low subthreshold drive strength of the main shifter stage. In order to avoid this drawback implementation was done with minimum delay voltage level shifter for multisupply voltage designs. This circuit reduce the propagation delay because here apply deep subthreshold voltage to the standard supply voltage, strength of pull-up networks is adapted to the next output switching transition this factor reduces the delay.

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I. INTRODUCTION

A voltage level shifter has a supply line receiving a supply voltage that varies between a first operating value in a first operating condition and a second high operating value, in a second operating condition [1], [2]. A latch stage is connected to an output branch and to a selection circuit, which receives a selection signal that controls switching of the latch stage. In digital circuits dynamic and short-circuit power consumption is reduced by lowering the value of the power supply voltage. It can be also reduced by increased supply voltage; because of this propagation delay of the circuits was increased. On the other hand minimized headroom in analog circuits decreases signal swings due to these increases the sensitivity to noise. Hence, in moderate-speed mixed signal circuits or in digital circuits where different parts operate at different speeds, dual-supply architectures are introduced in which a low voltage (i.e., VDDL) is supplied for the blocks which are in noncritical paths while analog and the high-speed digital blocks are driven by a high supply voltage (i.e., VDDH) [3].In a system with dual supply voltages, level-shifting circuits are needed to convert the lower voltage levels into the higher ones to provide correct voltage levels for the succeeding digital blocks. In this manner to alleviate the degradation of the entire performance of the circuit, the required level shifters must be implemented with minimum propagation delay and silicon area.

The remaining of this paper is organized as follows. In Section II, wide range modified Wilson current mirror hybrid buffer circuit is reviewed. The proposed circuit is introduced in Section III. Section IV presents the simulation results of the designed circuit verifying the efficiency of the proposed structure. Finally, this brief is concluded in Section V.

II. MODIFIED WILSON CURRENT MIRROR CIRCUIT HYBRID BUFFER

A modified Wilson current mirror (MWCM) is located in Block 1. When VDD1 is subthreshold and VDD2 is high, the MWCM structure balances the rising and falling delay at Node A, without losing the original static bias that is favored in the WCM LS. However, when the VDD1 and VDD2 levels are close, the MWCM encounters the same problem as the WCM does: the cascade PMOS has insufficient drive currents and increases the rising delay. Therefore, in Block 3, a delay path is designed adaptively to reduce the rising delay and maintain a moderate duty cycle. An output inverter offers sufficient drive strength, which is required in a standard cell design. Unlike the CCPNR LS, which has a similar structure, the proposed LS uses a CM-type amplifier, a balancing

delay path, and a complementary OR gate in Block 2.

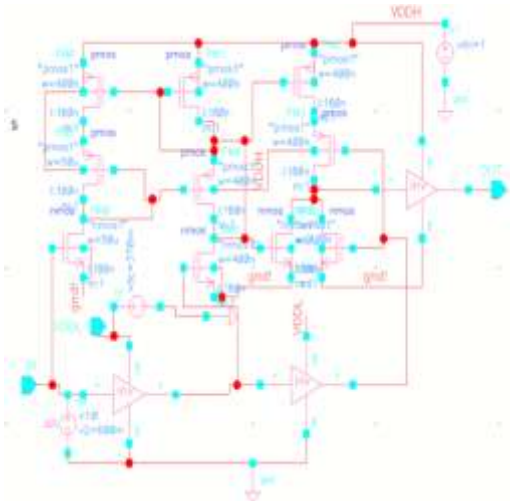

Fig. 1. A Wide Range Level Shifter Using A Modified Wilson Current Mirror Hybrid Buffer

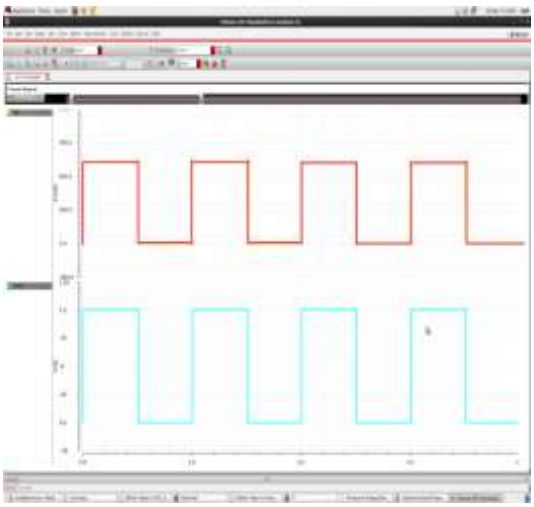

Fig. 2. Output Waveforms of Modified Wilson Current Mirror

Modified Wilson current mirror have the output wave forms same as the input waves but it have some voltage shifting it converts low input voltage into high output voltage. Here the input value is 0.6V it means it is in subthreshold region but after the entire operation of the circuit it gets 1V is the output value The wide range modified Wilson current mirror circuit have the power consumption of 101.9nW and delay of 10 ns[4]. Compared to conventional voltage level shifter with Wilson current mirror structure the modified Wilson current mirror have the reduced power consumption but the delay of the circuit war increased in 10 times compared to voltage level shifter with Wilson current mirror

III. MINIMUM DELAY VOLTAGE LEVEL SHIFTER FOR MULTISUPPLY VOLTAGE DESIGNS

Wide-range level shifters play important roles in ultralow- voltage circuits and systems. Although state-of-the-art level shifters can convert a subthreshold voltage to the standard supply voltage, they have limited operating ranges, which rule the flexibility of dynamic voltage scaling. Therefore, a novel level shifter, which has operating range is from a deep subthreshold voltage to the standard supply voltage and added upward and downward level conversion. A hybrid structure comprising a modified Wilson current mirror and generic CMOS logic gates. The simulation and measurement results were verified using a 180-nm technology [5]. The minimal operating voltage of the level shifter was less than 600 mV based on the measurement results. In addition to the operating range, the delay and power consumption level shifter were designed for practical applications.

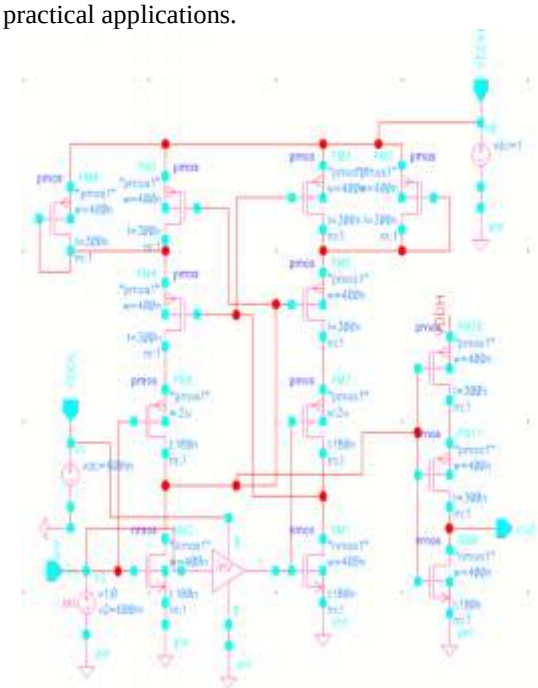

Fig. 3. Minimum Delay Voltage Level Shifter for Multisupply Voltage Designs

It combines the multithreshold CMOS design technique and novel topological strategies. The circuit has of an input inverter, a main voltage conversion stage and an output inverting buffer. The input inverter (MP1/MN1) is designed using low threshold voltage (lvt) transistors. This provides fast differential low-voltage input signals to the main voltage conversion stage. To have higher strength of the pull-down network, also MN2 and MN3 are lvt transistors. Then, two lvt

pMOS devices (MP2 and MP3) are added to both the branches of the circuit[6]. These devices limit the cross-bar current that is the current flowing in the pull-up network and opposing to the discharge of NH (or NL) node at the beginning of their high to low transition. To further facilitate the high to low transition at the nodes NH and NL, MP4 and MP5 are high threshold voltage (hvt) transistors. This choice also reduces leakage current flowing through the pull-up networks when MP4 or MP5 are turned off [7]. However, using hvt, pMOS transistors has the counter effect of slowing the low to high transition of the nodes NH and NL. Introducing the parallel connected hvt devices MP6-MP7 and MP7-MP8, with MP6 and MP7 being diode connected transistors. The latter devices impose two variable virtual power supplies VNHH and VNLL on the two branches of the circuit. Therefore, the strength of pull-up networks is adapted to the next output switching transition.

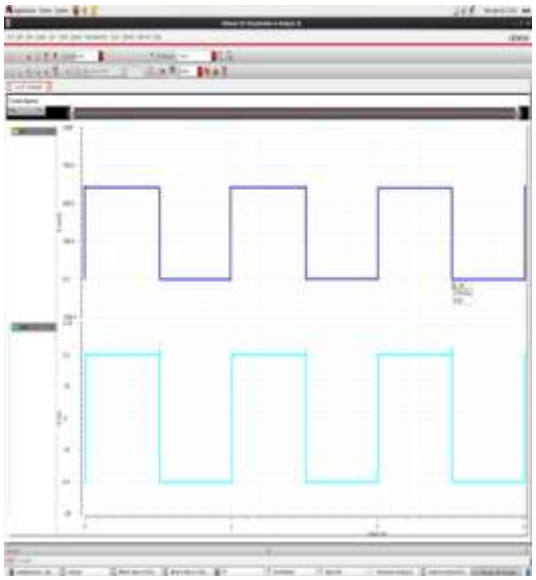

Fig. 4 output waveforms of Fast and Wide Range Voltage Level Shifter

To reduce the switching delay, a pull-up network able to self-adapt its strength to the actually occurring transition would be desirable. This behavior was obtained by when the output Z is initially low (high), the pull-up network of the left branch is weakened (strengthened) and that of the right branch is strengthened (weakened), thus speeding-up a low-to-high (high-to-low) output transition

IV. SIMULATION RESULTS

The proposed voltage level shifter was verified by using Cadence virtuoso in standard TSMC 0.18µm CMOS technology. The bend results have reduced power-delay product (PDP).

Table.1. power, delay and transistor count reports in 180nm Technology

. Circuit	Power	Delay	Transistor Count
A Modified Wilson Current Mirror Hybrid Buffer	247nW	3.23ns	14
Minimum Delay Voltage Level Shifter for Multisupply Voltage Designs	258nW	2.24ns	16

The given table contains the values at different frequencies and for various values of V_{ddl}, The delay and power are observed, the contention between devices is observed in sub-threshold region. Due to lower temperature the time required to generate signals will be increased and also produce less current.

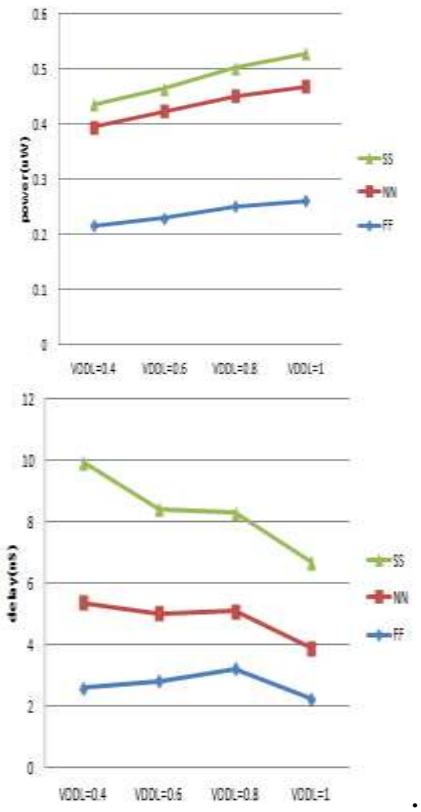

Fig. 5 Graph for Delay and power report at different Values of VDDL, on various corners.

This graphs shows the simulated output values of power and delay at different values of VDDL when supply voltage increases then power consumption increases and delay was reduced. In Fig. 6 shows the delay and the power report of the entire circuit.

V. CONCLUSION

In this paper the proposed circuit and existing circuit both are implemented in cadence virtuoso and observed the output functioning at different voltages to know the power levels at every point. The experimental results show the circuit with Minimum Delay Voltage Level Shifter for Multisupply Voltage Designs minimizes the power delay increase the speed by using the delay path adaptively it reduces the rising delay and maintain a moderate duty cycle. The overall circuit achieves on average 45% of time savings by connecting the delay path.

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