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Design Analysis of Deblocking filter for HVEC standard

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ABSTRACT
High Efficiency Video Coding (HEVC) has been developed to achieve a better compression standard over the existing compression schemes for the same perceptual video quality. The design of Deblocking filter is a vital components to achieve better video quality as it reduces the blocking artifacts. In this paper, five stage pipelined deblocking filter hardware structure is analyzed to achieve better throughput compared to iterative based deblocking filter. The Verilog HDL code verified in Xilinx 14.5 environment.
Keywords - Deblocking filter, high efficiency video coding (HEVC), parallel processing, parallel filtering, VLSI.

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I. INTRODUCTION

Rapid changes in multimedia communication demands for high data rate video transmission, these are put forward on the video coding technologies. Joint collaborative team on video coding (JCT-VC) developed a new video compression standard which achieves a compression 50% compression rate than the H.264 standard with same perceptual Quality [1,2]. In HVEC, each frame further divided into 64 x 64 blocks known as coding tree units [3]. These CTUs are further divide into smaller blocks. Complete bit stream pattern is obtained after transformation, quantization and entropy operations [4]. In the prediction phase of HEVC, some disturbance is created due to the misalignment of blocks known as blocking artifacts. The main purpose of Deblocking filter is remove the blocking artifacts frame due to coarse quantization [5]. Filtered frame is used as a reference frame to predict the future frames for motion prediction [6,7]. The DBF used in the HEVC is less complex than that of H.264 [8,9] as it passes 8x8 blocks instead of 4x4 blocks.

The rest of this paper is organized as follows. HVEC in-loop filter is explained in section II. Deblocking filter algorithm is explained in section III . Various architectures for deblocking filter are explained in section IV. Hardware implementation Deblocking filter with simulation results comparison are explained in section IV, Finally the conclusions are drawn in section V.

II. HEVC INLOOP FILTERS

In HEVC encoding and decoding stages two types of in loop filter are used after the quantization and before saving into buffer. The deblocking filter is important among the other filter to reduce the ringing artifacts [10]. The important advantage of in loop filter is improved quality of reconstructed picture. The purpose of the deblocking filter is to reduce the discontinuities in transform and prediction boundaries. Transform and motion prediction boundaries are used to remove the redundancies occurred in HEVC video coding. These techniques are block based and varies from 8x4, 4x8 and 64x64 Luma samples. While the size of block transforms and intra-predicted blocks varies from 4x4 and 32x32 samples. These blocks are coded relatively independently from the neighboring blocks and approximate the original signal with some degree of similarity. Since coded blocks only approximate the original signal, the difference between the approximations may cause discontinuities at the prediction and transform block boundaries [11-13]. These discontinuities are attenuated by the deblocking filter.

III. DEBLOCKING FILTER ALGORITHM

To In HEVC filtering operations performs on horizontal and vertical edges of adjacent 8x8 block boundary. The overall processing steps of deblocking filter is shown in Fig.1.

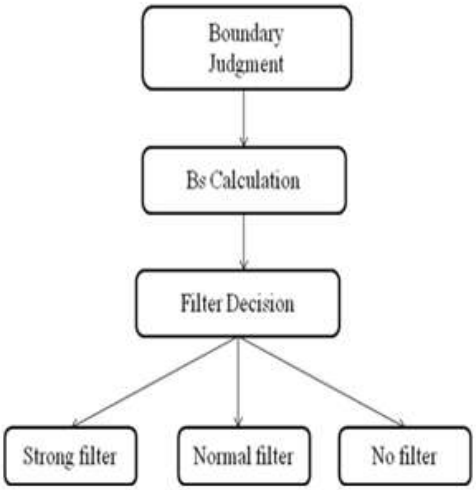

Fig.1. Processing Steps Deblocking Filter**.**

From Fig.1, the first step is the boundary judgment. In this current boundary judged to determine the type of boundary(CU.PU or TU). If neither exists, the current boundary processed without applying the any boundary. The second stage is the Boundary strength calculations. In this BS values are calculated for PU or TU boundaries. Finally filter is decided based on the filter parameters such as β, tc and dpq. At last, the corresponding filter is applied to the boundaries.

A. Boundary Judgment

The most difficult part in designing the deblocking filter is to decide whether the particular block boundary is filtered or not then the filtering strength is applied. Over filtering leads to excessive smoothing and at the same time lack smoothing may cause artifacts which reduce the quality of the image. In standard HEVC a recursive loop method [10] is used for boundary judgment to decide the current boundary is a boundary from CU, PU or TU. However recursive method suffers from high computational complexity. The fast and boundary judgment method is proposed to reduce the complexity and is explained in detailed in paper [14].

B. Boundary Strength Calculation

The purpose of the Boundary strength is decide how strong the filtering is needed. It value varies from 0 to 2. The value determines the predicted mode and motion vector for a reference frame. The more detailed explanation is given in [14].

C. Filtering Design

The filtering operation is performed based on the BS value. If BS is '0' then no filtering operation is performed. If its value is greater than '0' then filtering operation is required or not is decided for block boundary . Each block boundary consists of four samples. The Luma operation and Chroma operation is decided based on BS value.

IV. HEVC DEBLOCKING FILTER ARCHITECTURES

Different Deblocking filter architectures are proposed over the years. In [13], parallel architecture for both normal and strong filtering modes of deblocking filter is proposed. The architecture can able realize the 4KUHD video at 30 fps with an operating frequency 54MHz. Multi parallel high through put deblocking filter architecture is proposed in [14]. This includes three main modules one is the filtering module having four filters and are operated in parallel and other modules are control and memory modules. Boundary judgment is implemented in friendly method. But having slight high utilization of hardware. In this paper five stage deblocking filter is considered as shown in the Fig. 2.

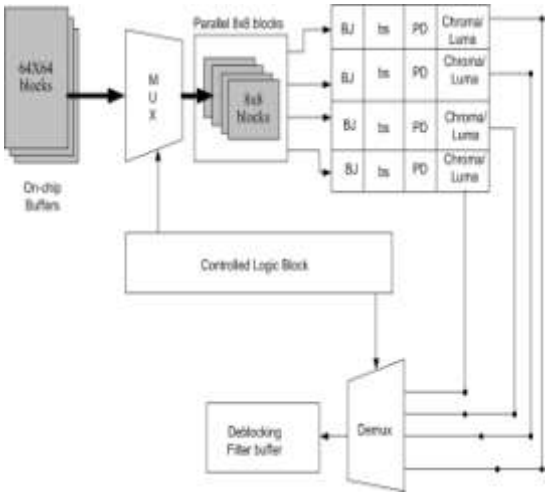

Fig. 2. Five stage Deblocking Filter

From the architecture shown in Fig.2 , Initially Mux selects the selects the on the 64 x64 block and is divided into parallel 8x8 blocks. In the next stage boundary judgment is performed in 8x8 block Each edge is processed either vertical judgment or horizontal judgment. After that boundary selection is processed. The internal architecture for BS is almost similar to the BS in[14],which is having comparators and multiplexers and then it processed to filtering for the Luma component or the chorma blocks . Finally the values are stored in the filter buffers and are considered as internal memory units which reduces the on chip area of HEVC deblocking filter.

V. HARD WARE IMPLEMENTATION OF DEBLOKING FILTER IN XILINX

The HEVC architecture is designed and analyzed in Xilinx platform using Verilog HDL programming . The results for the individual blocks are shown in Fig3 to Fig 9.

Fig.3. Simulation results of Horizontal Boundary Judgment.

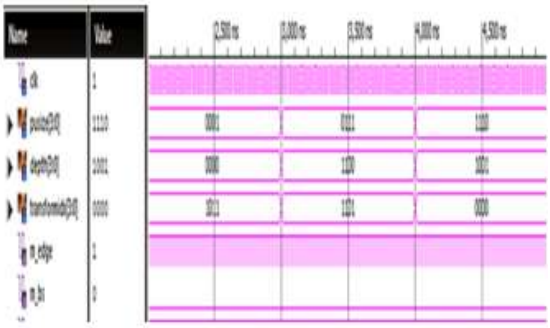

Fig.4. Simulation results of Vertical Boundary Judgment.

Fig.5. Simulation results of BS calculation

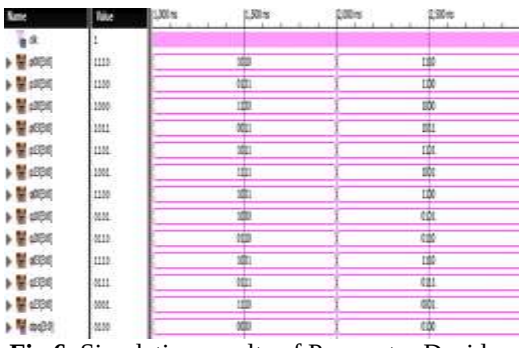

Fig.6. Simulation results of Parameter Decider.

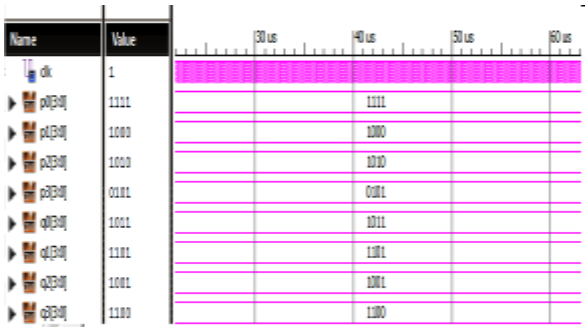

Fig.7. Simulation results of Luma filter.

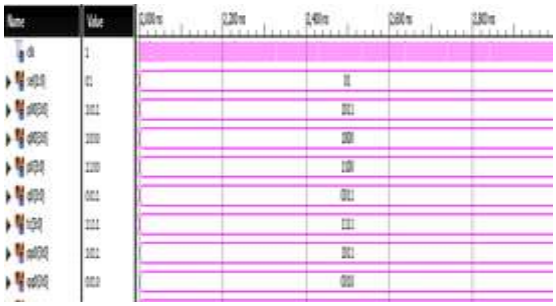

Fig.8. Simulation results of Chroma filter.

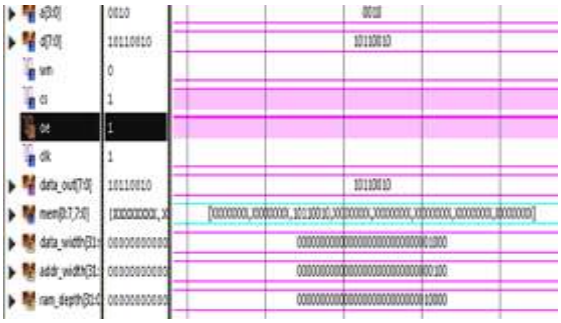

Fig.9. Simulation results of SRAM

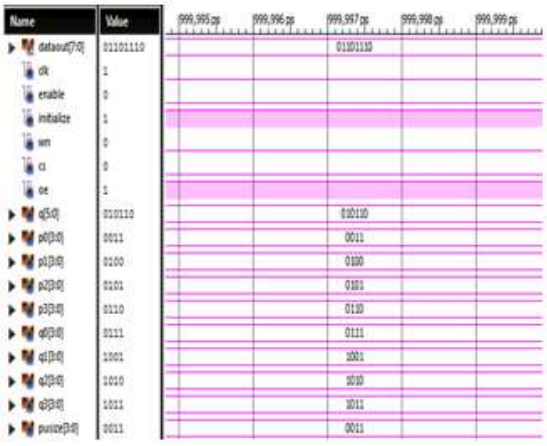

Fig.10. Simulation results of de blocking filter.

Fig 10 Shows the deblocking filter simulated using Verilog code and the corresponding RTL schematic is shown in Fig11.

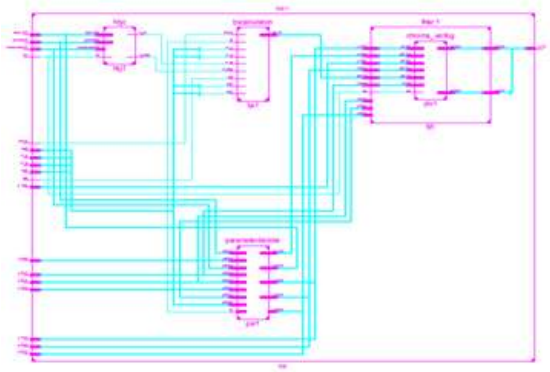

Fig.11. RTL Schematic of HEVC deblocking filter Architecture.
Summary of deblocking filter is shown in Table.1

Table.1. Design summary of HEVC deblocking filter

PARAMETERS	VALUE
No of Slices (in %)	5
No of flip flops (in %)	9
No of 4 input LUTs	11
No of bonded IOBs	14
Min clock period	3.492ns
Frequency	28.369MHz

From the Table .1, it is observed the designed HEVC deblocking filter utilizes slices count of 5 with flip-flop count of 9 and so on. Finally Fig.12 differentiates the non blocking and deblocking filter image.

(a) No blocking

(b)blocking is on

Fig.19. Subjective results of deblocking filtering.

VI. CONCLUSION

In this paper HEVC Deblocking filter is designed and analyzed using Xilinx 14.5 environment. It reduces the blocking artifacts better throughput compared to iterative based deblocking filter.

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REFERENCES

[1]. G. J. Sullivan, J. R. Ohm, and W. J. Han, Overview of the high efficiency video coding (HEVC) standard, IEEE Trans. Circuits Syst. Video Technol., vol. 22, no. 12, pp. 1649–1668, Dec. 2012.

[2]. J.-R. Ohm, G. J. Sullivan, H. Schwarz, T. K. Tan, and T. Wiegand, "Comparison of the coding efficiency of video coding standards-including high efficiency video coding (HEVC)," IEEE Trans. Circuits Syst. Video Technol., vol. 22, no. 12, pp. 1669–1684, Dec. 2012.

[3]. G. Zhai, W. Zhang, X. Yang, W. Lin, and Y. Xu, "Efficient deblocking with coefficient regularization, shape-adaptive filtering, and quantization constraint," IEEE Trans. Multimedia, vol. 10, no. 5, pp. 735–745, Aug. 2008.

[4]. A. Norkin et al., "HEVC deblocking filter," IEEE Trans. Circuits Syst. Video Technol., vol. 22, no. 12, pp. 1746–1754, Dec. 2012.

[5]. W. Shen, Q. Shang, S. Shen, Y. Fan, and X. Zen, "A high-throughput VLSI architecture for deblocking filter in HEVC," in Proc. IEEE Int. Symp. Circuits Syst., May 2013, pp. 673–676.

[6]. K. Ugur, K. R. Andersson, and A. Fuldseth, "Video coding technology proposal by Tandberg, Nokia, and Ericsson," presented at the Joint Collaborative Team

on Video Coding, Dresden, Germany, Apr. 2010, ITU-T SG16 WP3 and ISO/IEC JTC1/SC29/WG11 doc. JCTVC-A119.

[7]. G. Khurana, A. Kassim, T. Chua, and M. Mi, "A pipelined hardware implementation of in-loop deblocking filter in H.264/AVC," IEEE Trans. Consumer Electron., vol. 52, no. 2, pp. 536–540, May 2006.

[8]. W. Shen, Y. Fan, Y. Bai, "A Combined Deblocking Filter and SAO Hardware Architecture for HEVC," IEEE Trans. Multimedia, vol. 18, pp. 1022–1033, no. 6, June. 2016.

[9]. S. Baldev, K. Shukla, S. Gogoi, "Design and Implementation of Efficient Streaming Deblocking and SAO Filter for HEVC Decoder," IEEE Trans. Consum. Electron, vol. 64, pp.127-135, no. 1, Feb 2018.

[10]. E. Ozcan, Y. Adibelli, I. Hamzaoglu, "A High Performance Deblocking Filter Hardware for High Efficiency Video Coding," IEEE Trans. Consum Electron, vol. 59,pp.714-720, no. 3, Aug 2013.

[11]. H. Azgin, A. Can Mert, "An Efficient FPGA Implementation of HEVC Intra Prediction," in Proc. IEEE Int. Conf. Consum. Electron. , 2018, pp. 818-822.

[12]. K. Runlong, Z. Wei, H. Xiaodong, "An Efficient Deblocking Filter Algorithm for HEVC," in Proc. IEEE Int. Conf. Image Process., 2014, pp. 379-383.

[13]. Awais KHAN, et.al., "FPGA implementation of a HEVC deblocking filter for fast processing of super high resolution applications", Turk J Elec Eng & Comp Sci, Vol 24, 24: pp. 4661 – 4669,2016.

[14]. Wei Zhou, A High-Throughput and Multi-Parallel VLSI Architecture for HEVC Deblocking Filter" IEEE Trans. Cons. Electronics,2016.

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