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RESEARCH ARTICLE OPEN ACCESS

Differential Amplifier using CMOS Technology

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ABSTRACT: This paper aims to explain how to design a differential amplifier using CMOS technology. As indicated in Electronic contexts, the differential amplifier is one of the widely known and the basic building block in creating an analog circuit. Its characteristics are measured by Gain, its Bandwidth outcomes, and Common Mode Rejection Ratio (CMRR). We present a circuit comprising bipolar and MOS transistors. Its course uses NMOS and PMOS devices wherein the N-channel will be used to formulate differential pair, and P-channel current mirror load is applied. This design will present its optimized architecture using 0.18 μm and a supply voltage of 1.8V and its simulation and design is demonstrated using ADS tool.

Keywords: Differential Amplifier, CMOS

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I. INTRODUCTION

Over the decades, the epoch of very-large-scale integration (VLSI) technology has been contributed by the tremendous change in the electronics industry. Most significant changes were introduced in the market because of the invention of the MOS transistors. The small, medium and large-scale integration of the Integrated Circuits to over ultra-scale integration has changed and modified the electronic world.

The differential amplifier is a form of amplifier that strengthens the difference between two voltages in a circuit. In electronic designs, we use a differential amplifier to produce high voltage gain and high CMRR. Its main characteristics include very low bias current input, very high impedance input, and very low offset voltage. The essential benefit of differential mode from common mode is its higher immunity to noise. Also, differential amplifiers provide better immunity to environmental noise, improve linearity, and more upper signal swing.

It may operate in two modes: common mode and differential mode. The common method produces a zero voltage output result while the differential mode produces a high voltage output result. Given this, the differential amplifier generally has high CMRR. If the two input voltages are of similar value, the amp provides an output voltage value that is almost zero. When the two input voltages are unequal, the amplifier produces a high voltage output.The remarkable advantage of differential operation over common mode operation is its higher immunity to noise. Another advantage is the increase in voltage swings, wherein the peak to peak voltage swing is equal to 2 [V_{DD} - (V_{GS} - V_{TH})].

MOS transistor enhances the strength of CMOS technology. CMOS technology is used to satisfy all the design restrictions like power, speed, and area by minimizing the feature size and using the optimization techniques. These techniques are used in lowering the supply voltage, using VTCMOS and MTCMOS, etc.

CMOS differential amplifiers are more widely used for various applications as compared to single-ended amplifiers. A fully differential amplifier circuit produces two inputs and two outputs. In designing differential amplifiers, sensitivity is an essential specification. While the component is matching, their drift induces other output differential voltage that is unclear from the signal being processed. This voltage controls the minimum predictable differential voltage level. Such mismatch could convert the common mode input signal to the differential output, wherein it is treated as the desired signal by the following stages.

II. OBJECTIVE

This paper demonstrates a design of a differential amplifier using 0.18μmwith a supply voltage of 1.8V CMOS technology. From the various topologies, we will use the NMOS PMOS current meter load to achieve the specifications and purpose of the circuit.

III. CONTENT

1.1 The Role of Differential Amplifier and its Basics

The differential amplifier boosts the difference between the two input signals demonstrated as V+ and V-and rejects any common

signals from the two sources.Its ideal characteristics are infinite bandwidth, gain, and common mode rejection ratio (CMRR); and high input impedance, less distortion, and low output admittance. It is also characterized to have less harmonic distortion and high output voltage swing. Its characteristics test the effective performance of the circuit.

These amplifiers are broadly used in linear amplificationcircuits to obtain less distortion at the output. They can be designed in multiple ways, providing a result where output may be single or double ended. However, the most commonly used in designing a differential amplifier is the double ended, wherein two inputs provide two outputs, called a fully differential amplifier. Its advantage over single ended is simple biasing, high linearity, and high immunity to noise. But it has a large area to cover.

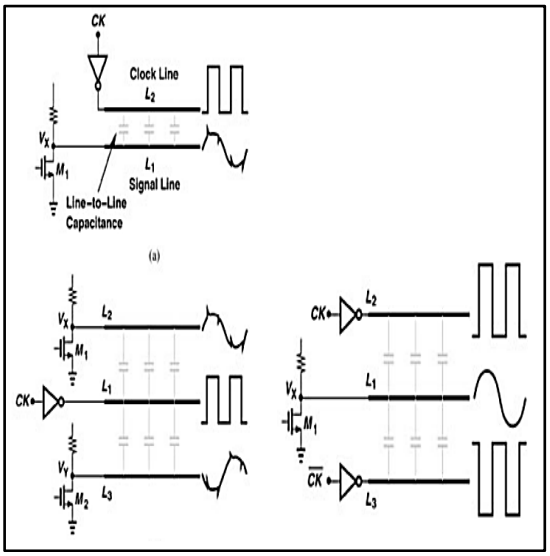


Figure1. Illustration of DA's High Immunity to Noise Coupling

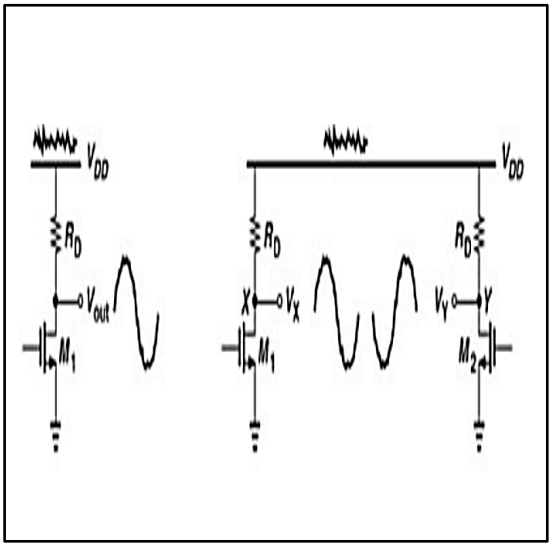


Figure2. Illustration of Supply Noise Reduction

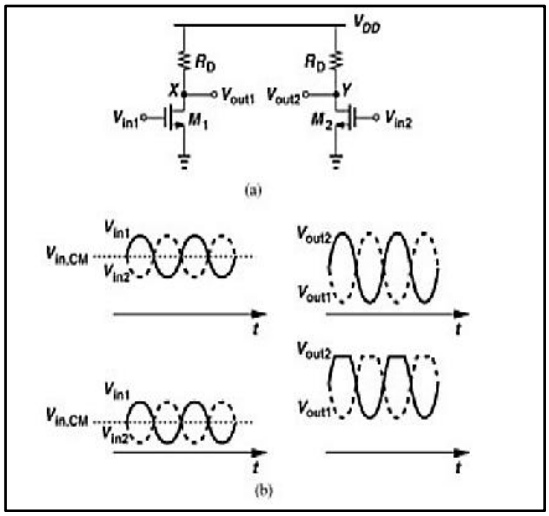


Figure3. Basic Differential Pair

A feedback circuit like common mode is used at the output of the amplifier to adjust the bias current and therefore rejects the common mode signals. Within the two types of offset voltages, the input offset and output offset voltage, the latter is defined as the difference from the final output voltage to the ideal output voltage when a common signal is applied at both end inputs. The same, when the differential voltage gain divides the output offset voltage; it is called the input offset voltage.

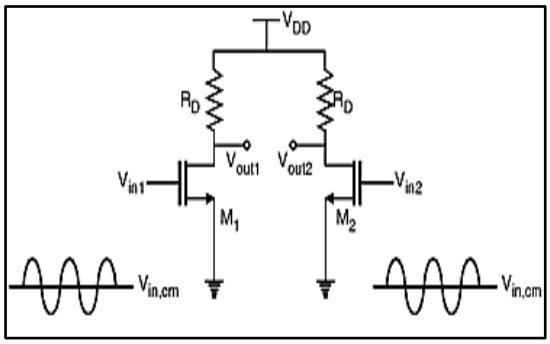


Figure4. Simple Differential Amplifier

From the circuit illustrated in Figure4, when V_{in1} and V_{in2} have a huge unequal common mode dc level, this means that the output response has distortion.When $V_{in.cm}$ changes, the M_1 and M_2 bias currents also change. Hence, the transconductance of the devices and its output common mode dc level change. This leads to a small amplifier signal gain, which becomes the problem.

To solve this issue, the circuit is modified by applying a current source (Iss) to make the I_{D1} and I_{D2}independent from $V_{in.cm.}$The revised figure

below is the circuit incorporating the I_{ss} current source.

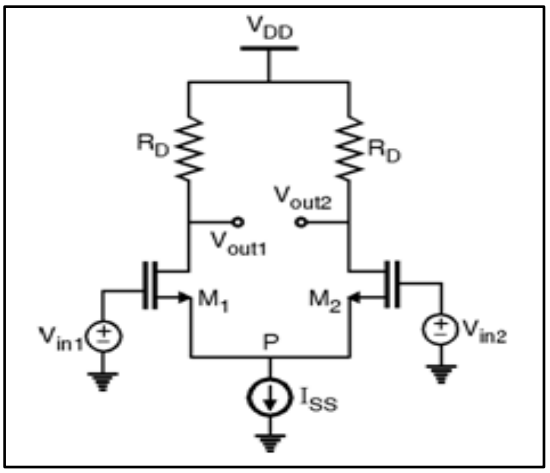


Figure5. The Basic Differential Amplifier

When the two inputs V_{in1} and V_{in2} are equal, the biasing current of the single transistor is equal, and the output common mode level is V_{DD}-.A minimum bias current is needed to maintain the common mode level.

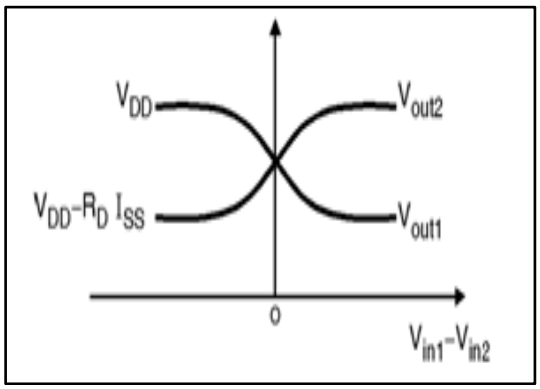


Figure6. Input-output characteristics of a differential amplifier

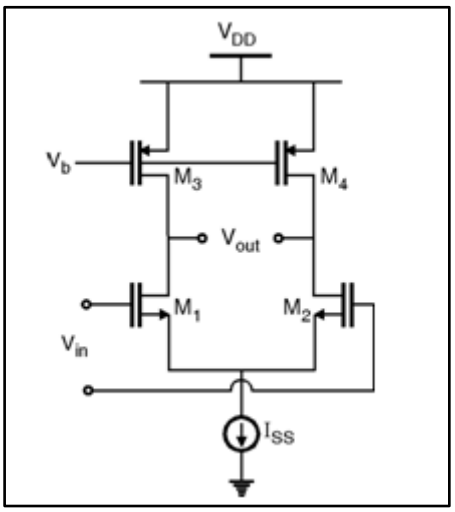


Figure7. Differential amplifier with current source load

Figure7 demonstrates an active load MOSFET differential amplifier. M_1 and M_2 form a DA pair, while M_5 is a sinking current that provides bias to the amplifier. M_3 and M_4 form a current mirror. As all transistors are considered in the saturation region, and as the bulk of all transistor connected to their respective sources, the current that flows from M_5 separated into two equal parts flowing through M_1, M_3, M_2, and M_4 respectively. Given this, transistors M_3 and $M_4$are linked to the V_{DD} supply while M_5 is connected to V_{SS}.

DA with Passive Load

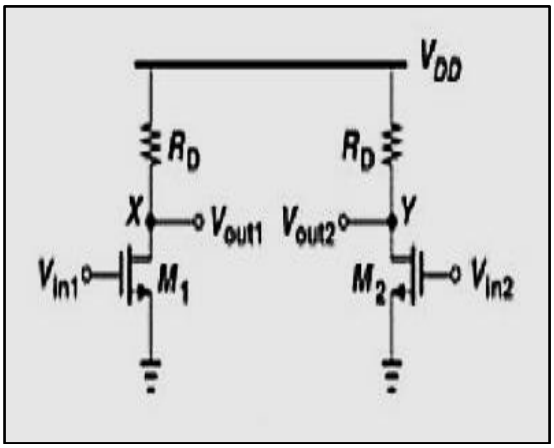


Figure8. Basic Differential Amplifier with a passive load

Figure5 is designed by using two n-channel MOSFETs (M_1 and M_2) to form a differential pair. R_D resistors are used as a load to drive the transistors into saturation. V_{in1} and V_{in2} are induced at the gate terminal of the MOS transistors, wherein they are opposite in phase and equal in magnitude. Nodes X and Y are where the output voltage is measured and in between these nodes, the differential signal which has similar magnitude and opposite phase to the inputs is measured. Its primary advantage is greater output voltage swing.

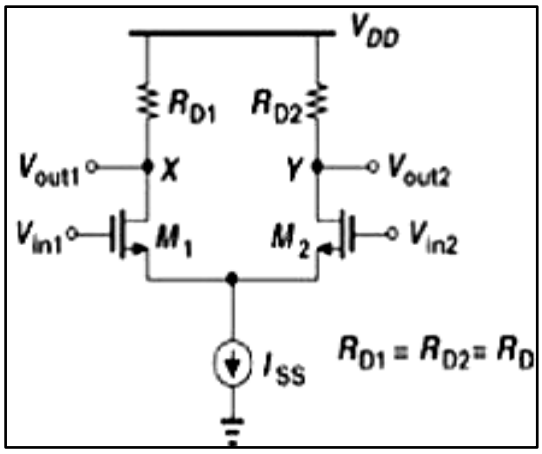


Figure9. Differential Amplifier with Passive Load and Current Source

Biasing problems are solved using the constant current source, which is presented as I_{ss}in the circuit. Figure9 shows constant current source used to maintain the minimum bias current to avoid the impacts of common mode level changes at the output. A transistor replaces the ideal current source in this circuit the deliver constant voltage source while operated in the saturation region. This acts as a constant current source.

1.2 DA with Active Load

The circuit shown below uses different load through active components like a currentsource load. It helps if a diode is connected to overcome the problem of decreasing the voltage swing and its effect on gain because of the common mode. We used PMOS transistors as a load to select proper dimensions and bias current. In achieving high gain, W/L of PMOS should decrease.

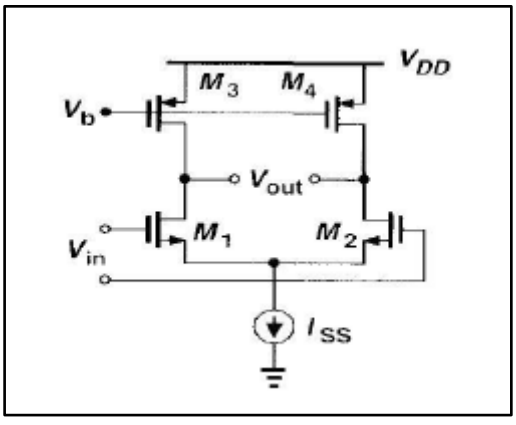


Figure9. DA with active load

1.3 NMOS

Biased with a positive gate to the source voltage V_{gs}=1.8V, anddrain to the source voltage V_{ds}=1.5V, the NMOS transistor body is linked to a source. The result between I_d and V_{ds} shows its I-V characteristics. When there is a gate to source positive voltage, the current I_d only flows when the $V_{gs}$is higher than the threshold voltage. The simulation of NMOS transistor is determined using the BSIM-3 model while all parameter values are sourced from the TSMC model file with 0.18µm technology. NMOS length is considered 1µm and 10µm for width. And then the threshold voltage βis determined and is used in further calculations.

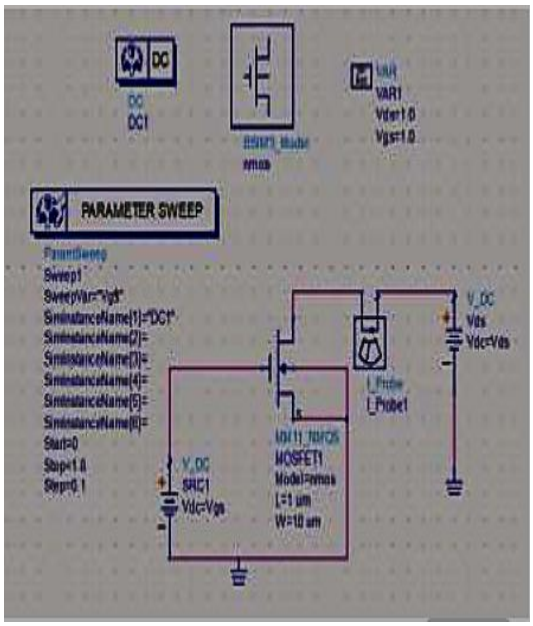


Figure10. NMOS Design

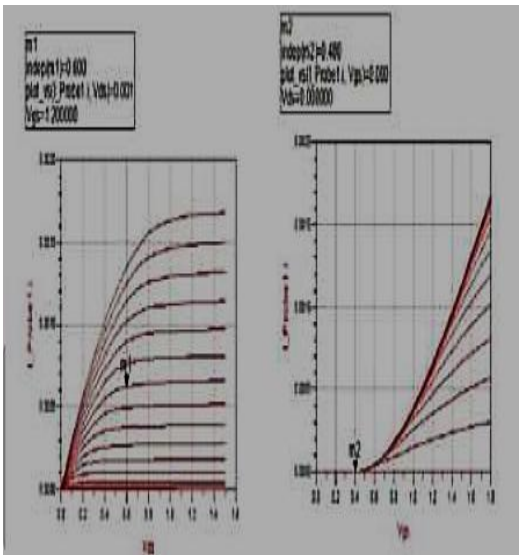


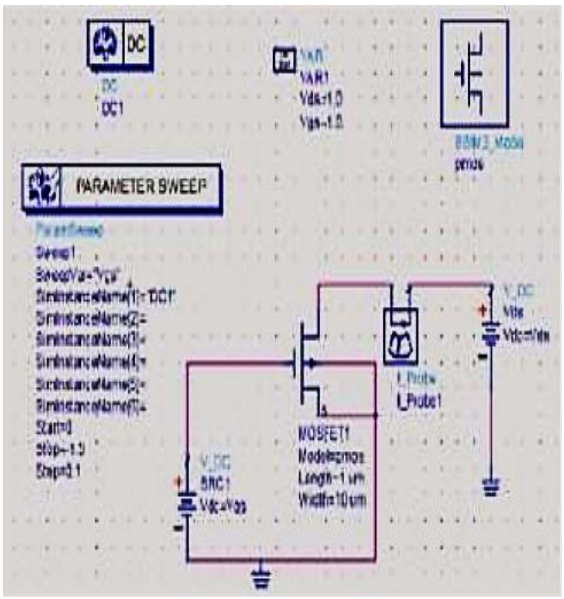
Figure11. NMOS Simulation

Figure11 shows that when the positive gate voltage is applied to NMOS with Vgs=0, the current I_d does not exist even though there were some positive Vds applied. To attain a significant amount of I_d, a sufficiently high positive gate Vgs must be applied. The minimum gate to source

voltage that produces the N-type inversion layer draining the current flow becomes a threshold voltage when V_{gs} is equal to V_t. When V_{gs} is less than V_t, the I_d=0. The I_d only starts when V_{gs}>V_t. In certain V_{ds}, virtual channel deepens and I_d increasesasV_{gs} is increased.

1.4 PMOS

Biased with a negative gate to the source voltage Vgs=1.8V, and drain to the source Voltage Vds= -1.5V, the PMOS transistor body is linked to a source. The I-V characteristics demonstrate the result between Id and Vds of different values of Vgs and another graph of Id and Vgs. When there is a gate to source negative voltage, the current I_d only flows when the $V_{gs}$is higher than the threshold voltage. The simulation of PMOS transistor is determined using the BSIM-3 model while all parameter values are sourced from the TSMC model file with 0.18 μmtechnology. PMOS length is considered 1μm and 10μm for width. And then the threshold voltage β is determined and is used in further calculations.



F**igure12**. PMOS Design

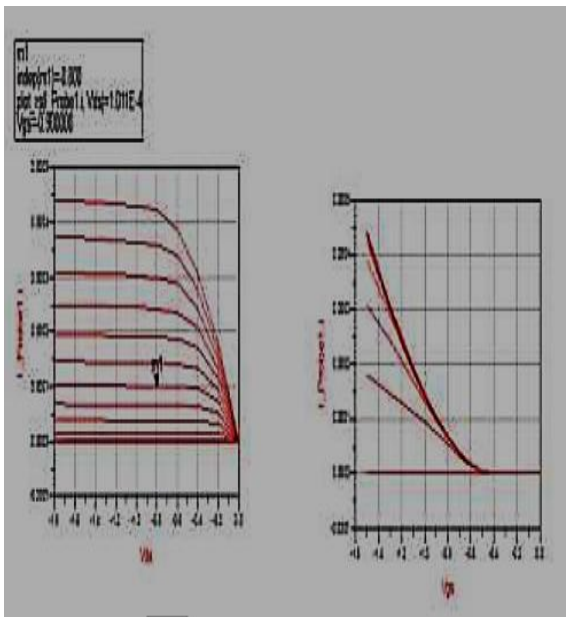


Figure13. PMOS Simulation

Figure13 shows that when the negative gate voltage is applied to NMOS with Vgs=0, the current I_d does not exist even though there were some negativeV_{ds} applied. To attain a significant amount of $I_{d,}$ a sufficiently high negative gate V_{gs} must be applied. The minimum gate to source voltage that produces the P-type inversion layer draining the current flow becomes a threshold voltage when V_{gs} is equal to V_t. When V_{gs} is less than V_t, the I_d=0. The I_d only starts when V_{gs}>V_t. In certain V_{ds}, virtual channel deepens and I_d increasesasV_{gs} is increased.

1.5 Differential Amplifier Design

The DA design comprises NMOS and PMOS transistors. NMOS current mirror is usedIn providing a stable current to the differential amplifier, wherein all the body of the transistor are connected to the source of respective transistors. The V_{DD} supply voltage is 1.8V. The input terminals V_{in1} and V_{in2} connect to a sine wave having 0.8V $V_{dc,}$ an amplitude of 1mv and V_{dc} 0.5V with 180 phase shift respectively. From the Vout terminal where the 10pf load is linked. Here, BSIM3, NMOS, and PMOS model are used to simulate a differential amplifier. As we consider al MOS in the saturation region, the transient analysis and simulation demonstrate V_{out}over Time. The calculation of gain AC analysis is also presented.

We assume that the slew rate is 10v/μsec, we can determine the current flowing through the transistor from this slew rate and capacitance.

Slew Rate = (dv/dt) = I/CL

Equation 1

Considering ICMR+ = 1.6V and ICMR-= -1.6V, we now determine the W/L for both M_3 and M_4.

Since M_1 and M_2 are in the saturation region, we use this equation:
$V_{ds}>V_{gs}-V_t$, where $V_t = 0.4V$.
Thus, in saturation region, the equations for current are:

$$I_{ds} = \frac{\beta}{2(V_d-V_s)^2}$$

Equation 2

$$I_{ds} = \frac{\mu C_{oxw}}{2L(V_d-V_s)^2}$$

Equation 3

The transconductance is,

$$gm = \frac{\partial Ids}{\partial Vgs}$$

Equation 4

$$\text{Gain BW} = \frac{gm}{2\pi fC_l}$$

Equation 5

$$W/L = gm^2/2I_{ds}\mu C_{oxw}$$

Equation 6

To calculate M_3 and M_4 W/L ratio, equations 1 and two will be used.

To calculate M_1 and M_2 W/L ration, equations 3,4,5,6 will be used.

To calculate M_5 and M_6 W/L ratio, equation three will be used.

Given that I_{ds} = 100 µA, V_{DD} = 1.8V, Gain BW = 4Mhz.

$W/L_{(1,2)} = 4$

$W/L_{(3,4)} = 28$

$W/L_{(5,6)} = 5$

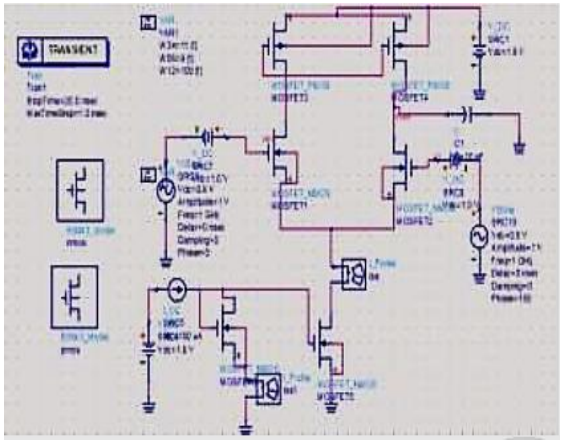


Figure13. Transient Analysis

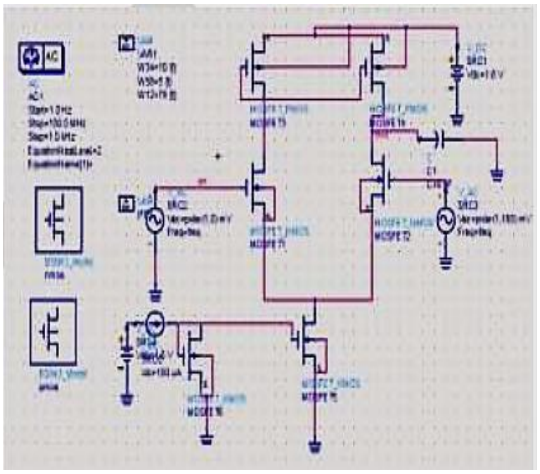


Figure14. AC Analysis

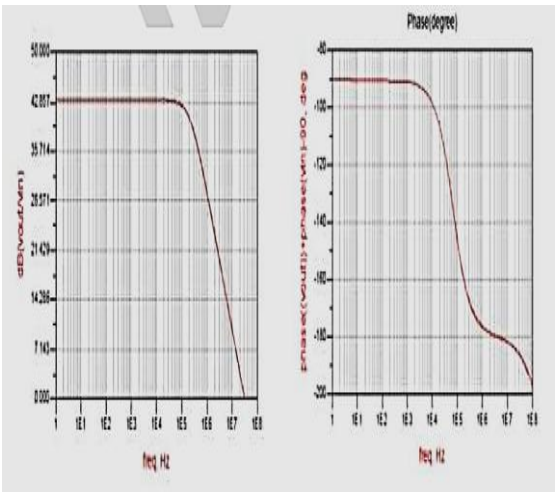


Figure15. AC Analysis Simulation

IV. RECOMMENDATIONS

The primary function of a differential amplifier is to amplify the input signal, precisely the difference between the two input voltages. You will need active elements (components) to amplify an input signal such as bipolar or unipolar transistors like MOSFETs, FETs, and BJTs. With

only passive elements, a differential amplifier cannot be made.Active elements are needed. Specific circuits can be used for differential amplifiers. However, it offers a wide array of responses.

Ideally, differential amplifiers should have infinite gain and impedance with zero output impedance; while all the frequencies are arithmetically perfect, which is in so many ways beyond passives. In constructing discrete elements, commonly, a functional and fair device could be simple: at least two transistors and a push-pull driver with two or more transistors, with some few passives. MOSFETs are great for the drive because its impedance is high with currently produced near zero.

V. CONCLUSION

A differential amplifier is designed to amplify two input signals and determines its difference.To achieve this, a design is needed. This paper uses an active load to analyze the model. NMOS and PMOS were used, and Advance Design System presents its simulations. Similarly, the amplifier design is also shown by ADS. The circuit specifications are designed for applications of operational amplifiers, and the W/L ratios are determined. Furthermore, the accuracy of the results is enhanced by the ADS.

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