Shreedhar A Joshi, et. al. International Journal of Engineering Research and Applications
www.ijera.com
ISSN: 2248-9622, Vol. 14, Issue 5, May, 2024, pp: 33-40

RESEARCH ARTICLE OPEN ACCESS

Low Power Design Techniques for 6T SRAM Cell in 45nm Technology Node: A Comparative Analysis

Shreedhar A Joshi*, Ankit Gumaste**, Prajwal H N***
**(Department of Electronics and Communication, SDM College of Engineering & Technology, Dharwad)*
***(Department of Electronics and Communication, SDM College of Engineering & Technology, Dharwad)*
****(Department of Electronics and Communication, SDM College of Engineering & Technology, Dharwad)*

ABSTRACT
Efficient power management is a critical aspect of chip design. Low Power Static Random Access Memory (SRAM) cells have become a focal point in modern semiconductor memory design, driven by the increasing demand for energy-efficient electronic devices. This paper investigates various methods to optimize power consumption of a 6T SRAM Cell, which is a significant component of chip architecture. Various low power techniques like Sleep Transistors, Transistor Stacking, Forced Stack are analyzed for their effectiveness in power reduction. Analysis was performed at 45nm technology node using Cadence Virtuoso to evaluate these techniques comprehensively. Results reveal that MTCMOS exhibits superior power-saving capabilities, followed by Gated VDD, reducing power from the order of microwatts to the order of picowatts. These findings provide valuable insights for chip designers aiming to enhance efficiency and minimize power consumption in SRAM designs. By implementing these findings, future computer chips can achieve reduced power consumption, contributing to advancements in energy-efficient chips.

Keywords – Stacking, Leakage Current, Sleep Transistor, SRAM Cell, Threshold Voltage

---

Date of Submission: 22-04-2024 Date of acceptance: 02-05-2024

I. INTRODUCTION

In recent years, the realm of Very Large Scale Integration (VLSI) design has witnessed a remarkable transformation characterized by the miniaturization of device geometries, scaling down to deep submicron levels resulting in increased density of transistors within Integrated Circuits (IC) and increased leakage current is becoming a major source of power consumption. This evolution has given rise to circuits of unprecedented complexity and frequency, accompanied by a substantial increase in power consumption and heat generation [1]. The consequences of excessive power dissipation are multifaceted, ranging from heightened vulnerability to runtime failures to significant reliability issues, exacerbated by the elevated temperatures associated with high-power processors. Every 10°C increase in operating temperature approximately doubles a component's failure rate. Increasingly expensive packaging and cooling strategies are required as chip power increases. Due to these concerns, circuit designers are realizing the importance of limiting power consumption and improving energy efficiency at all levels of the design.

In the era of rapid development and usage of portable devices, battery life is a major concern. As new devices are developed like smartwatches, small sensor nodes, wireless communication units, etc, energy-efficient hardware architecture is required [2]. Memory circuits form an integral part of every system design as more than half of the transistors in modern-day high-performance microprocessors are devoted to just cache memories itself [3] and this is expected to increase further in the upcoming years. Recently presented studies on reduced-power processors show that 43% and 50.3% respectively of the total system power consumption is attributed to memory circuits. Random Access Memory (RAM) like Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) are used in every digital system and significantly contribute to system-level power consumption. SRAM cells don’t require constant refreshing to retain the data stored as long as power is supplied to the cell.

Conventional SRAM Cell designs are power hungry and poor performers in this new era of fast mobile computing and wireless communication [4]. So, energy-efficient SRAM cells will have a positive impact on the overall system by significantly improving the system power-efficiency, performance, and reliability. Furthermore, as most of the transistors on a chip sit in the SRAM unit, and since memory uses an array architecture, power reduction in a single SRAM cell can contribute to huge power savings in the overall system.

In this paper, we analyze low-power design methodologies, with a specific focus on power reduction of the Conventional 6T SRAM Cell.

II. LITERATURE SURVEY

Reference [1] discusses power gating technique (Sleep Transistor Approach) for power reduction. Leakage power is measured by simulating a 1 kb SRAM Array. The leakage power of 10T SRAM cell (Sleepy) and 6T SRAM cell obtained are 19.36 mW and 36.52 mW respectively.

Reference [2] discusses two power reduction techniques for SRAM cells namely Gated VDD and MTCMOS in 90nm technology. MTCMOS based SRAM cell achieves 38.1% power savings while the Gated VDD SRAM cell achieves 16.8% power savings when compared with the Conventional 6T SRAM cell.

Reference [9] gives a brief review of different steps taken for the reduction of leakage power in VLSI design. It explains how power reduction is achieved in techniques like sleepy stack, forced stack and sleep transistors.

Reference [10] shows that, 6T SRAM cells with sleep transistor during sleep mode leads to 91.6% reduction in Static Power dissipation, and in active mode leads to 32.25% less power consumption than conventional 6T SRAM cell.

III. METHODOLOGY

3.1 Conventional 6T SRAM Cell

The conventional 6T SRAM cell consists of two cross-coupled inverters and two access transistors [2] as shown in Fig. 1. The cross coupled inverters act as a single bit data storage element and reinforce the data bit within the cell as long as the power is supplied (VDD). Access transistors (or pass transistors) are used to access this data storage element. Word Line (WL) is used to turn the access transistors on or off. Bit Lines (BL and BL_Bar) are used to write the data into the cell or read the data stored in the cell.

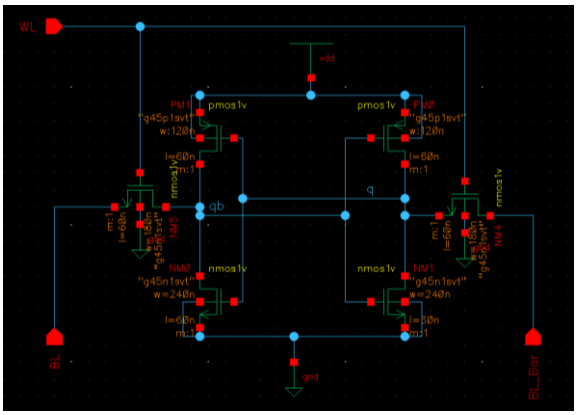

Fig. 1. Conventional 6T SRAM Cell

When the Word Line (WL) is at logic ‘0’, the access transistors disconnect the cell from the Bit Lines. The two cross coupled inverters in the cell continue to hold the data bit present in the cell as long as power is supplied (VDD). This mode of operation is known as Standby or Hold mode.

For a write operation, WL is set to logic ‘1’, turning on the access transistors. The contents from the Bit Lines are then transferred into the cell via the access transistors. After a successful write operation, the access transistors are turned off by setting WL to logic ‘0’.

For reading the data bit present in the cell, Bit Lines are initially pre-charged to VDD (logic ‘1’). The WL is then set to logic ‘1’. Depending on the data bit stored in the cell, one of the bit lines gets discharged slightly via an access transistor and pull-down transistor thereby developing a differential voltage drop between the Bit Lines. This small differential voltage drop is then detected by a Sense Amplifier which determines the data bit stored in the cell.

3.2 Power Dissipation

In SRAM, power dissipation refers to the energy consumed by the memory cells and

associated circuitry during operation. There are primarily two types of power dissipations in SRAM, namely Static Power Dissipation and Dynamic Power Dissipation.

3.2.1 Static Power Dissipation

Static power dissipation occurs when the SRAM is in steady state, i.e. when not performing any read or write operations. It is primarily due to leakage currents like gate leakage, sub-threshold leakage, junction leakage, etc. The leakage power becomes more significant in lower technology nodes due to the reduced distance between source and drain and increase in transistor density.

3.2.2 Dynamic Power Dissipation

Dynamic power dissipation occurs due to switching activity, i.e. when the SRAM cell is actively performing read or write operations. It is primarily due to charging and discharging of capacitances within the memory cells during read and write operations. Dynamic power dissipation mainly consists of switching power dissipation and short circuit power. Dynamic power dissipation increases with frequency and with the number of memory accesses.

3.3 Power Reduction Techniques

Power can be reduced by implementing Low Power Circuit Design Techniques, Voltage Scaling, and Clock Management.

Low Power Design techniques include utilizing low threshold voltage transistors to reduce leakage currents, employing power gating techniques to cut off power to inactive blocks when they are not in use. Voltage Scaling refers to lowering the supply voltage to reduce both static and dynamic power dissipation. Clock Management refers to reducing clock frequencies wherever possible to decrease dynamic power consumption.

By combining these techniques, designers can effectively reduce power dissipation in SRAM, making it more energy-efficient for various applications.

3.3.1 Gated VDD

This technique introduces a sleep transistor. A sleep transistor acts as a switch to disconnect the power supply from SRAM cell when not in use (Standby or Hold mode). When the sleep transistor is turned off, it acts as an open circuit between the power supply and SRAM cell and also serves as stacking transistor thereby reducing leakage current, and consequently reducing the leakage power dissipation [2] [5].

The sleep transistor is a high threshold voltage (High Vt) transistor introduced either in the supply path (pull-up path) or the ground path (pull-down path) of the SRAM cell. Control signal is used to turn on or turn off the high Vt transistor.

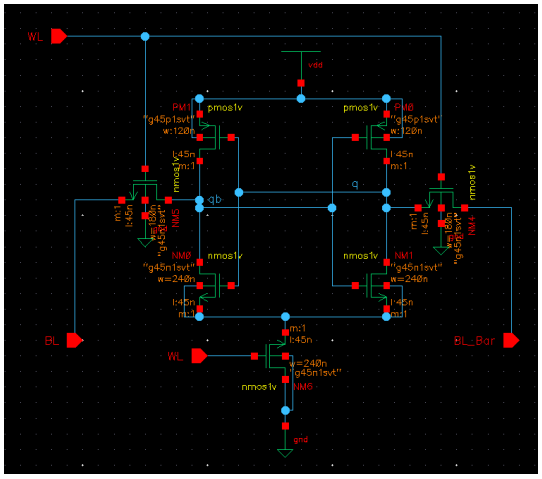

Fig. 2. Gated VDD with Sleep Transistor in the Ground Path

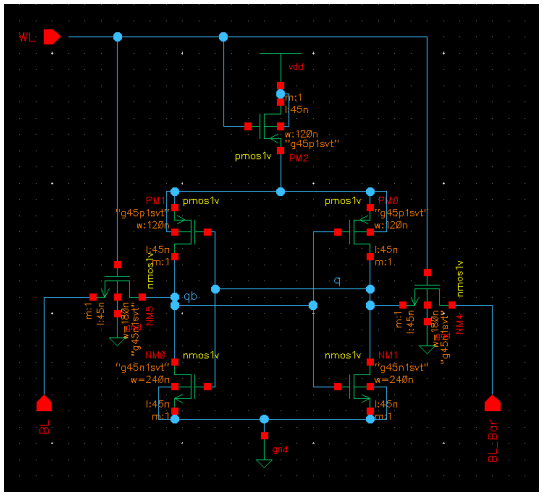

Fig. 3. Gated VDD with Sleep Transistor in the Supply Path

Fig. 2 shows Gated VDD SRAM cell design with sleep transistor in the ground path, and Fig. 3 shows Gated VDD SRAM cell design with sleep transistor in the supply path.

3.3.2 MTCMOS

This technique introduces sleep transistors in both the supply path (pull-up path) and the ground path (pull-down path). Sleep transistors are turned on in active mode and off in standby mode (hold or sleep mode) by the control signal [2] [5] [6].

Transistors with multiple threshold voltages are used to optimize both delay and power, hence the name MTCMOS. Low threshold transistors switch faster but have higher static power leakage. On the other hand, high threshold transistors reduce static power leakage but switch slower. Hence, the sleep transistors are modelled as high threshold transistors to reduce leakage current whereas the transistors in the SRAM cell are critical path transistors which are required to switch fast are modeled as low threshold transistors to minimize the delay.

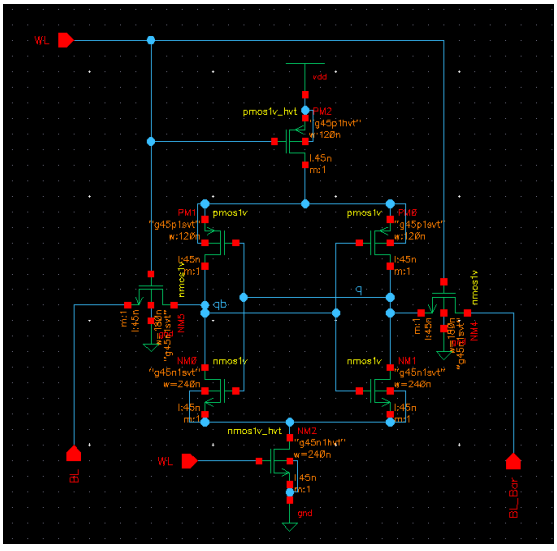

Fig. 4. MTCMOS with Standard Threshold Voltage SRAM Cell

Fig. 4 shows an MTCMOS implementation with high threshold sleep transistors, and transistors in the SRAM cell modeled as standard threshold voltage transistors. This configuration results in more power reduction but higher delay. Whereas Fig. 5 shows an MTCMOS implementation with high threshold sleep transistors, and transistors in the SRAM cell modeled as low threshold voltage transistors resulting in slightly increased power consumption but lesser delay.

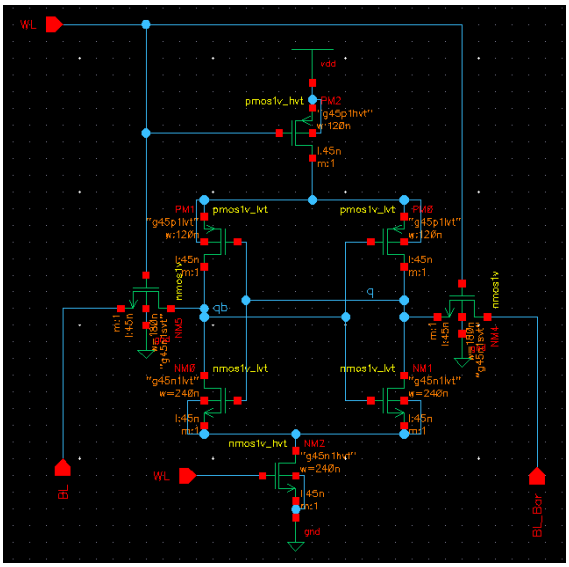

Fig. 5. MTCMOS with Low Threshold Voltage SRAM Cell

3.3.3 Dual Threshold CMOS (DTCMOS)

In this technique, transistors in the cross coupled inverter are modeled as high threshold voltage transistors to reduce leakage current in the steady state, and the access transistors are modeled as low threshold voltage transistors to provide faster access to the cross coupled inverter [7].

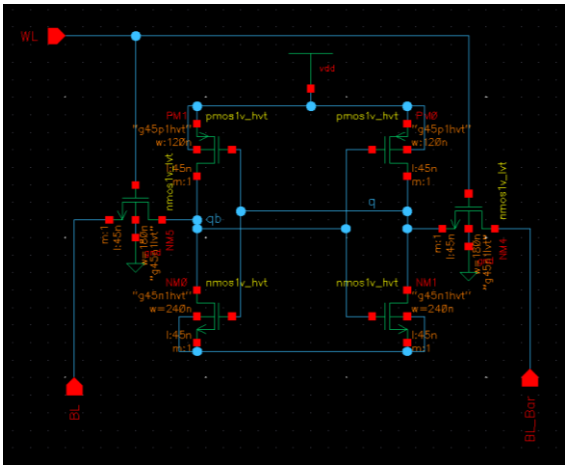

Fig. 6. DTCMOS Implementation

3.3.4 Dynamic Threshold MOSFET (DTMOS)

In this technique, the threshold voltage of the transistors (MOSFETs in this case) is altered dynamically to suit the operating state of the circuit.

A high threshold voltage in the standby mode gives low leakage current, while a low threshold voltage allows faster switching in the active mode of operation. Varying the threshold voltages dynamically can be achieved by connecting the gate and body terminals together, resulting in body effect [8]. This dynamically changes the threshold voltages of the transistors, which means if there is any change in the gate voltage, it will lead to change in the body voltage which further leads to a change in the threshold voltage.

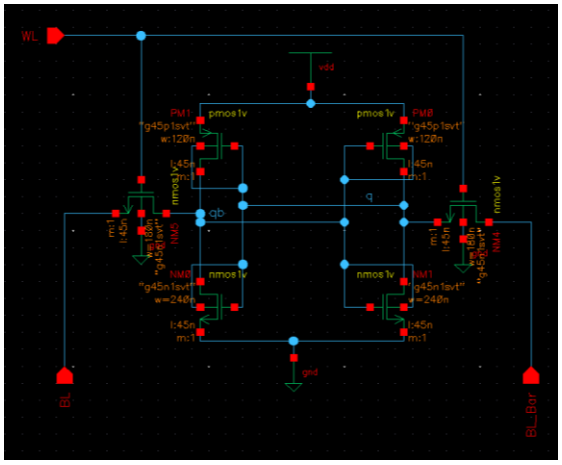

Fig. 7. DTMOS Implementation

The supply voltage of DTMOS is limited by the diode built-in potential in bulk silicon technology. The PN diode between source and body should be reverse biased. Hence, this technique is only suitable for ultralow voltage (0.6V and below) circuits in bulk CMOS.

3.3.5 Transistor Stacking

In this technique, two or more transistors are placed in series leading to variation in the threshold voltage due to the short channel effects resulting in significantly less leakage current. Leakage current flowing through a stack of series-connected transistors reduces when more than one transistor in the stack is turned off [8].

The stacking transistors provide the self-reverse biasing effect. Drain-to-source voltage decreases, leading to reduced DIBL current and the sub-threshold leakage current. Gate-to-source voltage is less than zero, thus decreasing sub-threshold current exponentially. Substrate-to-source voltage is negative, thus increasing the threshold voltage due to body effect, resulting in a decrease in sub-threshold leakage current.

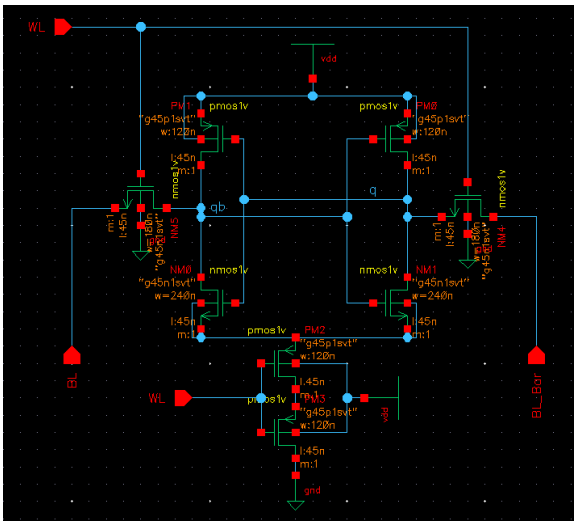

Fig. 8. Transistor Stacking Implementation

Leakage current in the stack is equal to the leakage current of the transistor in the stack with highest threshold voltage as transistor with highest Vt will correspond to the lowest leakage current and the same current flows through all the transistors in the stack because of series connection.

3.3.6 Forced Stack

In this technique, a duplicate transistor is used for every transistor in the network. Each transistor bears half the original transistor width.

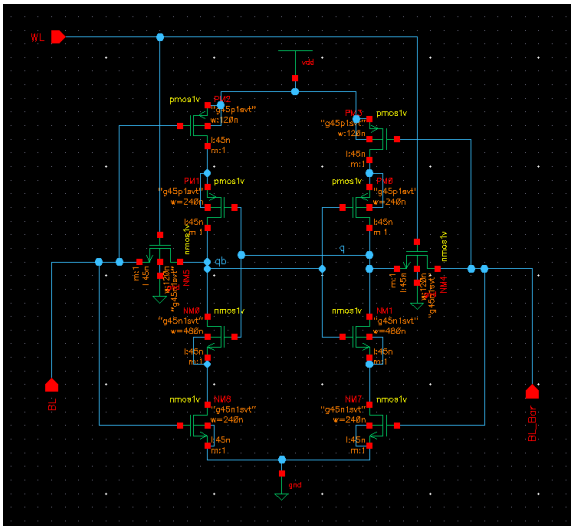

Fig. 9. Forced Stack Implementation

In the off state, the duplicate transistors produce a low reverse current from gate to source. Due to this reverse current overall leakage current reduces, thus reducing the leakage power consumption [9].

3.3.7 Sleepy Stack

Sleepy stack technique is the combination of sleep transistor and forced stack technique. This technique has lower leakage power dissipation, lesser delay, and is also capable of retaining the exact state. The sleep transistor in this technique works same as in the case of techniques that implement sleep transistors like Gated VDD and MTCMOS [9].

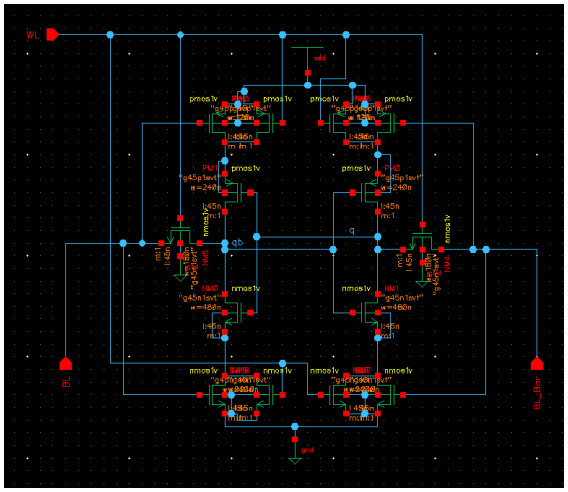

Fig. 10. Sleepy Stack Implementation

IV. RESULTS

The I-V characteristics graph was generated using Cadence Virtuoso, illustrating the relationship between voltage (V) and current (I). Subsequently, the total current across the range of voltages was calculated and averaged. Multiplying this average current by the supply voltage (VDD = 0.7 V) yielded the power dissipated by the circuit under consideration. Fig. 11 provides an illustrative example of the I-V characteristics curve for the Conventional 6T SRAM cell.

Among the power reduction techniques analyzed, MTCMOS emerged as the most promising followed by Gated VDD (PDN) in terms of power reduction, achieving a substantial reduction in power from the order of microwatts (uW) to the order of picowatts (pW). I-V Characteristics of 6T SRAM Cell with MTCMOS and Gated VDD are obtained as shown the Fig. 12 and Fig. 13 respectively. We can observe that the area under the curve is significantly smaller for both the MTCMOS and Gated VDD implementations when compared to the area under curve of the conventional 6T SRAM Cell.

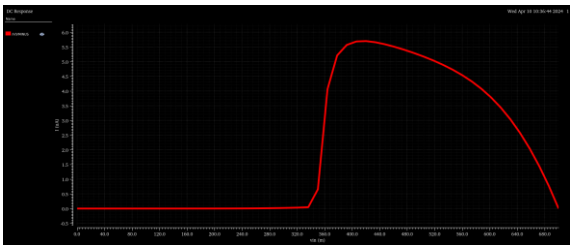

Fig. 11. I-V Characteristics of Conventional 6T SRAM Cell

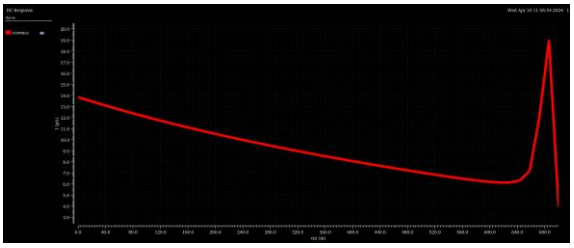

Fig. 12. I-V Characteristics of MTCMOS Implementation

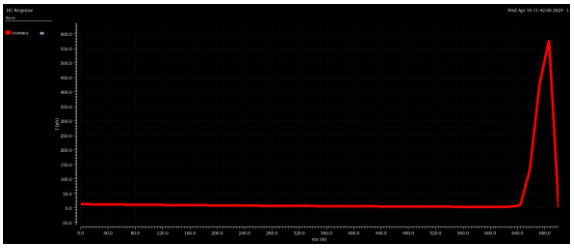

Fig. 13. I-V Characteristics of Gated VDD (PDN) Implementation

Additionally, other techniques such as Forced Stack, Sleepy Stack, DTCMOS, DTMOS, and Transistor Stacking exhibited varying degrees of power reduction in the order of nanowatts (nW). Fig. 14 to Fig. 18 illustrate the I-V characteristics of some of the other low power implementations.

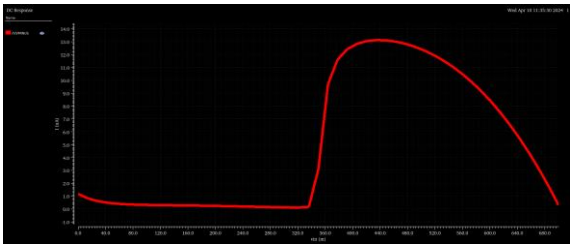

Fig. 14. I-V Characteristics of DTMOS Implementation

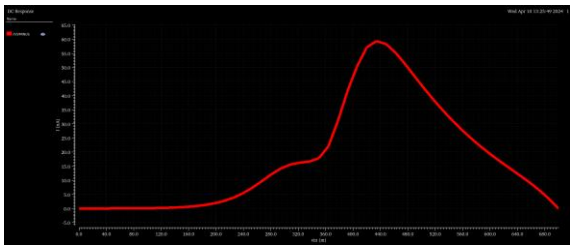

Fig. 15. I-V Characteristics of Forced Stack Implementation

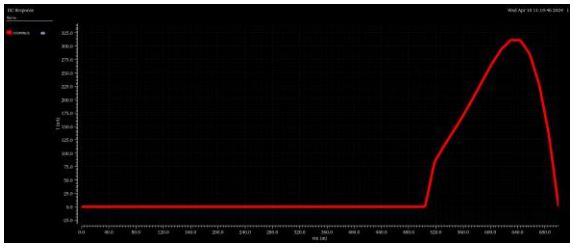

Fig. 16. I-V Characteristics of Transistor Stacking Implementation

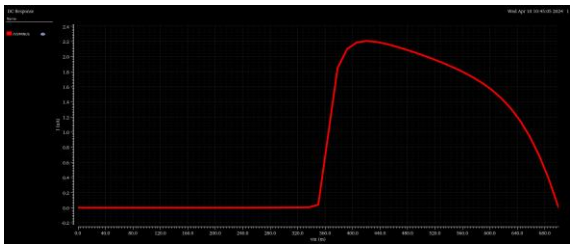

Fig. 17. I-V Characteristics of DTCMOS Implementation

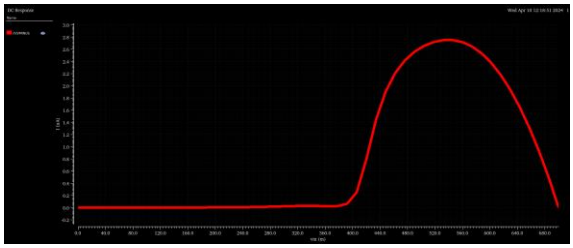

Fig. 18. I-V Characteristics of Sleepy Stack Implementation

Table 1. Comparison of Total Power

Sl. no	***Power Reduction Technique***	***Total Power***
1	Conventional 6T SRAM Cell	1.46 uW
2	MTCMOS (Standard Threshold Voltage SRAM Cell)	6.55 pW
3	Gated VDD (PDN)	20.82 pW
4	MTCMOS (Low Threshold Voltage SRAM Cell)	37.25 pW
5	DTMOS	3.478 nW
6	Forced Stack	12.61 nW
7	Transistor Stacking	38.79 nW
8	DTCMOS	566.0 nW
9	Sleepy Stack	580.1 nW
10	Gated VDD (PUN)	745.5 nW

V. CONCLUSION

In conclusion, the integration of various low-power techniques in 6T SRAM has proven highly effective in reducing power dissipation. Techniques such as MTCMOS and Gated VDD have demonstrated significant contributions to reducing overall power dissipation. The combinations of these techniques' present potential synergies, providing a comprehensive approach for further minimizing power consumption.

REFERENCES

[1] S. Khandelwala, S. Akasheb, and S. Sharmac, Reducing Leakage Power for SRAM Design Using Sleep Transistor, Proceedings of the 2nd International Congress APMAS2012, April 26-29, 2012.

[2] Akshay Bhaskar, Design and Analysis of Low Power SRAM Cells, International Conference on Innovations in Power and Advanced Computing Technologies [i-PACT], 2017.

[3] Jitendra Kumar Mishra, Harshit Srivastava, Prasanna Kumar Misra, Manish Goswami, A 40nm Low Power High Stable SRAM Cell using Separate Read Port and Sleep Transistor Methodology, IEEE International Symposium on Smart Electronic Systems (iSES), 2018.

[4] Deepak Mittal, V.K. Tomar, Implementation and analysis of Leakage Reduction Techniques in 6T SRAM cell, ICIIIE, IOP Conference Series: Materials Science and Engineering, October 8-12, 2023.

[5] Shreya R. Patel, K. R. Bhatt, Ms. Rachna Jani, Leakage current reduction techniques in SRAM, International Journal of Engineering Research & Technology (IJERT), ISSN: 2278-0181, Vol. 2 Issue 1, January-2013.

[6] Tripti Tripathi, Durg Singh Chauhan, and Sanjay Kumar Singh, A Novel Approach to Design SRAM Cells for Low Leakage and Improved Stability, Journal of Low Power Electronics and Applications, 8, 41, 2018.

[7] Chua-Chin Wang, Po-Ming Lee, and Kuo-Long Chen, An SRAM Design Using Dual Threshold Voltage Transistors and Low-

Power Quenchers, IEEE Journal of Solid - State Circuits, Volume. 38, No. 10, October 2003.

[8] Pavankumar Bikki, Pitchai Karuppanan, SRAM Cell Leakage Control Techniques for Ultra Low Power Application: A Survey, Circuits and Systems, 8, 23-52, 2017.

[9] Chetan, Prachi Chaudhary, Pawan Kumar Dahiya, Different leakage power reduction techniques in SRAM Circuits: A State-of-the-art Review, International Research Journal of Engineering and Technology (IRJET), Volume 04, Issue 07, July -2017.

[10] Kanika, Pawan Kumar Dahiya, Analyzing the Impact of Sleep Transistor on SRAM, IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), Volume 7, Issue 3, Version I, May – June, 2017.