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Implementation of Channel Coding Block for Uplink Base-Band Encoder

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ABSTRACT
The modern aspects of Information Technology (IT) community requires quick transmission speeds. Past generations of wireless mobile networks are manufactured in the sake of phone calls and slow data rate services. The transmission speeds are coping up with today's needs due to the 3rd generation (3G) technologies.
The processing system of an UMTS base station a test environment is used. The test environment is generating sampled antenna data in an offline fashion. The data provides information that is not dealt with all times and this creates unnecessary interference in the system. The memory has a limited amount so the data has to be repeated giving weak statistical confidence. Then, there is a need for a real _time system in order to generate long and unique test cases and decrease the interference.
The aim of this thesis is to systemize and implement a real-time channel encoding block for the baseband encoding for the uplink. The implementation is to be done on existing hardware. The work was divided into modules. These modules were first tested in MATLAB and then implemented on real hardware using SIMULINK block on FPGA. The design and implementation of real time encoder has been presented. The RSC encoder together with the interleaver and the turbo encoder have been designed and then real time implemented and evaluated.

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NR Non-Recursive Systematic Convolution
NSC Non-systematic convolution
RMTS Radio Telephone Mobile System
RSC Non- systematic Convolution
RSC Recursive Systematic Convolution
SIR signal – to – Interference Ratio
SMS Short Message Service
TACS Total Access Communication System
TDMA Time Division Multiple Access
UE User Equipment
UMTS Universal Mobile Telecommunication System
WCDMA Wideband Code Division Multiple Access

I. INTRODUCTION

1.1 Background

The twentieth century is said to be the century of revolutions. Science in every field expanded revolutionary. The most fascinating invention took placed in the field of communications. The analogue communication was the base and then the digital communication was the stem to the technology boom. The cellular communications was introduced by the Bell systems in late 1940s [1]. Before the cellular concept, the mobile communication was carried out through

List of Abbreviations
1G 1st Generation
2G 2nd Generation
3G 3rd Generation
3GPP 3rd generation partnership project
Amps Advance Mobile Phone System
BPSK Binary Phase Shift Keying
BTS Base Transceiver Station
CDMA Code Division Multiple Access
DSCDMA Direct Sequence Code Division Multiple Access
DSP Digital Signal Processing
ETACS Extended Total Access Communication
FDMA Frequency Division Multiple Access
FEC Forward Error Correction
FIR Finite Impulse Response
FPGA Field Programmable Gate Array
GSM Global Mobile System
HDL Hardware Description Language
IIR Infinite Impulse Response
JDC Japanese Digital Cellular
JTACS Japanese Total Access Communication
LSR Linear Shift Register
MTSO Mobile Telephone Switching Office
NMT Nordic Mobile Telephone

implemented on the FPGA using SIMULINK block set. These already built and tested recursive convolution codes the turbo encoder was tested in MATLAB and then implemented on FPGA.

To summarize the work, the ECB (error correcting block) of UMTS encoder using MATLAB and FPGA need to be implemented and evaluted.

1.3 Thesis Outline

- Chapter One provides background information .
- Chapter Two gives the details the background theory of basic concepts in mobile communication system and specifically on the uplink encoders used in this thesis.
- Chapter Three Presents the encoder design and implementation. The uses of MATLAB,SIMULINK, VHDL in the implementation were also presented.
- Chapter Four shows the system evaluation and the results. The results compares experimental with theory and simulation.
- Chapter Five gives the conclusions and the suggestion for future works.

II. ENCODER FOR MOBILE COMMUNICATION SYSTEMS

2.1 Introduction

In recent years research and development in the field of wireless communications technology has increased many folds. It has been a topic of study since 1960's but research activities in this topic have increased on a large scale for the past two decades. The ability to have an access to a communication system is vital and necessary for all kind of human activities. With the progress in communications technology and the rapid deployment of fast network infrastructure, multiple modes of communication are available to people located around the world. On the basis of structural organization the mobile communication networks can be divided into two groups; infrastructure based networks and infrastructure-less networks.

2.2 Infrastructure Based Networks

The most widely used network topologies in existing communication networks have a very well organized structure and follow strict guidelines for operations and management. A well known implementation is the cellular mobile phone network. In these networks, the base stations are an integral part of the entire network. The coverage of these types of network reaches about 95% of the urban population [5]. Cellular service is a ubiquitous method of providing wireless service to users. Infrastructure based cellular networks consist of a base station, a Mobile Telephone Switching Office broadcasting through a single power transmitter located at a high enough height and transmitting the signal to a large area. The Bell system model was based on many low power transmitters designed to offer services to a small area called a cell. With this concept, large city would be divided into many small cells each with a single low power transmitter.

The first generation was the age of analog cellular systems as many analog cellular systems were developed throughout the world, for instance, TACS (total Access Communication System), ETACS (extended Total Access Communication), and NMT (Nordic Mobile Telephone) 450, C-450, RMTS (Radio Telephone Mobile System) and Radicom 2000 in Europe, and JTACS (Japanese Total Access Communication System) in Japan. The corresponding analog system in USA was AMPS. Each of these systems was design to suit to the environment of the country in which it was developed and so a universal standard could not be achieved [2].

The problem of capacity appeared to cellular technology in 1990s when the cellular radio technology grew very rapidly. Enhancing the capacity of cellular systems by cell splitting might not solved the problems especially in congested and large cities where it is difficult and expensive to locate the case stations at the best sites. So other problems were also there hence to fix these problems efforts were carried out which gave birth to second generation digital cellular systems with GSM (Global Mobile System) in Europe IS-56 for North America, and JDC (Japanese Digital Cellular) in Japan [3].

As the needed change to fix the problems of second generation third generation and fourth generation cellular systems came into being. The second and third generation are suitable for voice communication but for burst data traffic to be required as a consequence of exponential growth for future challenges [4].

1.2 The Purpose of the Study

The purpose of the study is to systemize and implement a real-time channel encoding block for the baseband encoding for the uplink. The implementation is to be done on existing hardware. The work was divided into modules. These modules were first tested in MATLAB and then were implemented on real hardware using SIMULINK block on FPGA.

Since the real time implementation of a complete encoder is too complicated to be covered in the project, a real time implementation for the error correcting block of encoder side is only adopted in this study. The recursive convolution codes were firstly tested in MATLAB and then

other by accessing base stations and utilizing mobile switching office. In the absence of base station or a switching facility, the network fails to operate.

(MTSO), and communication devices as shown in Figure (2.1). We see that the communication devices such as mobile phones can communicate with each

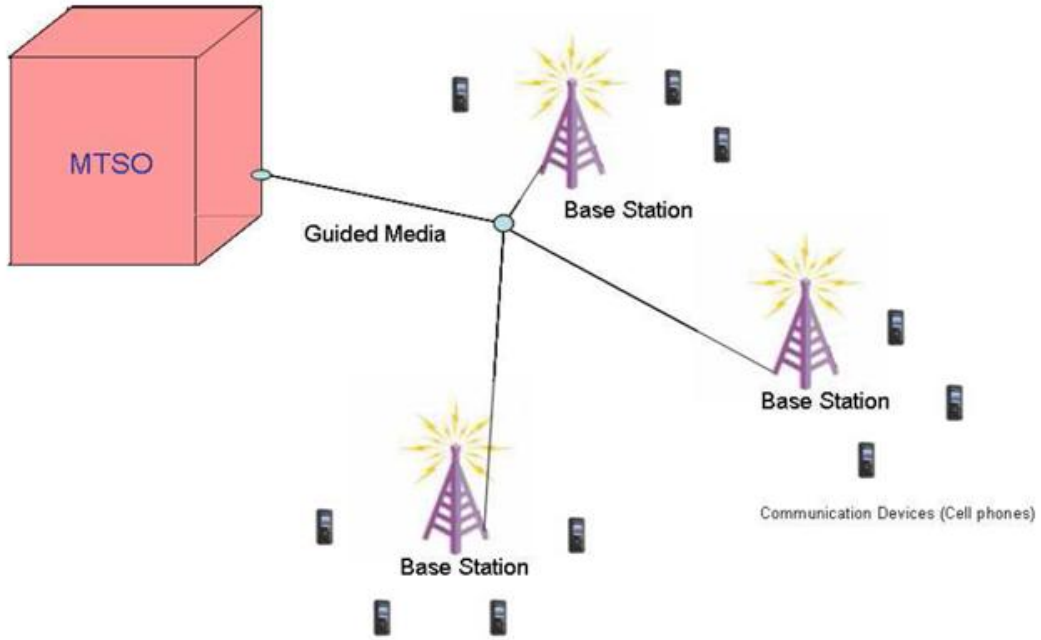

Figure 2.1: An Infrastructure based network.

devices are at the user side and exchange signal with cellular base station to send or receive data from other communication devices. These communication devices are typically mobile. The communication systems must have capability to manage the mobility and location updating of the nodes [6].

2.2.4 Cellular Networks

Traditionally the analogue or digital mobile communication systems rely on infrastructure based networks. A variety of communication standards are developed and used in different geographical regions over a period of time. First generation mobile communication standard was developed in early eighties. This mobile communication system is based on analog techniques in which Frequency Division Multiple Access (FDMA) technology is used. It is also referred as 1G mobile phones. Advanced Mobile Phone Systems (AMPS) is an example of first generation.

The second generation mobile phone standard was developed in early nineties. This mobile phone standard is based on digital technology. It is also referred as 2G mobile phones. Utilization of transmission resources in the second generation is more efficient than first generation. The new services introduced in second generation include Short Message Service (SMS), which initially became possible on GSM networks and

2.2.1 Cellular Base Stations

The base stations communicate with other base stations in addition to its local nodes in their range. The BTS transmits and receives signals for this purpose through antennas. The nodes are spread around base station randomly and may stay in the state of rest or motion. BTS plays a fundamental role in present age communication systems.

2.2.2 Mobile Telephone Switching Office (MTSO)

The mobile telephone switching office connects all of the individual cell towers to the Central Office (CO). It plays a basic role in the control operation of a cellular communication system. It consists of a highly efficient computer that monitors all cellular calls, tracks the location of all nodes, handles mobility of nodes and keep track of billing information etc. It monitors the quality of the communications signal and transfers the call to other base stations which are better suited to provide communication to the mobile device and controls call to and from other telephony systems.

2.2.3 Communication Devices

Communication devices consists of hand held phones, laptop computers, palm computers, notebook computers, car phones, and portable data collection devices. The most popular mobile units are the cellular telephones [5]. These communication

multimedia services that enhance the popularity of this generation. The third generation mobile phone uses a different range, in the radio frequency spectrum, to provide a wider range of services. The third generation can be used for the video conferences and calls, Internet access, high resolution camera links, music storage, and games [7]

eventually on all digital networks. GSM is the second generation and is still the most popular system for mobile communication.

The Third Generation (3G) mobile phones technology is an improved and more successful version of 2G mobile phones technology. The 3rd generation system represent a huge investment in technology. The main feature of the 3G mobile phones is consumer-driven access to mobile

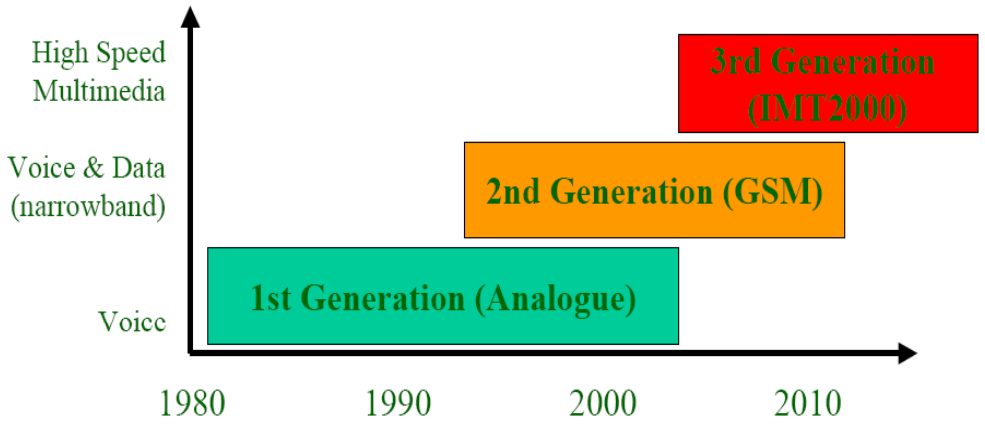

Figure 2.2 : Communication generation period

2.4 Uplink Baseband Encoder

2.4.1 UMTS

In 3G cell phones cell phone technologies we use UMTS. WCDMA is used as air interface and is standardized by the 3GPP in UMTS. Figure 2.3. The network supply switching, routing and transit for user traffic. UTRAN connects UE's to the CN and UE's are the mobile nodes. UMTS uses two 5 MHz wide physical channels, one for the uplink and one for the downlink. The carrier wave frequency for these channels differs between different countries and technologies, Figure 2.4.

The third generation brings together the two faster growing sectors, Mobile and Internet. Figure (2.1) shows the performance and evolution of different generation for mobile phone communications.

2.3 Infrastructure-less Networks

Networks without any infrastructure and central administration are referred as infrastructure-less networks. In these networks communication devices like mobile phone can directly communicate with each other. [8], wireless mesh networks are some examples of these networks. These networks are very attractive for communication in disaster areas, battle fields, and the area where deployment of network is not possible.

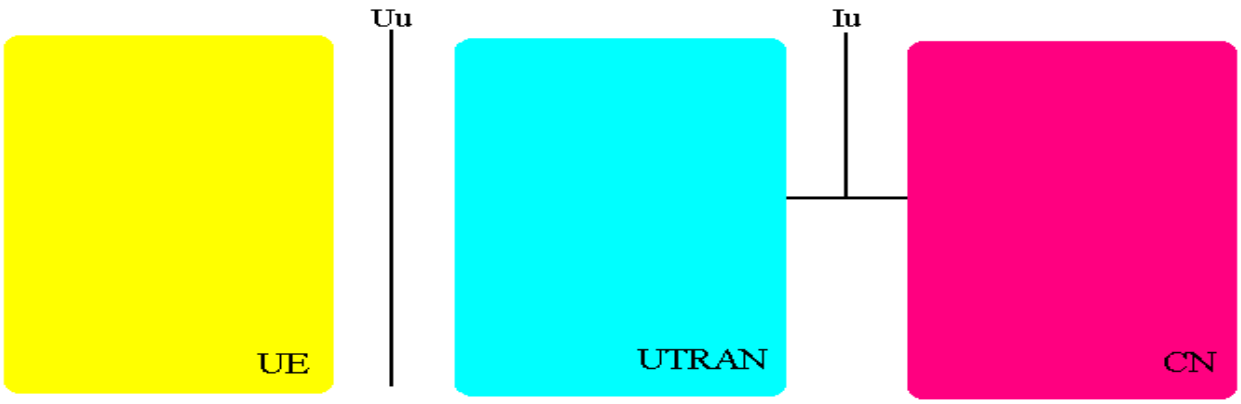

Figure 2.3: UMTS- Interacting domains

Release '99 of 3GPP theoretically supports transfer rates up to 14 Mbit/s, but in the network, a rate of 384 kbit/s on CS and 2 Mbit/s on PS connections can be expected. Newer releases have features such as High Speed Packet Access (HSPA). The transfer rates, its up to 7.2 Mbit/s for the downlink and 5.76 Mbit/s for the uplink.

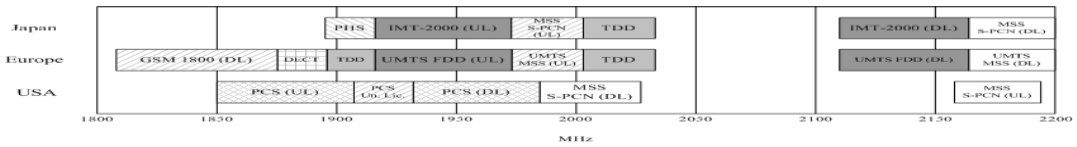

Figure 2.4: IMT-2000 spectrum allocations

2.4.2 WCDMA

WCDMA is the air interface for UMTS. It uses so called spreading codes.

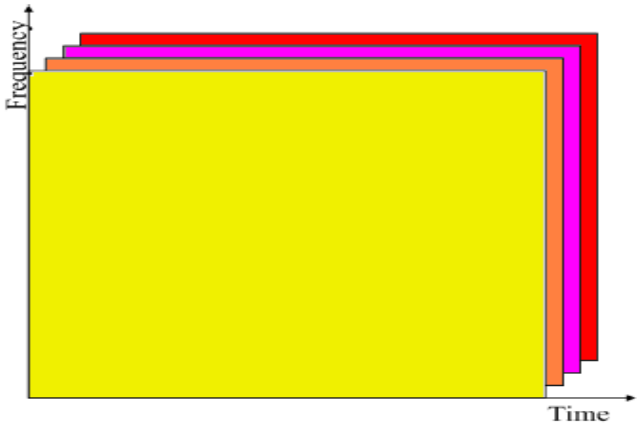

Figure 2.5: Air Interfaces (WCDMA)

In Figure 2.5 and Figure 2.6 WCDMA and TDMA can be seen respectively. It divides transmitters in time a slot while in Figure 2.7 FDMA is presented, which divides transmitters in frequency bands.

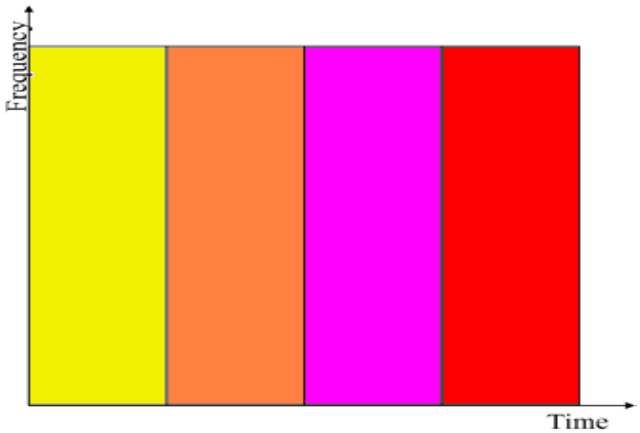

Figure 2.6: Air Interfaces (TDMA)

The WCDMA work properly if adaptive power control is used. This minimizes the interference in the system and is based on a Signal-to-Interference Ratio (SIR) value.

WCDMA is Code Division Multiple Access (DSCDMA) system. its means the transmitted bits are spread over a wider bandwidth than the actual data symbols. Spreading is done by multiplying the data symbols with quasi-random bits called chips. The chips are included in spreading codes that can be of different lengths.

The convolution codes are used as constituent codes in original turbo codes idea. In order to understand turbo codes, we present a detailed study of convolution codes. In this section, we discuss different aspects of convolution encoding. In the first part, we discuss its notations and construction, the second part deals with representation of convolution codes, the third part is concerned with the types of convolution codes, and in the last section free distance is discussed which is used as performance parameters for convolution code.

The structural representation is useful from implementation point of view. The code parameters of convolutional codes are usually given as C (n k [m]). In the code parameter, [m] means that encoder consists of a shift register of length m, n is the number of output symbols consisting of linear combination of memory contents of shift register with k input bits, as shown in Figure (2.9):

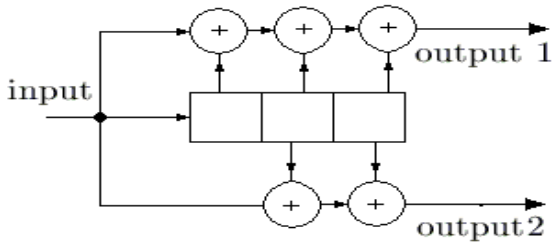

Figure 2.9: Structure of Convolutional Encoder, C (2 1 [3]) with constituent code (17, 13).

The convolutional codes can be categorized in four categories.

1. Systematic convolutional encoder.
2. Non-Systematic convolutional encoder.
3. Recursive convolutional encoder.
4. Non-recursive convolutional encoder.

Systematic Convolutional Encoder: If the convolutional encoder includes the input bit as one of its output, then this encoder is called systematic convolutional encoder. In systematic convolutional encoder, out of total n output bits, n-1 output bits are linear combination of input bit and memory elements and one bit is same as the input bit, in Figure (2.13) the systematic convolutional encoder is depicted.

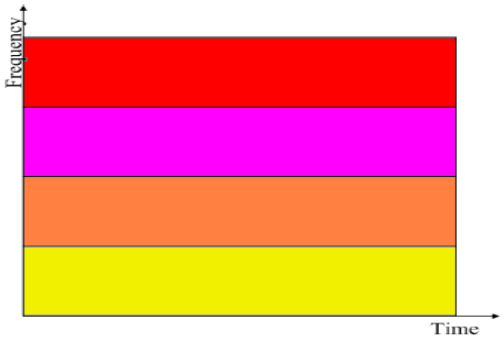

Figure 2.7: Air Interfaces (FDMA)

2.5 Forward Error Correction (FEC) Encoding in Uplink Encoder

The error correcting codes is used in Uplink to make the communication immune against noise. This thesis deals with this part hence the basics of FEC are added in this section. When the TBs have been segmented they are encoded with a channel coding. The channel coding is a FEC coding that is applied to enable the receiving side to correct errors. Two types of channel coding are used in UMTS, convolution coding and turbo coding. The two types are discussed below.

2.5.1. Convolution Codes

The convolution codes are based on linear mapping. Convolution encoder is based on passing the information through a linear-shift-register (LSR) as shown in Figure (2.8).

Figure (2.8), show they are not constituted .However, we can obtain a concrete mathematical description of mapping between information and codeword.

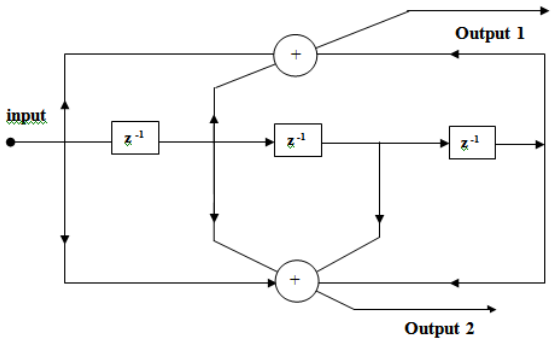

Figure 2.8: Structure of Convolutional Codes

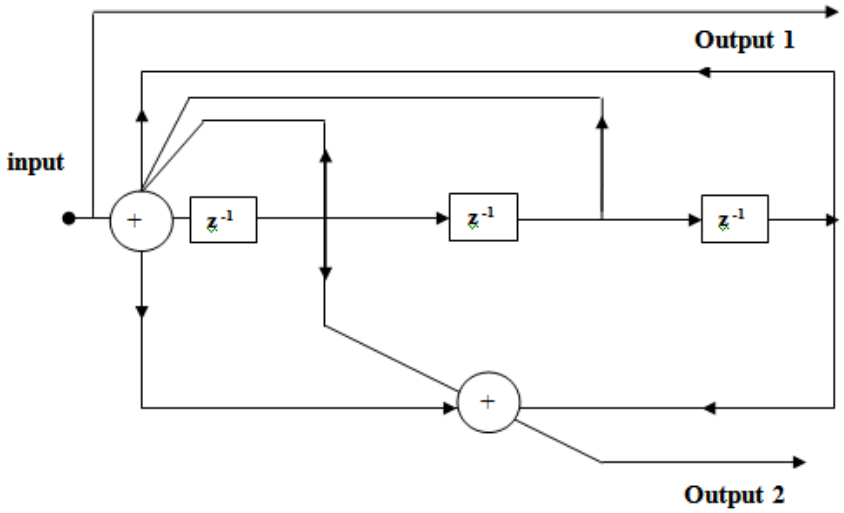

Figure 2.10 RSC Encoder

First we will study the structure of encoder and then the decoding method will be explained comprehensively.

Turbo codes are named Turbo because the decoder in this scheme works on the principle of iterative decoding, in which the decoders share the prior information in iterative way. Since we are concerned with the encoding side only hence we will study the encoding side only.

The conventional arrangement for the turbo encoder consists of parallel concatenated, two identically recursive systematic convolutional (RSC) encoders, which share data via an interleaver, as shown in Figure (2.14). The encoded data from the two encoders is punctured (optional) and multiplexed before sending on the channel. Hence the full turbo encoder includes a block for perforation and a multiplexer. The modified BCJR [9] algorithm is used for decoding, so the convolutional encoders are preferred for the encoding since they give a good approximation of Markov source [10]. There is no strict reason for using identical encoders; however, it is conventional to use the same transfer function for each encoder. Since RSC encoders and non-systematic convolutional (NSC) encoders have same free distance but RSC encoders are preferred over NSC encoders because the performance of RSC encoder is much better than that of an NSC encoder. A detailed comparison between the performance of RSC and NSC is given in literature; however, a quick analysis is also available in [9].

Non-Systematic Convolutional Encoder: If no input bit is present at the output, then this encoder is called non-systematic convolutional encoder. In this type of encoder all n output bits are linear combination of input bit and memory elements and no input bit is present at the output as it is. In Figure (2.10) a non-systematic convolutional encoder is depicted.

Recursive Convolutional Encoder: This type of convolutional encoder has a feedback. The feedback is carried out by adding one of output bit with input bit and then feeds the resultant bit to the Linear shift register (LSR) as shown in the Figure (2.13). This type of encoder has a rational system function or we can say it is an infinite impulse response (IIR) encoder. The recursive convolutional encoder is mostly used in systematic form, and named as a Recursive Systematic Convolutional (RSC) encoder.

Non-Recursive Convolution Encoder: This type of convolutional encoder has no feedback and is usually called feed-forward convolutional encoder. This type of encoder has an irrational system function or we can say it is a finite impulse response (FIR) encoder. The non-recursive convolutional encoder is mostly used in non-systematic form, and named as a Non-Recursive Systematic Convolutional (NRC) encoder.

2.5.2. Turbo Codes

As an information theorist Shannon told us what the best we can do but not how to do it(20). In 1993 turbo codes were introduced. In this section, we will discuss the turbo codes in detail.

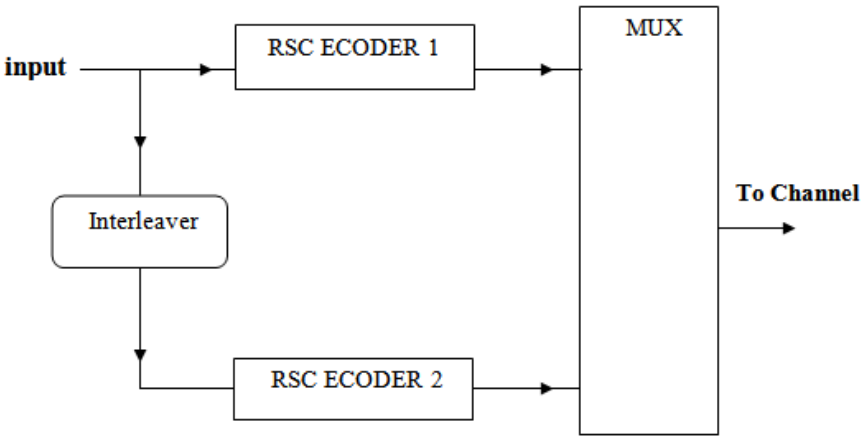

Figure 2.14: Block Diagram of a Turbo Encoder.

system before implementation. There are many tools available for modeling a system. An effective way of doing this is using a numerical computation and graphics program such as MATLAB. We also have used this tool for verification.

The way to approach the solution of our problem is to divide it in different parts. In the first stage the results were verified using MATLAB and in next stage they were implemented using SIMULINK tool.

3.2 MATLAB as Verification Tool

As mention above any communication system may be modeled using a MATLAB program. By the MATLAB program is easily plot both the time and frequency of a signal that are generated and then passed through the system in same tool and importantly we can verify our design.

The programming m-file editor in MATLAB enables us to make our desired signal or system. Once a system is designed then we can generate our desired signal using same editor and finally we pass the generated signals through the system and then based on results we analyze the system and verify our results.

3.3 SIMULINK as Implementation Tool

The communication circuits and subsystems are now available as merchant integrated circuits. Scientist in the modern telecommunication industry configures systems and builds them from subsystems and ICs. SIMULINK is popular software for developing using blocks that perform different operations.

Once the design is made using the blocks SIMULINK is so powerful that it can also implement the design on FPGA. After verification of system the design is modified in such a way that it is implemented with FPGA. Figure 3.1 shows system design and implementation stages.

A good question can be that how the rate of overall turbo encoders is influenced by the rate of elementary encoders. The answer to this question is given in the [10], if R1 is the rate of first encoder and R2 is the rate of second encoder, the overall rate R of the turbo encoder is given as shown in equation 2.6.

$$\frac{1}{R} = \frac{1}{R1} + \frac{1}{R2} - 1 \quad (2.6)$$

For better performance must be R1 ≤ R2. The parallel scheme allows the encoders and decoders to run on the same clock, which are not possible as in the case of serial concatenation.

Interleaving is used in digital data transmission technology to protect the transmission against burst errors. The most complex part of turbo encoder is interleaver because the mathematical aspects of interleaver is not trivial and the minimum free distance of turbo encoder is not fixed, chiefly, by the constituent RSC codes but by the interleaving function. In original turbo encoder a random interleaver was used.

The overall process of turbo encoder can be summarized as the information sequence with the tail bits added for trellis termination is fed to the first RSC encoder and at the same time the interleaved version of that sequence is fed to the second RSC encoder. The encoded bits generated from both the encoders are multiplexed and punctured (if required) and sent over the channel, and any scheme can be used for modulation such as BPSK (binary phase shift keying) etc.

III. SYSTEM DESIGN AND IMPLEMENTION

3.1 Introduction

In communications one of the most important concepts is modeling of communication

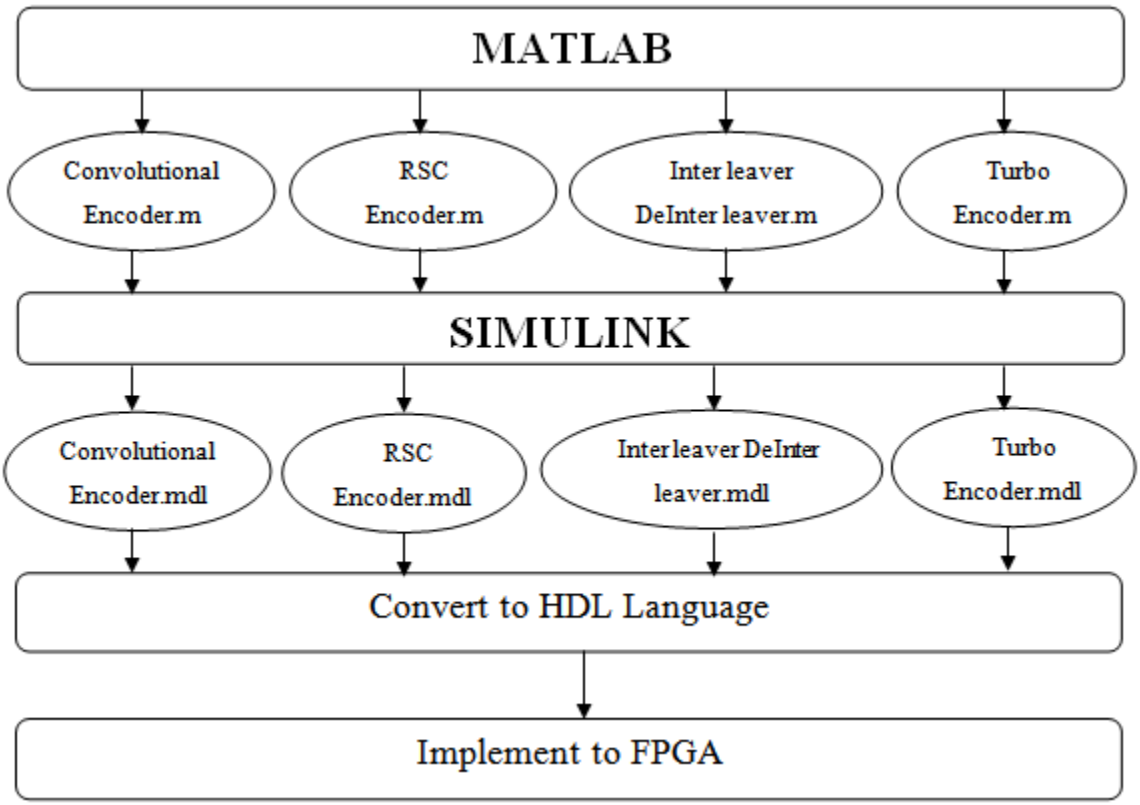

Figure 3.1 System Design and Implementation Chart

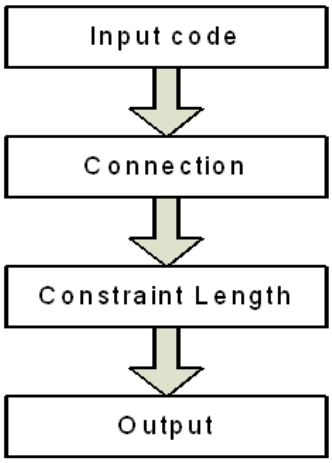

Figure 3.2 Flow Chart for Simple Convolutional Code Encoder in MATLAB

3.4.2 RSC Encoder in MATLAB

The second block designed was the recursive convolutional encoder. The design was named and rsc convolutional encoder since this type of convolutional code is also based on linear mapping of a set of information words to a set of codeword. The file simply accomplished the above mentioned procedure.

3.4 System Implementation Using the Matlab

The different parts of FEC block for Uplink encoder have been implemented using Matlab.

3.4.1 Simple Convolutional Encoder in MATLAB

The first block designed was a simple non recursive convolutional encoder. The design was named and simple convolutional encoder since the convolutional codes is based on linear mapping. It is based on transcendence the information to be encoded through a linear-shift-register (LSR). This file simply accomplished the above mentioned procedure.

The design made has an input vector contained two parameters, a set of variables which defined the structure of encoder and the vector to be encoded. The output of this file was the encoded version of data. It was verified that this structure encodes the data same as original real time encoder.

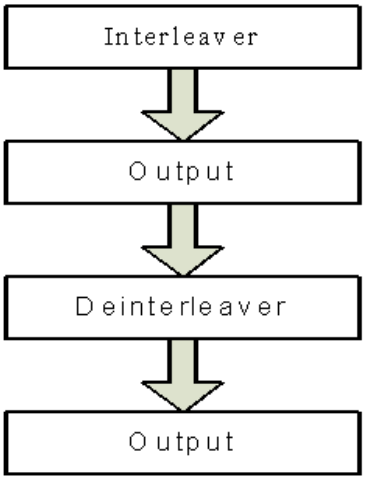

Figure 3.4 Flow Chart for Interleaver and Deinterleaver in MATLAB

3.4.5 Turbo Encoder in MATLAB

The fifth block designed in MATLAB was Turbo encoder. The design was named as turbo encoder. Since turbo encoder uses block interleaver and RSC encoders so this structure was a combination of previous built structures. The structure of two identical RSC encoders used in turbo codes along with the input vector is the input to this structure and encoded vector by turbo encoder is the output.

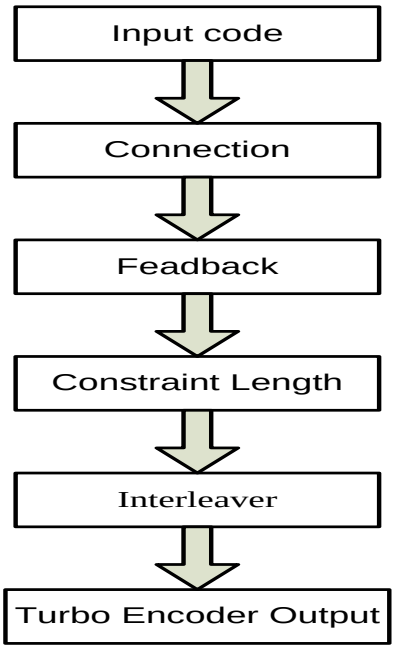

Figure 3.5 Flow Char for Turbo Encoder In MATLAB

3.5 SIMULINK

As an extension to MATLAB, SIMULINK adds many features specific to dynamic systems while retaining of MATLAB's general purpose functionality. SIMULINK represents dynamic

This design also has input vector which contained two parameters, a set of variables which defined the structure of encoder and the vector to be encoded. The output of this file was the encoded version of data. It was verified that this structure encodes the data same as original real time RSC encoder.

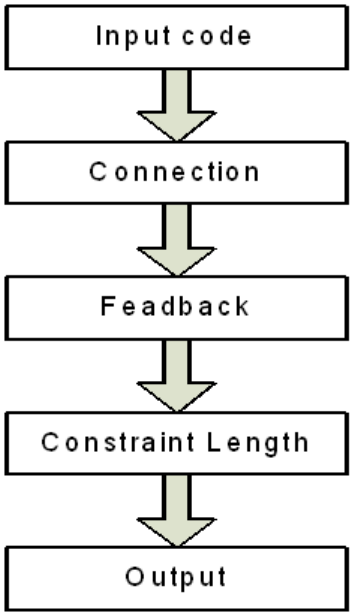

Figure 3.3 Flow Chart for RSC Encoder in MATLAB

3.4.3 Interleaver in MATLAB

The third block designed was the interleaver. The design was named as interleaver.m. Since there are two types of interleaver random and block interleaver, but the turbo encoder uses block interleaver so we also implemented the block interleaver. The design had a single input. The structure write the input in matrix row wise and then read it column wise in this manner interleaving was performed.

3.4.4 DeInterleaver in MATLAB

The fourth block designed was the Deinterleaver. The design was named as deinterleaver. The design had a single input. The structure produces the reverse result of interleaver.

the two RSC encoders separated by an interleaver was designed in SIMULINK.

3.6 HDL and FPGA Implementation

The FPGA configuration is generally specified using a hardware description language (HDL), to define the behavior of the FPGA; the user provides a hardware description language (HDL) or a schematic design. The HDL form is more suited to work with large structures because it's possible to just specify them numerically rather than having to draw every piece by hand. However, schematic entry can allow for easier visualization of a design. VHDL is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as FPGA(field-programmable gate arrays).

The scrambling is decided to be done on the FPGA, so a scrambling code generator and a scrambler will be implementing in VHDL and simulate in Modelsim. After creating the four functions in SIMULINk we can convert them to HDL language by following a certain step as I will describe in chapter 4.

IV. SYSTEM EVALUATION AND ASSESSMENTS

4.1 Introduction

The entire encoding scheme was first written in MATLAB. This was to get an understanding of how every step worked in detail. To use MATLAB was a given choice since it is designed to work with matrices which the baseband encoding mostly consists of. Since a lot of bit matrices are used in the encoding, MATLAB was a given choice. It also makes it simple to see the result of every step.

The baseband encoder is implemented using a MATLAB, a SIMULINK and a FPGA is the software used for testing of the different parts of encoder. I have created four functions in MATLAB that are converted to MDL. Then we convert the four functions in SIMULINK that are in MDL into HDL language.

4.2 MatLab Results and Data Analysis

The MATLAB was used for encoding and interleaving. The four function are created in MATLAB are:-

i. SIMPLECONVOLUTIONALENCODER.M
ii. RSCCONVOLUTIONALENCODER.M
iii. INTERLEAVER.M
iv. DEINTERLEAVER.M

systems with block diagrams, defining a system is much like drawing a block diagram.

After verifying the structure in the MATLAB the design were implemented using SIMULINK. The structures were first converted into block and then the data types and other interfacing parameters were adjusted. The four functions in SIMULINK is shown as in the following points.

3.5.1 Convolutional Encoder in SIMULINK

The Simulink model which I will use is the same as in the MATLAB function build for encoding an input through the convolutional code.

Iwill use the Trellis structure parameter field in two ways:-

1- If you have a variable in your MATLAB workspace that contains the trellis structure, enter its name as the trellis structure parameter. This method is preferable because Simulink takes less time to update the graph at the beginning of each simulation than the use described below.

2- To define an encoder using the constraint length, the generator polynomial, and possibly the feedback connection polynomial, use the network command inside the network architecture field.

3.5.2 Interleaver in SIMULINK

Interleaving switches symbols according to the mapping. Corresponding interferometer uses the reverse mapping to restore the original sequence of symbols. Interleaving and de-interference can be useful to reduce errors caused by impulse faults in the communication system.

Interleaver random block rearranges input vector elements with random transposition. The number of elements parameter indicates how many digits are in the input vector. If the input is frame dependent, then it should be facing upright. The block can accept data types int8, uint8, int16, uint16, int32, uint32, Boolean, single, double, and Fixed point. The data type of this output will be the same as that of the input signal. The prime parameter initializes the random number generator that the block uses to determine permutation.

The Bernoulli Binary Generator block generates random binary numbers using a Bernoulli distribution. The SIMULINK Structure for interleaver I will design two blocks the Random Interleaver & the Bernoulli Binary Generator block.

3.5.3 Turbo Codes in SIMULINK

The SIMULINK Block for Turbo Encoder which I will design is a combination of interleaver and convolutional encoder so the encoded can be found by combining them. The two models was tested and verified in MATLAB so the implementation of turbo codes just by concatenating

"simple convolutional encoder ([1 0 1 0 1],[37,21],5)" since the constraint length is memory+1=3+1=4 and connections are 15,17 in octal form. The output result for this sequence is 1110010010 is show in figure 4.1.

4.2.1. Simple Convolutional Encoder

This is the MATLAB function build in figure 4.1 for encoding an input through the convolutional code.

To get output by encoding input sequence [1 0 1 0 1] using this encoder we will use the function as:

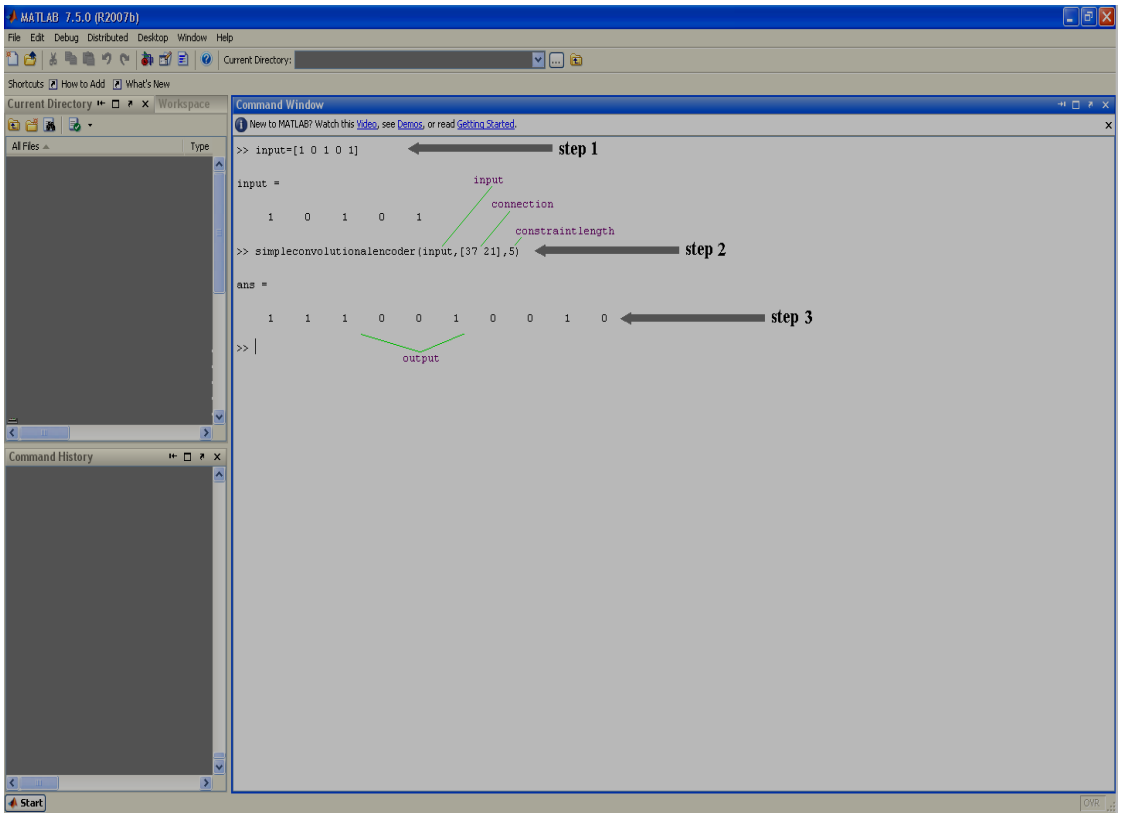

Figure 4.1 MATLAB Result for Convolutional Encoder

4.2.2 RSC Convolutional Encoder

This is the MATLAB function is build for encoding an input through the convolutional code.

To get output by encoding input sequence [1 0 1 0 1] using this encoder we will use the function as: rsc convolutional encoder([1 0 1 0 1],[37,21],37,5)"Since the constraint length is memory +1=3+1=4 and connections are 37,21 in octal form with feedback connection is 37. The output result is 1101110110 is show in figure 4.2.

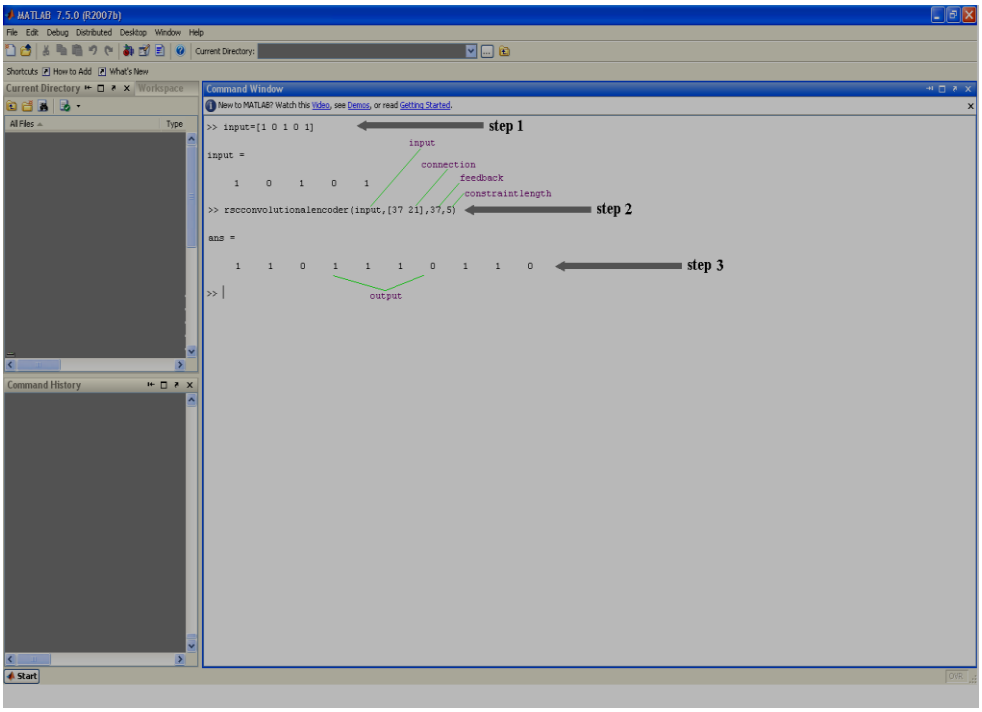

Figure 4.2 MATLAB Result for RSC Encoder

Figure 4.3 MATLAB Result for Interleaver & Deinterleaver

4.2.4 Turbo Encoder

This is the MATLAB function is build for encoding an input through the TURBO code of rate 1/3 shown in Figure 4.4.

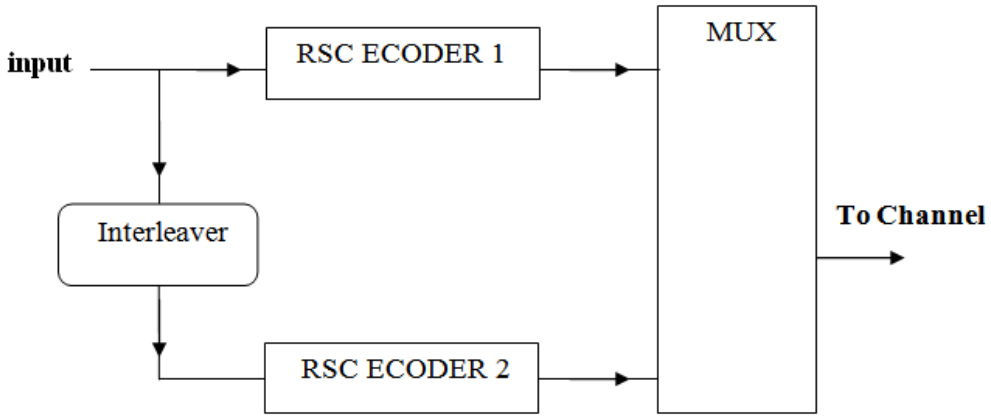

Figure 4.4 Block Diagram of Turbo Encoder

4.3 SIMULINK Implementation Results

As previously we have created four functions in MATLAB that are converted to MDL (SIMULINK Model). The result and use of the four functions is presented in the following sections.

4.3.1 Convolutional Encoder

The MDL model is same as in the MATLAB function build for encoding an input through the convolution code. The Model is shown in figure 4.6.

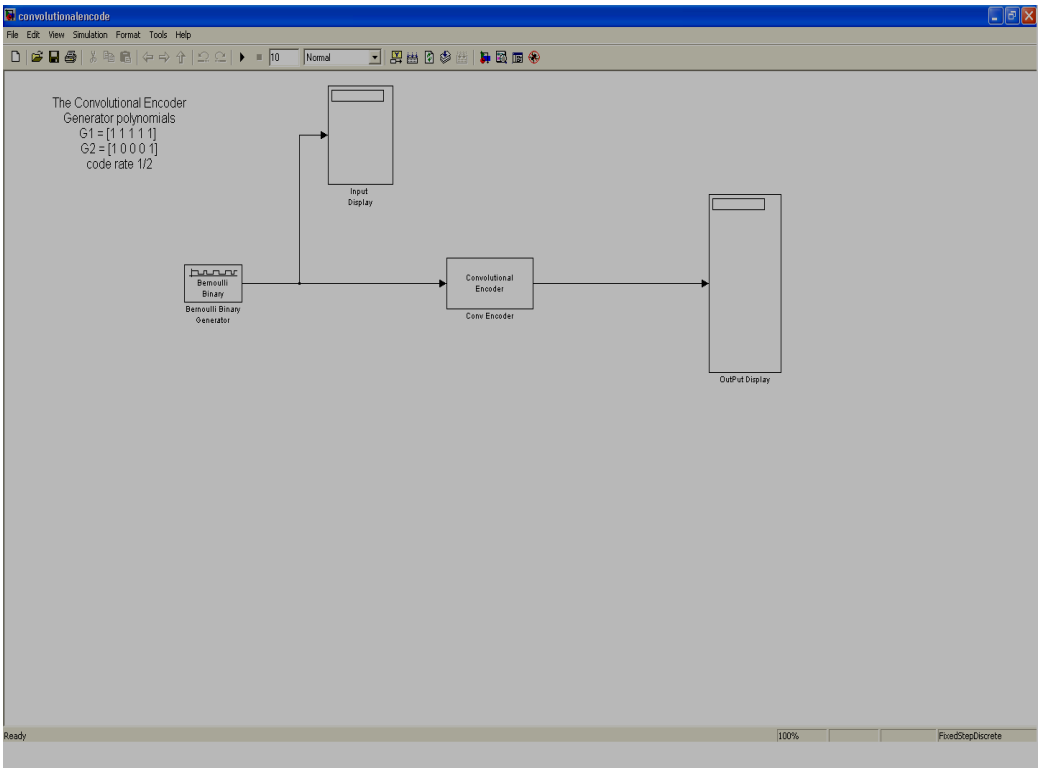

Figure 4.6 SIMULINK Convolutional Encoder Block

4.3.3 The Interleaver

The interleaver implementation using the simulink is depicted in figure 4.9. It is the simple generation of a randomized data to performs data scrambling.

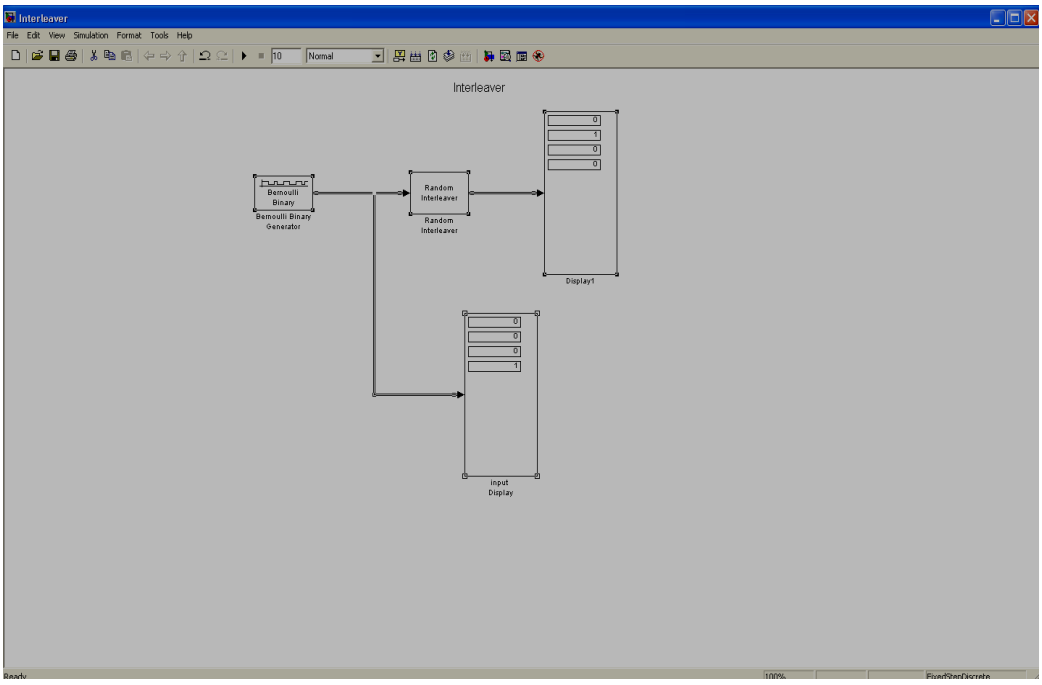

Figure 4.9 SIMULINK Structure for Interleaver

4.3.4 The Turbo Encoder

The turbo encoder is combination of interleaver and convolutional encoder so the encoded result can be found by combining them as shown in figure 4.10.

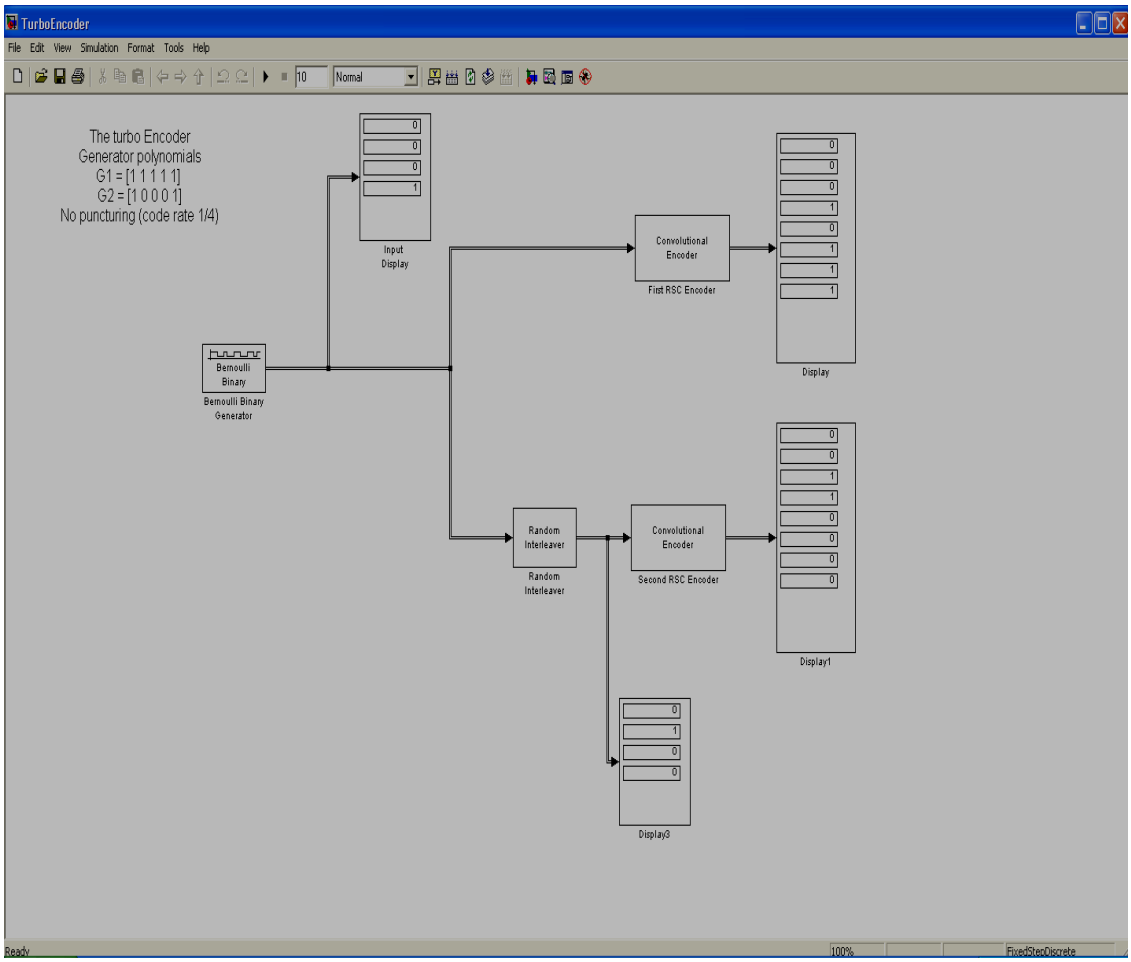

Figure 4.10 SIMULINk Block for Turbo Encoder

4.4 FPGA code conversion from MDL to HDL

created The four created functions in SIMULINK that are in MDL (SIMULINK MODEL) now can be converted to HDL language using the following steps. The result and use of the four functions is given diagram in figure 4.11.

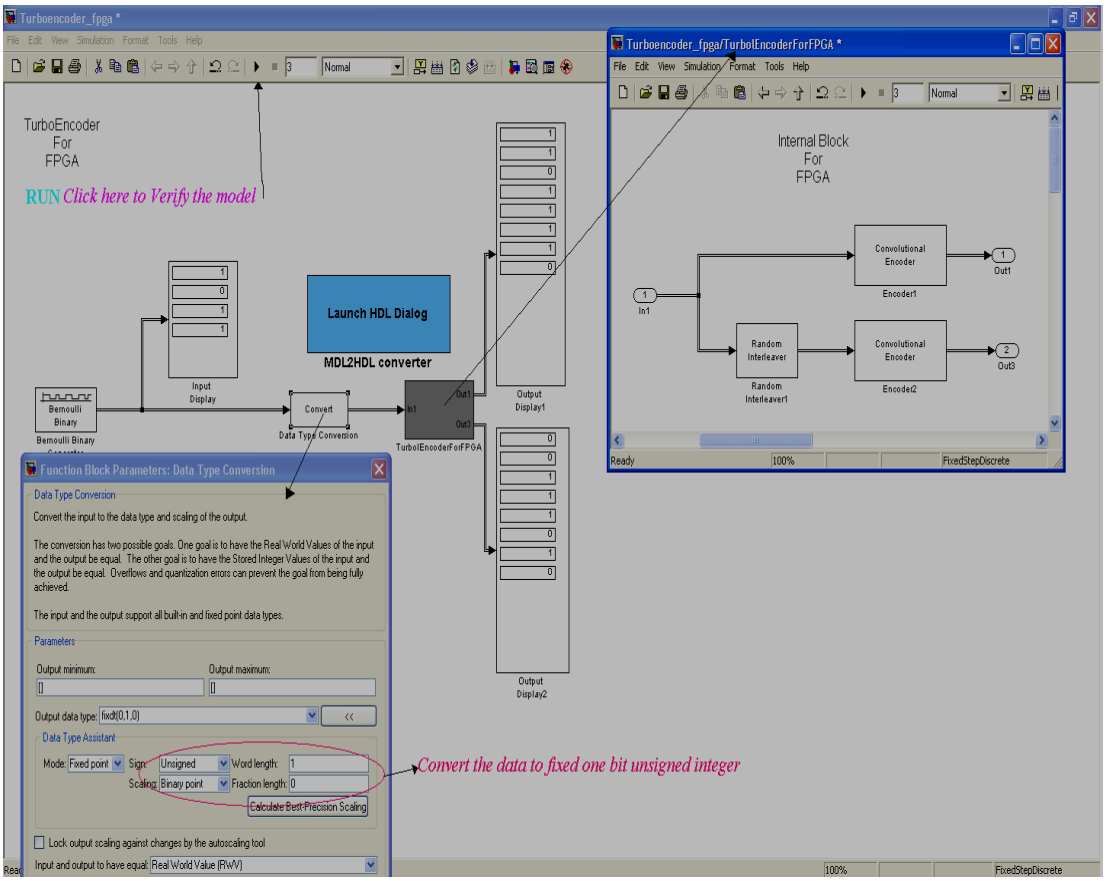

Figure 4.11 The result for all the function

To genertae the HDL code from mdl model open the mdl model turboencoder.mdl and click the block MDL2HDL in figure 4.12.

Figure 4.12 MDL2HDL Converter

research that is carried out in the field of wireless communications.

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4.5 Results of Implementation Analysis and Assessments

The work was divided into modules. These modules were first tested in MATLAB and then were implemented on real hardware using SIMULINLK block on FPGA. The designing and implementation of real time encoder has been presented. The RSC encoder together with interleaver and turbo encoder have been designed, and the real time is implemented and evaluated.

v. CONCLUSIONS AND FUTURE WORKS SUGGESTIONS

5.1 Conclusions

A real time channel encoding block has been systemized and the baseband encoding block has been implemented in software. The encoder has been verified in different way. The Design constructed was based on verification and then implementation for verification MATLAB was used as it is easy to program it. While for implementation SIMULINK HDL code generator was used. The overall problem of designing the error correcting code block was divided into three parts. First to verify and design convolutional codes then to design the interleaver model and at the end the turbo codes which was the main objective. Most of the functionality was tested by using MATLAB, Implementing baseband encoder is done by FPGA and its VHDL code simulated in Modelsim.

5.2 Suggestion for Future works

The base-band encoder has different parts one can implement the other parts too. Like the baseband encoder transmitter and receiver analog parts have to be designed. The speed optimization can be done, where the division of functionality between the DSP and FPGA is an important and complex part. Much time must be spent on testing if it is worth sending data to the FPGA and back for some functionality, or if it is better to do it on the DSP. Also the work can be upgraded with the latest