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RESEARCH ARTICLE OPEN ACCESS

Optimized Reversible Arithmetic and Logic Unit (ALU)

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ABSTRACT
Reversible logic is one of the emerging techniques which has promising applications in quantum computing. For more than 40 years for now, we have been using logic gates (which are irreversible) for designing the digital circuits like mux, encoder, decoder multiplier, ALU, Processors, Etc. Since reversibility over-rides some of the major problems of irreversible concepts like dissipation of major amount of energy in the form of bits, and input can be derived from output bits, we have started adopting that technique. And also low power is the main goal in today's challenging VLSI industry. The main agenda of reversible circuits is to minimizing the no. of garbage outputs, constant inputs, Quantum cost and no. of gates used. The objective of this project is to design a reversible ALU and write the verilog code, simulate it using Xilinx(14.7) tool and compare it with the existing ALU designs. So as to say that we have improved the design and minimized all the constraints.
Keywords **-** ALU, Constant inputs, Garbage outputs, Quantum cost , Reversible logic**.**

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I. INTRODUCTION

We have been using conventional logic gates i.e AND, OR, NOR, NOT, Etc to design the digital circuits for so many decades. John von Neumann had proposed a theory saying that if we use irreversible gates (conventional logic gates), then there is loss of data since we give more inputs and get only one output the other input bits are lost and that lost bit is librerated as heat. . In[2] 1961 Rolf Landauer attempted to apply thermodynamic reasoning to digital computers, and he stated that the date or bit is lost and the lost bit is generated as heat, which has an energy of $kT \ln 2$ **(**which is called Landauer limit**),** where k is the Boltzmann constant (approximately 1.38×10^{-23} J/K), T is the temperature of the heat sink in kelvins, and $\ln 2$ is the natural logarithm of 2 (approximately 0.69315). After setting T equals to room temperature 20 °C (293.15 K), and Landauer limit is almost equal to 0.0175 eV, which is very less, but as millions and millions of gates are used in a processor design and billions of operation is performed per sec, the energy liberated will be very large in amount. Due to this the system will become warm in no time. In 1973, C. H. Bennett proved that using a network of reversible gates, the energy dissipation can be controlled [3]. He showed that kTln2 energy dissipation would not occur if the computation are carried out in a reversible way. Reversible logic has several applications in quantum computing, nanotechnology, DNA technology, Etc. In current generation there is a lot of demand for reversible logic design since one of the major advantage is low power consumption, which is the main requirement in low power VLSI design.

II. MOTIVATION

Since we already are using 9nm cmos transistors chips, and it is not possible to reduce the gate oxide length of a semiconductor(can be almost reduced to 5nm but it becomes complex to reduce the size still more), we needed a new technology to keep the moore's law alive. As and when people started designing the reversible logic for various fields, they started to find many applications of reversible logic. For high computation devices we need to have less power consumption that was the main criteria, but by using conventional logic gates the power consumption was increasing rather than decreasing. So reversible logic was a promising and

pre-eminent technology we started designing reversible logic circuits. And it has also been said that reversible logic will be used in future generation for Quantum computing, and for complex calculations.

III. BASIC DEFINITIONS

1. GARBAGE OUTPUTS

Some of the output remains unused to maintain bijective mapping between inputs and outputs in a circuit. These unused outputs are termed as Garbage Outputs.

2. QUANTUM COST

The operations of a reversible gate is directed by several quantum operations which is constituted with elementary quantum gates. The Quantum Cost (*QC*) is equal to the total number of elementary used to realize a reversible circuit.

3. GATE COUNT

The total number of basic reversible gates required to realize a circuit is its Gate Count.

4. CONSTANT INPUTS

For some operation to be performed we need to make one or more inputs as logical 0 or 1, so as to get the desired outputs. The number of constant inputs needs to be reduced.

IV. BASIC REVERSIBLE GATES

Reversible logic gates are the gates which have same number of inputs and outputs(n*n) which has one to one mapping. This is the main difference between conventional logical gates(AND, OR, NOR, Etc) and reversible logic gates. This helps to determine the inputs uniquely from the outputs. And there are some set of rules which needs to be followed while designing the reversible circuits. They are ;

- Fan-out is not permitted.
- Loops or feedbacks are not permitted.
- Garbage outputs must be minimum
- Minimum delay
- Minimum quantum cost.
- Minimum constant inputs.

1. Feynman Gate (Cnot gate)

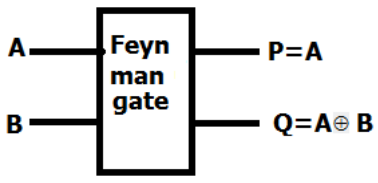

Fig 1

The Reversible 2*2 gate with Quantum Cost of 1 having mapping input (A, B) to output (P = A, Q= A⊕B) is as shown in the Fig. 1.

2. Toffoli Gate

Fig 2

The Reversible 3*3 gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P=A, Q=B, R=A&B⊕C) is as shown in the Fig. 2.

3. NOT Gate

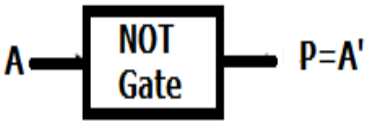

Fig. 3

This is a 1*1 gate having 1 to 1 mapping. The input A is mapped to P=~A is as shown in the Fig. 2.

4. Fredkin Gate

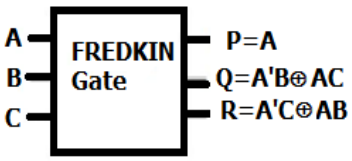

Fig 4

This is a 3*3 gate, the input (A, B, C) is mapped to output (P=A, Q A′B⊕AC, R=A′C⊕AB) as shown in Fig. 4.

5. Peres Gate

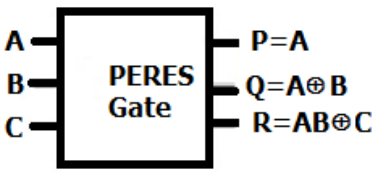

Fig 5

This is a 3*3 gate, the input (A, B, C) is mapped to output (P=A, Q A⊕B, R=AB⊕C) as shown in Fig. 5.

V. COMPARATIVE STUDY

There are many reversible gates which are given in the table 2.31, which contains the comparison is in terms of no. of input, output

vectors, and there respective Quantum cost. Every gate is unique in there own way, each gate has the capability to perform more than one logical operation by making some changes in the input i.e by making some inputs as logic 1 / logic 0.

Table 1: Basic reversible gates

REVERSIBLE GATES	QUANTUM COST	TYPE
Feynman Gate	1	1*1
Fredkin Gate	5	3*3
Toffoli Gate[4]	5	3*3
New Gate	7	3*3
Peres Gate[5]	4	3*3
COG Gate	4	3*3
Feynman Double Gate	2	3*3
NFT Gate	5	3*3
URG Gate	5	3*3
TR Gate	6	3*3
HNG Gate	6	4*4
PEAG Gate	6	4*4
MRG Gate	6	4*4
TSG gate	14	4*4
MKG Gate	13	4*4
FTGA Gate	8	5*5

VI. APPROACHES FOR DESIGNING AN ALU

There are 3 main approaches for designing an reversible ALU. They are;

1. DESIGN USING MUX

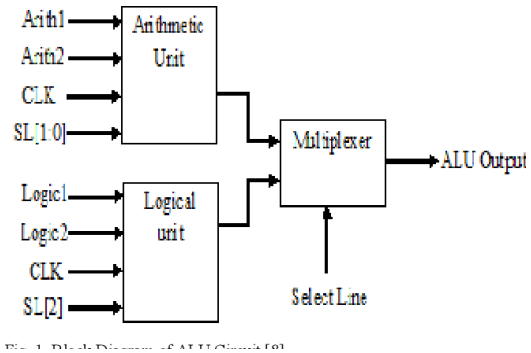

Fig. 6

As we can see in the Fig.6, first we design the Arithmetic unit(AU), and then Logical Unit(LU), and then with use of MUX we integrate the whole circuit [8]. Here MUX is used to select the operation to be performed whether arithmetic or logical operation, If we increase the no. of operation units then we also have to increase from 2:1 mux to 4:1 or 8:1, and so on. So the complexity and quantum cost also increases drastically.

2. DESIGN USING CONTROL UNIT

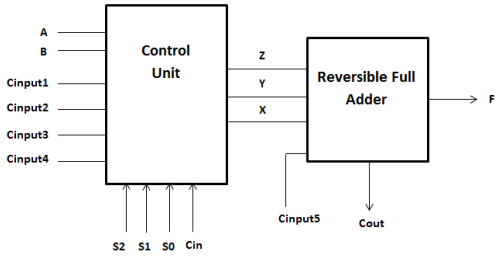

Fig. 7

As we can see in Fig. 7 that control Unit is used to design an ALU [9]. According to the select lines given to the control unit the specific operation is selected and performed.

3. SINGLE DESIGN

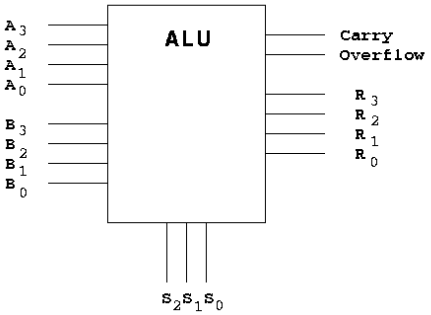

Fig. 8

As we can see in Fig. 8 the arithmetic and logical operation which needs to be performed in a single design [10], and the operation which needs to be performed is selected using the select lines. As the number of operations increases the no. of select lines also must be increased, so the design complexity increases.

VII. PROPOSED DESIGN

We have taken the second approach, using CU. Here we have designed a main block that is control unit, where all the operations are performed and are selected using select lines given to it. An adder is cascaded in front of cu in-order to perform extra addition operations.

Here we have used 3 CNOT, 2 MFRG and 2 PERES gates to design the control unit, and an extra HNG gate to act as an adder. The CU circuit is shown in fig 9 and the overall ALU circuit is shown in fig 10.

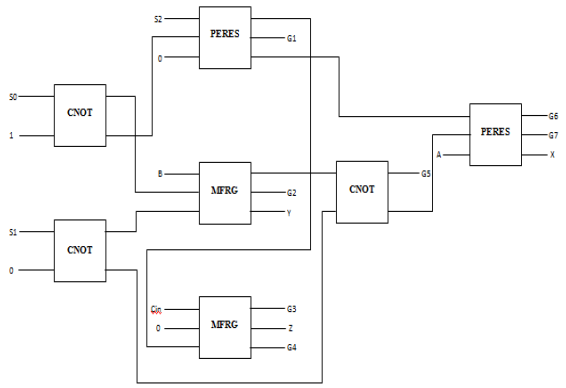

Fig. 9 Control unit block

The output which propagates from cu block, which are X,Y and Z are given as inputs to the HNG gate to perform addition operations and according to the select lines given to the control unit the specific operation is selected and performed.

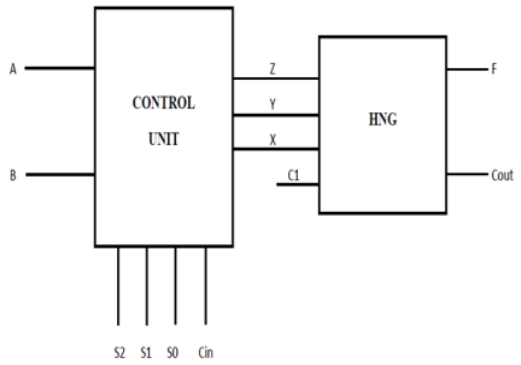

Fig. 10 of ALU design using Control Unit

The quantum cost, constant inputs, and garbage outputs are given in the comparison section. The truth table indicating all the operations performed by the ALU using Control Unit is shown in the table 2.

Table 2 operations being performed

S2	S1	S0	Cin	Operations	Function
0	0	0	0	A	Transfer A
0	0	0	1	A+1	Increment A
0	0	1	0	A+B	Addition
0	0	1	1	A+B +1	Add with Carry
0	1	0	0	A-B -1	Subtraction with Borrow
0	1	0	1	A-B	Subtraction
0	1	1	0	A-1	Decrement A
0	1	1	1	A	Transfer A
1	0	0	X	A|B	OR
1	0	0	X	A^B	XOR
1	0	1	X	A&B	AND
1	0	1	X	~A	NOT A

VIII. SIMULATION AND RTL SCHEMATIC

The RTL schematic is shown in fig 11, and simulation snap is given in fig 12. As we can see in the RTL schematic, we are able to find out how many gates have been used and which are those. Totally 8 gates have been used.

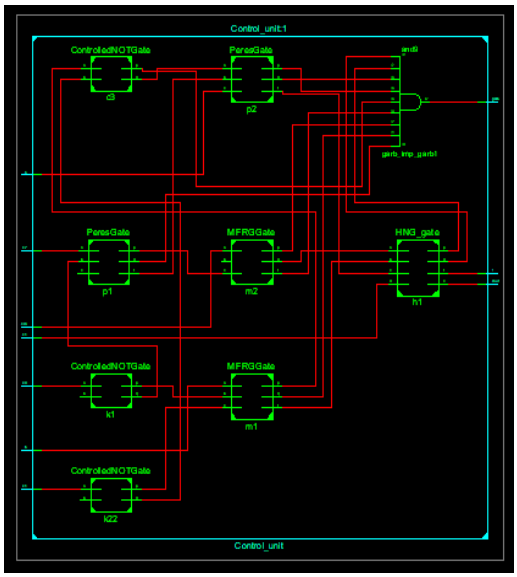

Fig. 11

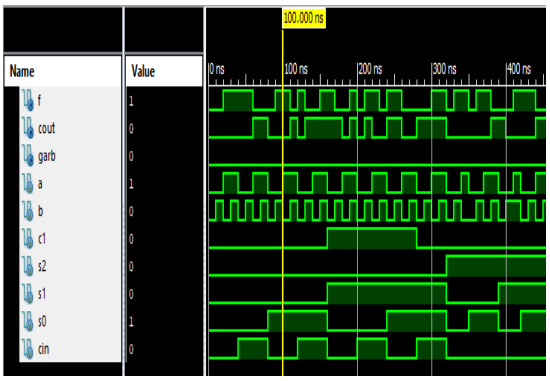

Fig. 12

In the above simulation results of the ALU designed using Control Unit, the yellow marker indicates the results when: **s2=0; s1=0; s0=1;** indicating that the operation **(A+B)** is chosen (according to the table 2) and the inputs given are **a=1; b=0; cin=0;** hence the result obtained is **sum(f)=1; cout=0.**

IX. COMPARISON AND DISCUSSION

As design [7] has been optimized to the fullest in terms of design, we tried to optimize still more and we were successful. As we can see in the below comparison, garbage output has been reduced by 1 when compared to design [6], number of operations are same compared to both the designs,

but quantum cost has been reduced by 2 when compared to design [6], qc has been reduced and by 1 when compared to design [7] and finally gate count has been reduced by one when compared to design [6].

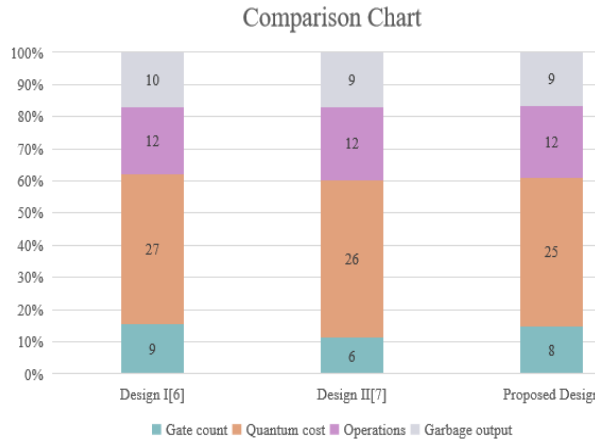

Fig. 13

X. CONCLUSION

The proposed ALU deigns show significant improvement in terms of quantum cost and garbage outputs when compared to the existing counterpart designs. The comparison table is given in fig 13. By looking at the table 13 we can say that our design is better in terms of quantum cost, garbage outputs and also no. of gates used.

XI. APPLICATIONS

There are many applications to reversible logic, this is going to be the future technology. Some of them are,

- Nanocomputing
- Quantum computations
- Laptop/Handheld/Wearable Computers
- Spacecraft
- Implanted Medical Devices.
- Wallet “smart cards”.

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