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Design and Analysis of High Gain DC-DC Converter with a combination of LC Network

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ABSTRACT
In this paper, Active switched capacitor effectively enhances the voltage by producing maximum voltage gain with minimum duty cycle in the high gain DC–DC circuit due to the presence of combination of LC network. The proposed circuit is the modification of conventional high gain converter to overcome drawbacks and proposed network is simple as it requires a low number of switch components and also the voltage stress on the diodes, capacitor and switches are reduced compared to base circuit. This paper presents the system design, operation of the proposed system and the comparison with base network is presented. Performance is verified by simulating circuit using MATLAB software for the proposed system.
Keywords – Active switched capacitor network, Duty cycle, High gain DC-DC converter, Voltage gain, Voltage stress

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I. INTRODUCTION

DC power converters with maximum voltage are

normally used as generators to attain desired load and they are used in applications like PV, medical equipment, electric tractions, automobiles, uninterrupted power supplies and mainly used in renewable energy conversion.

A boost converter can be used to enhance voltage

but it is not sufficient to use in high step up applications with a disadvantage of extreme duty ratio. Hence, transformer less converters can be preferred to enhance voltage with minimum duty ratio and also reduction in stress across devices [1].

Bidirectional converter with coupled inductors [2]

produces voltage higher than other converters with high stress leading to reverse recovery problems. Voltage gain is boosted with average duty cycle by integrating quadratic boost and boost converters and losses are also minimized [3]. Interleaving converters produces voltage more than traditional converters with lower stress and enhances efficiency [4]. Boost converter with coupled inductors [5] and converter with current fed Cockcroft-Walton multiplier [6] achieves a high voltage gain ratio with eliminating ripple input current and efficiency reduces due to hard switching. Employing soft switching techniques [7] like ZVS or ZCS enhances efficiency but stress across power devices will not be reduced. An active snubber circuit is employed to reduce the voltage spike and produces zero voltage switching. ZVS can also be achieved by interleaving parallel input and series output [8]. Converter with switched capacitor and inductor, converter with series of voltage-lift inductors [9] and by expanding active-passive inductor cells [10] attains maximum gain but the components used are high. Interleaving voltage multiplier with boost converter [11] can produce desired voltage for low input voltage and this topology can be used in PV applications. voltage can be further amplified by increasing the number of turns in an inductor but circuit should be designed in such a way to avoid transformer saturation

In this paper, a traditional high gain converter as

shown in fig. 1 gives desired voltage but consists of some drawbacks. Hence, it is modified and proposed as shown in fig.2 by adding an active switched capacitor to overcome the demerits of base converter. Some of the disadvantages of base converter are number of switch components used are high, high duty cycle is used and voltage stress across switches are high. Hence modified circuit enhances the voltage gain by using only one with least duty ratio. The system design, working and operating principle of the modified system is discussed in detail and also comparative analysis with base converter is also discussed.

II. OPERATION OF PROPOSED TOPOLOGY

Non-isolated high gain converter as shown in fig.1
consists of some drawbacks, hence it is modified by including one extra capacitor, diode is replaced between capacitor and switch S_1 and switch S_3 is removed as shown in fig.2. Operation of the modified converter is done by assuming that all are ideal components in the circuit and voltage is constant by using high rating capacitors. The CCM mode operation of proposed topology consists of two modes and it is explained below:

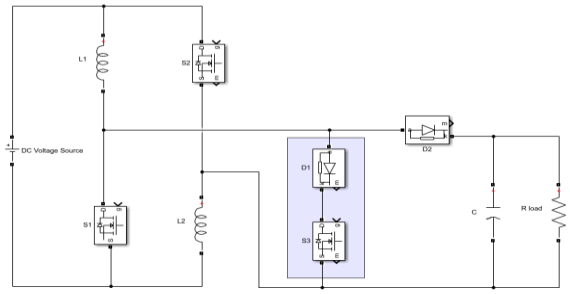


Fig.1 : High gain converter

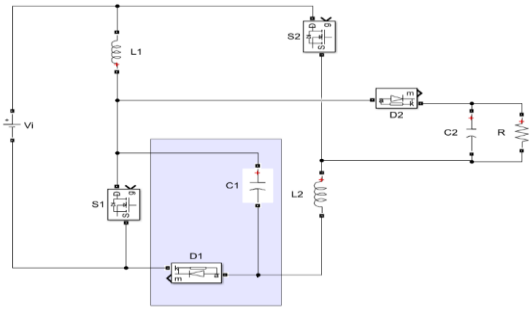


Fig.2 : Modified converter

Mode 1: Diodes are in off condition and the switches are in active mode. The inductors get charged from the input source and inductor L_2 and load are energized from the discharged energy of capacitors. The voltage equations are derived as

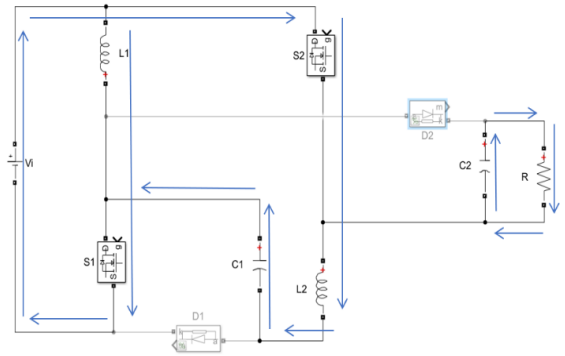
$$V_{L1} = L_1 \frac{di_{L1}}{dt} = V_i$$

$$V_{L2} = L_2 \frac{di_{L2}}{dt} = V_i + V_{C1}$$

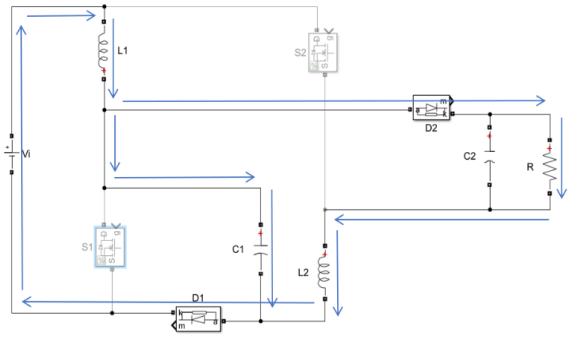
Mode 2: Diodes are active and the switches are not in working mode. The series connected inductors are discharged and the energy discharged charges load and output capacitor. Also, input supply charges capacitor C_1. The voltages equations are

$$V_{L1} = L_1 \frac{di_{L1}}{dt} = V_i - V_{C1}$$

$$V_{L2} = L_2 \frac{di_{L2}}{dt} = V_{C1} - V_0$$



(a)



(b)

Fig. 3: Operation in CCM. (a) Mode 1. (b) Mode 2.

III. DESIGN PARAMETERS:

The converter with a rating of 100W gives 200V output for an input of 20V. The output current and resistance are calculated as follows:

$$I_o = \frac{P_o}{V_o} = \frac{100}{200} = 0.5\,A$$

$$R_o = \frac{V_o^2}{P_o} = \frac{200 * 200}{100} = 400\Omega$$

Voltage gain:
Voltage gain is calculated for duty ratio, D = 0.65

$$Voltage\ Gain = \frac{(1 + 0.65 - (0.65)^2)}{(1 - 0.65)^2} = 10$$

Inductor design:
To calculate inductor value, inductor ripple current should be calculated

$$\Delta i_L = (20\%\ to\ 40\ \%\ of\ I_0) * \frac{V_o}{V_{in}}$$

Δi_{L1} = 1.3 and Δi_{L2} = 1.25,

$$L_1 = \frac{V_i\ D}{\Delta i_{L1}\, f_S} = \frac{20 * 0.65}{1.3 * 50K} = 200\mu H$$

$$L_2 = \frac{V_i}{\Delta i_{L2}\, f_S} \frac{D(2 - D)}{(1 - D)} = \frac{20 * 0.65 * (2 - 0.65)}{1.25 * 50K * (1 - 0.65)} = 800\mu H$$

Capacitor selection:

The output capacitance is obtained by assuming ΔV_{C0} as 0.065 and ΔV_{C1} as 0.84,

$$C_1 = \frac{D}{(1-D)}\frac{I_0}{\Delta V_{C1} f_s} = \frac{0.65 * 0.5}{(1-0.65) * 0.84 * 50k} = 22\mu f$$

$$C_o = D\frac{I_o}{\Delta V_{C0} f_s} = \frac{0.65 * 0.5}{0.065 * 50K} = 100\mu f$$

IV. SIMULATION RESULTS

The proposed topology is simulated using
using MATLAB Simulink and it is presented in fig.4. The circuit is designed and simulated based on the parameters shown in Table I and the simulated results are represented in fig.5.

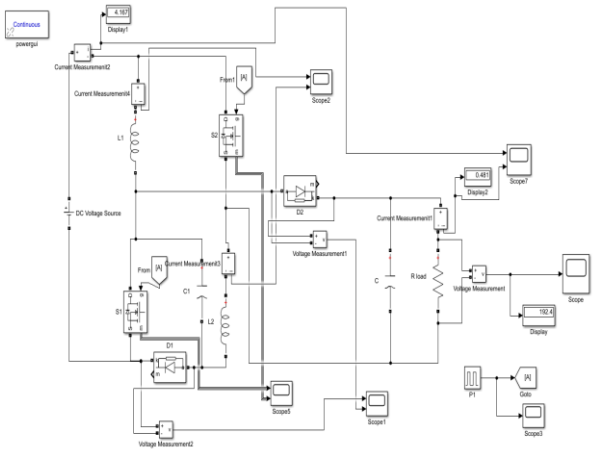


Fig 4: Simulink circuit

Table I: Simulation parameters

Parameters	Value
Input voltage	20 V
Output voltage	200 V
Duty ratio (D)	0.65
Power	100W
Frequency	50 kHz
Resistance	400 Ω
Inductors (L_1, L_2)	200µh,800µh
Capacitors (C_1, C_2)	22µf, 100µf

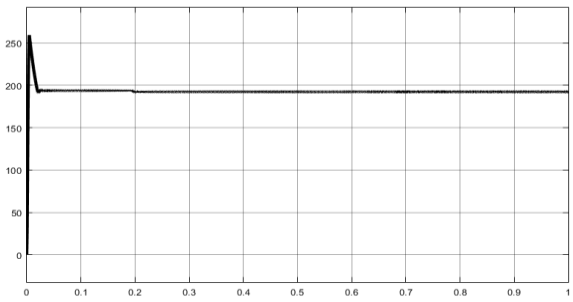


Fig 5 (a): Output voltage

Fig. 5(a) represents the output voltage of 193 V for input voltage of 20 volts and a voltage gain of 9.65 is achieved.

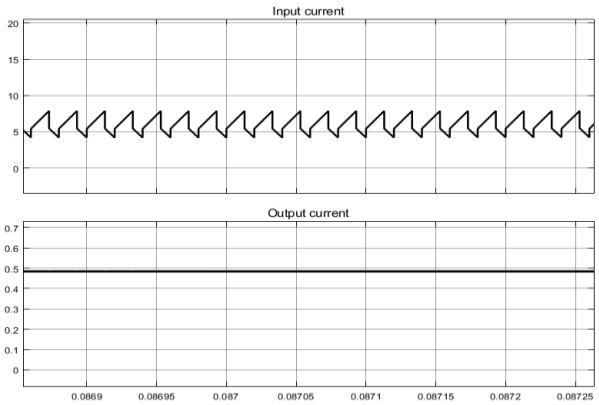


Fig 5 (b): input and output currents

Fig. 5(b) represents the input and output current waveforms with a mean value of the 5.8 A for input current and the output current of 0.48 A and they are close to theoretical values.

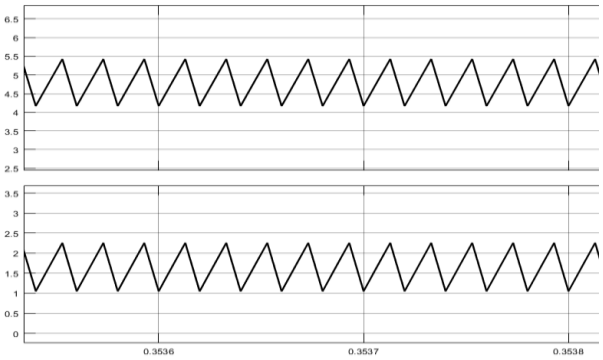


Fig 5 (c): inductor currents (i_{l1}, i_{l2})

Fig 5(c) represents the inductor currents with $i_{L1\,(max)}$ =5.4 A, $i_{L1\,(min)}$ =4.16 A and $i_{L2\,(max)}$ =2.25 A, $i_{L2\,(min)}$ =1.05 A and change in inductor current is obtained as Δi_L= 1.2 A.

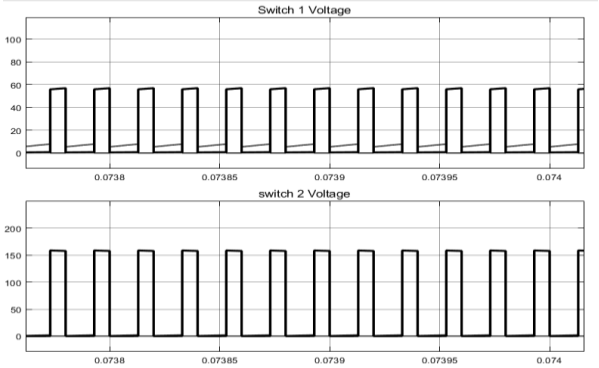


Fig 5 (d): Switch voltages

Fig. 5(d) shows the voltage stress on switches, S_1 = 56 V and S_2 = 157 V respectively.

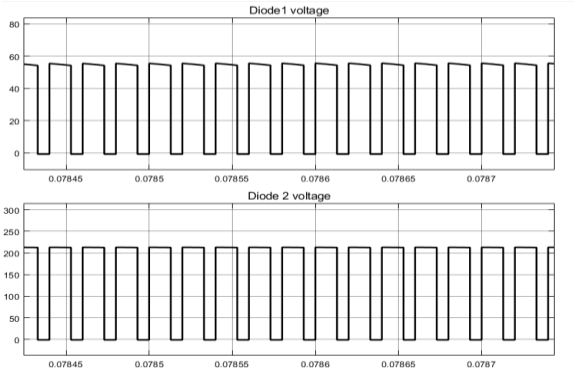


Fig 5 (e): Diode voltages

Fig. 5(e) represents the diode voltages, V_{D1} = 55 V and V_{D2} = 211 V respectively, which are close to theoretical values. The comparative analysis of the modified with base circuit is represented in the table II. As per the table same voltage gain is obtained with less duty cycle only compared to base circuit and the stress on switches of modified topology are less than the base circuit which is shown graphically in fig.6. and also the modified system consists only two switches.

Table II : Comparison of circuits:

	Base topology	**Proposed topology**
Voltage Gain	$\frac{V_o}{V_i} = \frac{1+D_1}{1-D_1-D_2} = 10$	$\frac{V_0}{V_i} = \frac{1+D-D^2}{(1-D)^2} = 10$
Duty Cycle	$D_1 = 0.5$ $D_2 = 0.35$	D =0.65
Voltage stress on Switches	$V_{DS1,2} = \frac{V_o + V_i}{2} = 110V$ $V_{DS3} = V_0 = 200V$	V_{DS1} = 56 V V_{DS2} = 157 V
Switches	3	2

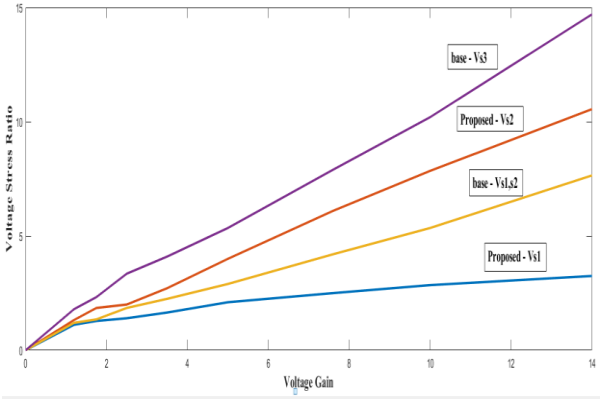


Fig.6: Voltage gain versus Voltage stress

V. CONCLUSION

The design of base and modified circuit and the operation of proposed system is represented and also advantages of modified with base system is presented. Performance of system is verified by simulating circuit using MATLAB software which produce a voltage of 193V for an input of 20V. Hence, this proves that the maximum gain with duty cycle of 0.65 is achieved and also stress across devices are minimized.

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