RESEARCH ARTICLE OPEN ACCESS

Implementation of Sinusoidal Pulse Width Modulation for Single Phase Inverter Using FPGA

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Abstract: The purpose of this project is to control the switches of Single phase inverter using Sinusoidal Pulse Width Modulation technique. The SPWM technique is used because it is facile to accomplish in circuits and provide better control of switches in the circuit. The SPWM generation is flourished using Xilinx Spartan 6 based Field Programmable Gate Array (FPGA). Xilinx ISE is a software tool designed by Xilinx for analysis and synthesis of HDL designs, which will help the developer to configure target device. SPWM is created using VHDL program. Simulation results are obtained using ModelSim software and FPGA implementation using Digilent Adept Software. Output of SPWM generation developed in FPGA and displayed in DSO.
Keywords: Field Programmable Gate Array (FPGA), Sinusoidal Pulse Width Modulation (SPWM), Pulse Width Modulation(PWM), Very high speed integrated circuit Hardware Description Language (VHDL).

Date of Submission: 22-03-2020 Date Of Acceptance: 08-04-2020

I. INTRODUCTION

Nowadays, FPGA is preferred over other devices because they are flexible, can be reprogrammed to perform different task from original task and faster to acquire. That is reason to use FPGA for SPWM for single phase inverter. Drive control of analog circuits is done using Pulse Width Modulation. Inverter output voltage is regulated by diverse methods and one of the efficient method of control is Pulse Width Modulation control technique. It is nothing but adjusting turn on and turn off periods of switching devices of the inverter. Due to development in the field of power electronics PWM inverters is be used for many industrial applications like motor control. Countless modulation techniques are available in practical applications. Basically, they are classified into two types as carrier based and carrier less modulation techniques. Some of the common methods among them are Sinusoidal Pulse Width Modulation (SPWM), Modified Pulse Width Modulation (MPWM), Space Vector Pulse Width Modulation (SVPWM) and Random Pulse Width Modulation (RPWM).The Sinusoidal Pulse Width Modulation technique is the effortless and imprecise method used for industrial applications as it is uncomplicated to establish and control. It is also more suitable with modern digital systems. This paper establishes the generation of SPWM using FPGA.As an initial stage of this process software program is generated using VHDL code in Xilinx software. Next that code is simulated in ModelSim tool and output of the code is verified. Then, it is accomplished in Atlys Spartan 6 FPGA board using Digilent Adept software. It creates the drive signals for the switches of the single phase inverter. Atlys board is based on Xilinx Spartan-6 FPGA. It is programmed by Digilent Adept software and programming can also be done using the Digilent Plugin for Xilinx Tools. It is also computed that use of FPGA is much better to create control signals for single phase inverters. Further, it is established that switching pulses can be altered without any changes in hardware and reduces hardware complexity. The aim of this modulation technique is to get variable output voltage with lesser harmonics. As, FPGA can perform better DSP, Microcontroller and ASIC functions PWM switching sequence is controlled via FPGA The sinusoidal pulse width modulation is wave shaping technique used to discover the switching instants. This method is realized by comparing a high frequency carrier (triangular) signal with a sinusoidal reference signal. The crossover points will determine the switching periods. The following section extends the pulse width modulation. Section III extends about the single phase inverter. Section IV extends about the SPWM generation in Modelsim. Section V extends

FPGA design and specifications. Section VI confers the experimental investigation. Section VII deduces the paper.

II. PULSE WIDTH MODULATION

The Pulse Width Modulation is implemented widely to generate gate signals for power semiconductor switches. PWM is a method to reduce the average power delivered by the electric signal, by effectively chopped into discrete parts. The duration of the pulses varies from one pulse to another pulse according to a modulating reference signal. When the PWM signal is applied to a gate or base of a transistor, it causes "ON" and "OFF" intervals of the transistor to vary from one PWM to another PWM by the modulating reference signal. The frequency of a PWM signal must be much greater than the reference signal and the fundamental frequency.

The Carrier based modulation techniques is classified as

- ✓ Sinusoidal pulse width modulation
- ✓ Space vector modulation
- ✓ Modified pulse width modulation

2.1. Sinusoidal Pulse Width Modulation

The sinusoidal pulse width modulation is one among the foremost widespread and easy strategies utilized in most of the power electronics converters and to manage electric drives. The output waveform is obtained from the sine-triangle wave comparison. A reference sinusoidal waveform is compared with a carrier wave with high frequency (triangle wave) and PWM signal output is obtained high level ("1") at sinusoidal wave is greater than the instantaneously varying triangular signal and when it's lesser, then the signal is low level ("0"). therefore, the various come across points lead to variable duty cycle of the output wave shape. In sinusoidal pulse width modulation the gate signals are generated by comparing sinusoidal reference signal and triangular carrier signal and their intersection points determine the turn ON and OFF instants. It's easy to implement and control. Harmonic distortion is reduced by increasing the switching frequency. Fig. 2.1 depicts the waveform generation.

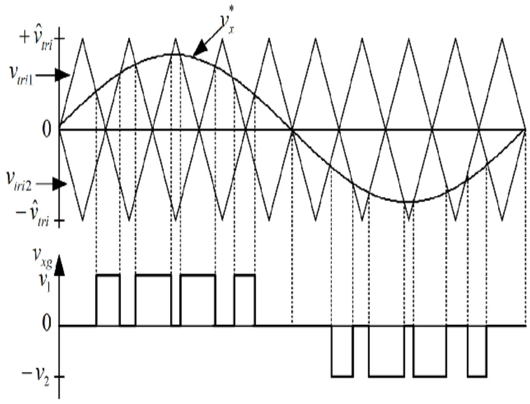

Fig 2.1. SPWM waveform generation

III. SINGLE PHASE INVERTER

An Inverter is known as DC-AC converter. It is a device which convert a DC input supply voltage into symmetric AC voltage of desired magnitude and frequency at the output side. Ideal and practical inverter have the output waveforms as sinusoidal and non-sinusoidal waveforms respectively. The inverter is called a Voltage Source Inverter (VSI),if the input is a voltage source. Similarly Current Source Inverter (CSI), where the input to the circuit is a current source. The VSI circuit has direct control over 'output (ac) voltage' whereas the CSI directly controls 'output (ac) current'. Fig. 3.1 shows the circuit of a single phase inverter.

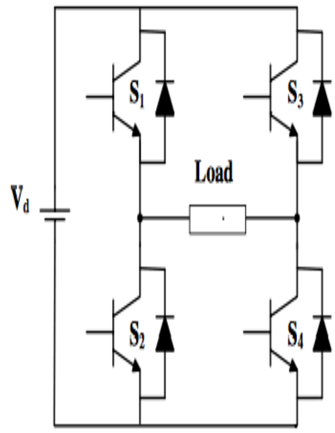

Fig 3.1. Single phase Inverter

3.1. SWITCHING SEQUENCE

The single phase full bridge inverter consists of a four power switches (S1-S4). The inverter operates in positive and negative cycles. Two switches are operated in each cycles. The switches S1 and S4 are operated in positive cycle and S2 and S3 are operated in negative cycle. We are generating the PWM signals for the gate of the semiconductor switches. Fig. 3.2 depicts the model graph of the gate signals and output voltage waveforms.

Condition for switching

Condition	Switching sequence
Vsin > Vtri	S1,S4 ON; S2,S3 OFF
Vsin < Vtri	S2,S3 ON; S1,S4 OFF

The TABLE gives the condition for which the sequence if switches turn ON.

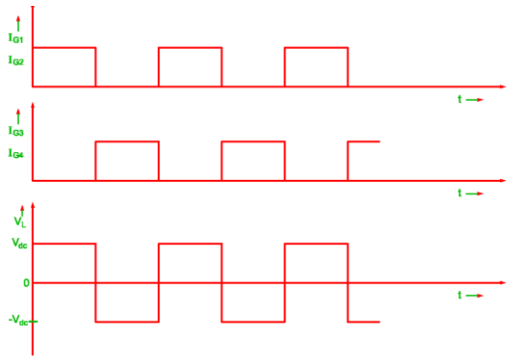

Fig 3.2. Gate signals and output voltage waveforms

IV. SPWM GENERATION IN MODELSIM

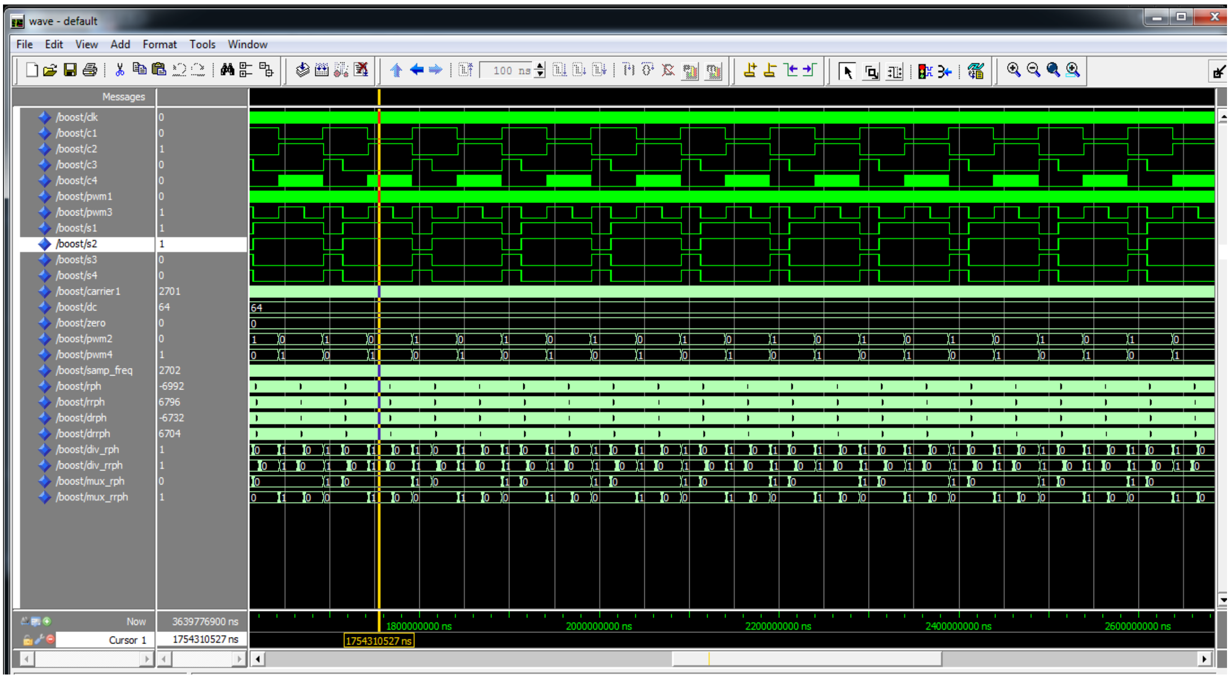

Fig. 4.1. Simulation output for SPWM generation

Fig.4.1 shows the SPWM generation using Modelsim. The clock act as input parameter, and the S1,S2,S3 and S4 act as output parameters. The other parameters are used as signals. The clock is used as input and the input clock range is set as 50 ns. When the clock pulse is given the output waveforms are obtained based on the program written. The sequence of two switches are similar.

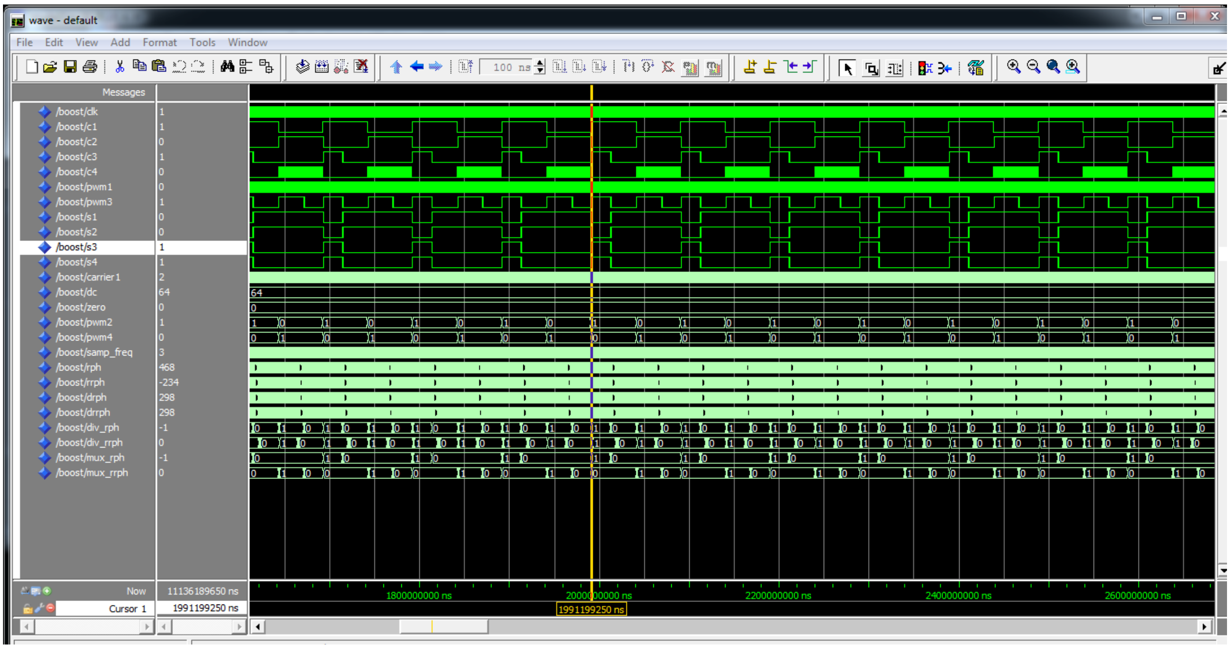

Fig 4.2. SPWM output for switches in the ModelSim Simulation

Fig.4.2 shows the SPWM generation for operation of switches in different cycles of supply. The Parameters PWMI and PWM2 are used as Gate pulses for the single phase inverters. In this fig the changes in switching sequence is shown.

V. FPGA DESIGN AND SPECIFICATIONS

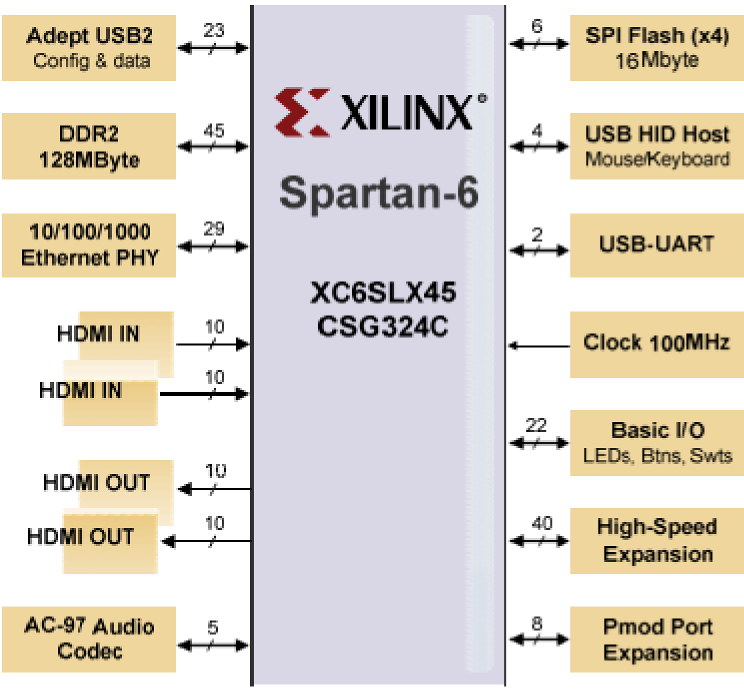

Fig 5.1. Block diagram of development board

The fig. 5.1 shows the block diagram of the development board. The Atlys circuit board is a complete ready-to-use digital circuit development platform based on Xilinx Spartan – 6 LX45 FPGA , speed grade -2. It supports several high-end peripherals such as Gbit Ethernet, HDMI Video, 128MByte 16-bit DDR2 memory, and USB and audio ports which makes the Atlys board an ideal host for various digital systems which includes embedded based processor design. It is also compatible with all types of Xilinx CAD tools including chip scope. The main advantage of this is that the designs can be completed at no extra cost. The CAD tool used as programming interfaces in the Atlys board are Xilinx and Digilent. The sources for the programming software are Digilent and Xilinx. The purpose of SRAM based memory cells in FPGA is to store the programming files which gives information about logic functions and circuit connections. The bit files are created for the VHDL , Verilog and Schematic based source files. The Adept software of Digilent and Impact software of Xilinx is used to program the FPGA using USB port. The Atlys Spartan – 6 FPGA is optimized for high performance logic and operates at 500MHz and above clock speeds. It has six phase locked loops which can be used to attain different frequencies using oscillator frequency. It consists of Adept and Impact USB port which can be used for the programming purposes. The Atlys board requires an external power source of 5V,4A which has a 2.1mm internal diameter plug. The voltage rails on the board use Linear Technology LTC2481 Delta-Sigma 16-bit ADC's to continuously measure supply current. The Atlys board uses a128Mbit Numonyx N25Q12 Serial Flash memory device for the purpose of storing configuration files. It consists of Marvell Alaska Tri-mode PHY (the 88E1111) paired with a Halo HFJ11- 1G01E RJ-45 connector. This can be used as a reference for creating custom designs. It consists of four HDMI ports of which two buffered ports used as input or output ports , one buffered port used as output port and one unbuffered port used for input or output purpose. The three buffered ports use type A connectors and unbuffered port use type D connector. It consists of a single 100MHz CMOS oscillator connected to pin L15 internally. The board consists of an EXAR USB UART bridge which facilitates the PC applications to communicate with the board. All the Atlys boards are guaranteed with a built in self test feature during the manufacturing process. It is possible to reprogram the FPGA and change the non-volatile data stored in the serial EEPROM chip at any time. The board consists of 68 - pin VHDC connector for high speed parallel input or output purpose and an 8-pin Pmod connector for low speed and lower pin count I/O pin.

VI. EXPERIMENTAL INVESTIGATION

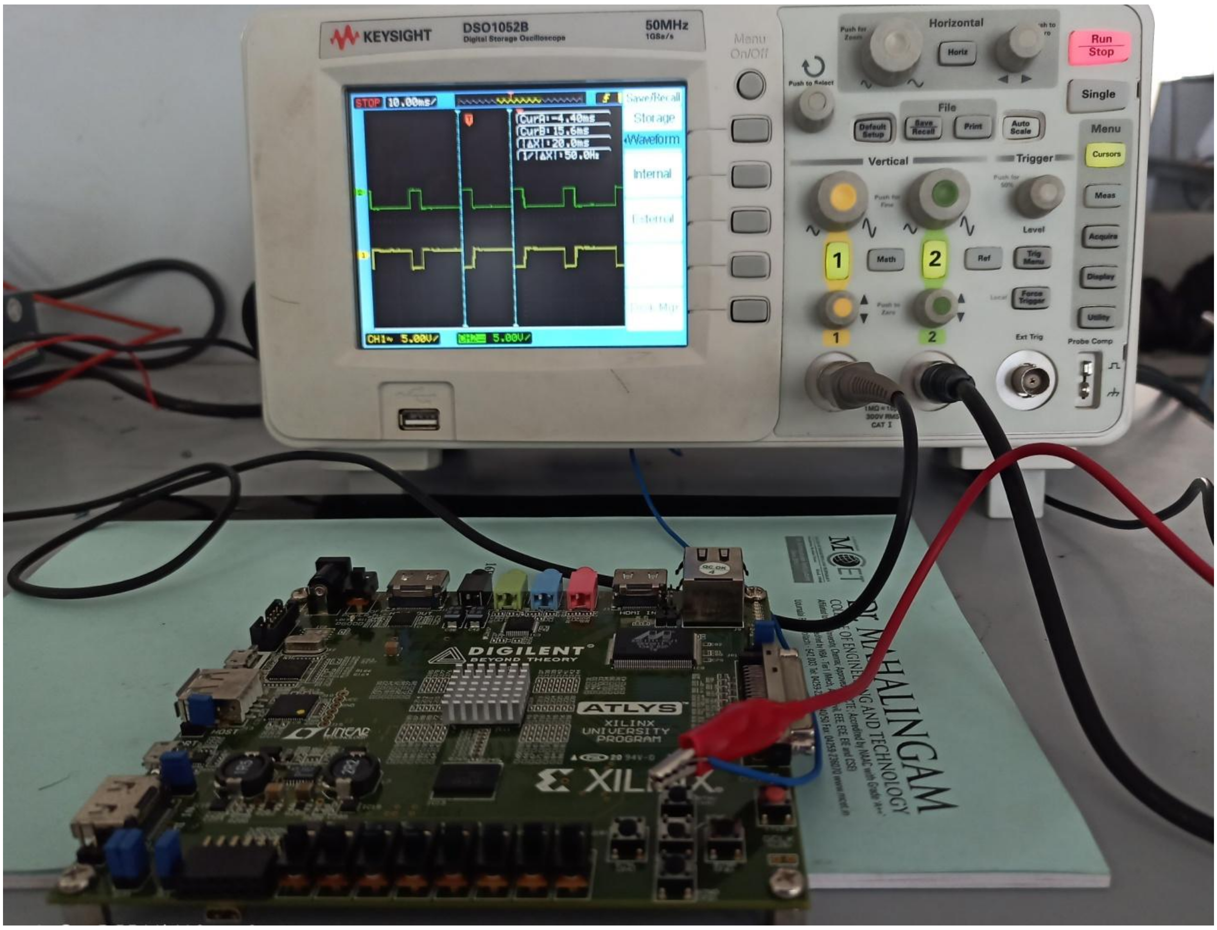

Fig. 6.1. Hardware Setup

The Fig. 6.1 shows the hardware setup for VLSI implementation of sinusoidal pulse width modulation of a single phase inverter using Xilinx Spartan- 6 FPGA is shown in figure. The VHDL code is simulated in the Xilinx software and is checked for errors. The .bit file of the error free source code is generated in the Xilinx software. The .ucf file is generated by programming using the Plan Ahead tool available in the Xilinx software to assign the ports for inputs and outputs correspondingly. The device is then configured. The ports can also be directly assigned without programming in the Plan Ahead tool. The appropriate program is browsed and loaded on to the FPGA using the Adept software of Digilent. After the programming is successful, the output is visible on the hardware setup once the power source of the Atlys board is switched ON. The ouputs can be connected to the LEDs or it can be assigned to the Pmod pins which can be connected to the DSO or CRO and the pulses generated can be viewed.

VII. CONCLUSION

The generation of pulses using SPWM technique for an inverter using FPGA is successfully implemented. The programming language used for the implementation is VHDL and the software used for simulation are Xilinx ISE and ModelSim 6.3 SE. The implementation is performed on Spartan 6 FPGA platform. The pulses for the inverter has been designed and tested using ModelSim and Xilinx software and implemented on Atlys Spartan 6 board. Experimental results are shown by interfacing a DSO with the Atlys board using Adept software of Digilent. The experimental results also match with the simulation results. SPWM technique is widely used for motor applications and power electronics control applications. This method is adopted because of the improved quality of the output waveform.

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Ms.K.Annapoorani,etal. "Implementation of Sinusoidal Pulse Width Modulation for Single Phase Inverter Using FPGA." *International Journal of Engineering Research and Applications (IJERA*), vol.10 (04), 2020, pp 26-31.