RESEARCH ARTICLE OPEN ACCESS

A Combined Low-Cost Overload and Short Circuit Protection with Automatic Reclosure for Transistorized DC Chopper

A. A. Abbas*
**(Department of Electrical Engineering & Islamic Architecture,Umm Al-Qura University, KSA*

ABSTRACT
A combined, low cost, fast acting over load and short circuit protection for power transistors with a controllable current level and traced short circuit current is proposed. The fault - either over load or short circuit - current is traced for a selected number of automatic reclosure trials up to eight trials depending on the maximum short circuit pulse time determined by the transistor manufacturer. The proposed automatic reclosure trials are intended to bypass any transient overloads. The proposed circuit was tested in a DC -to- DC converter and showed excellent response and gave reliable protection of the power transistor.
Keywords-DC choppers, protection, short circuit.

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I. INTRODUCTION

Due to the simplicity of control, fast switching times, absence of forced commutation, and smaller switching losses; the transistor has an established position in the field of power electronics applications specially in the high frequency applications of inverters and DC -to- DC converters applications.On the other hand, power transistors need a special scheme of protection against short circuit and over voltage. While over voltage is usually due to circuit inductance during the switching operation and can be eliminated by switch aid networks, overload and short-circuit protection schemes are necessary for power electronics circuits. Many schemes are presented in literatures but usually, the proposed circuits are intended and implemented for certain configuration with certain devices as illustrated in [1], [2]. Although these circuits are well designed and implemented, they are complicated and dedicated to certain configurations and devices. Here, a simplified fast acting over load and short circuit protection is proposed. The circuit was built using linear elements and is provided with a level control for the fault current and a tracing for the fault clearing. The circuit trace part is to connect and disconnect automatically the transistor's drive circuit for a certain number of trials -selected as desired- up to eight trials depending on the maximum allowable time corresponding to minimum ON time of the transistor. Each trial requires about 5.25 µs for propagation and turn off time of the transistor. The proposed circuit is intended to be applicable for different devices and it is suitable for educational purposes specially student's projects with low implementation cost.
Finally, some experimental results are presented for a transistorized DC -to- DC converter operating under different duty cycle conditions and differentnumber of protection trials.

II. SHORT CIRCIIT

It is helpful before proceeding to highlight the process of short circuit in power transistors. Fig.(1) shows the collector current (Ic), collector - emitter voltage (V_{CE}) and base drive current (I_B) under direct short circuit between the collector and emitter. Assuming that the short circuit occurs at (t1), before this instant the transistor is operated normally in the saturation region.During the period (t1-t3), the collector current increases with a rate equals to V/L where L is the inductance of the circuit under fault conditions including the stray inductance of the wires. Since the base current remains constant, the transistor is desaturated and the operating point moves from the saturation region to the linear region and as a result, the voltage V_{CE} rises to the applied DC voltage at t3.

During (t3-t4), the collector current is limited at point t3 according to the relation $I_C = H_{FE} \times I_B$.

At t4, the base current is cut-off and the interval (t4-t5), is the time required to turn-off the transistor. This period is very short due to the absence of the storage time since the transistor operates in the linear region and as a result, a very steep current decay is produced. This high rate of current changing together with short circuit path inductance results in an over shoot of collector - emitter voltage V_{CE} [3].

Finally, the time at which short circuit is detected is t2 and the period (t1-t4) is the time between fault detection and turning off the base

drive current.

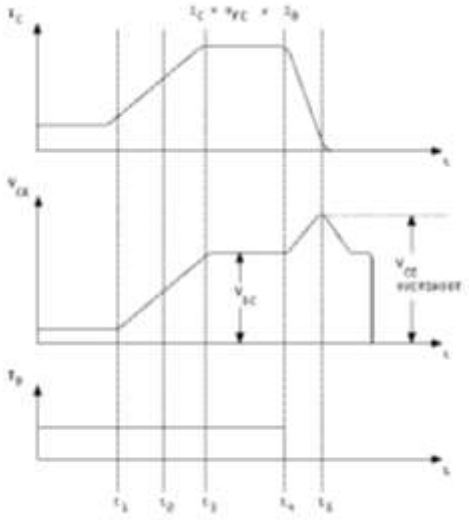

Fig.(1) I_C, V_{CE}, and $I_B$under direct short-circuit

III. SHORT CIRCIUT PROTECTION

For a reliable protection of transistors, the control circuit must be provided with an active protection against short circuit. The protection circuit has to detect the short circuit condition and turn off the transistor in a very short time. The sum of detection and operation times must be less than the short circuit pulse time given by the transistor manufacturer. From figure (1), short circuit can be detected either by monitoring V_{CE} or I_C. The first choice uses the fact that during short circuit, the operating point moves to the linear region and V_{CE} rises above the saturation voltage. The monitoring of V_{CE} can be implemented with a reference voltage set to a value slightly above V_{CE}. The drawback of this scheme is that during the turn on time - time required to change the transistor state from off state to on state- V_{CE} changes from the supply voltage to V_{CE} sat. Hence, the protection circuit must wait for the ON delay time of the transistor. During this period, short circuit cannot be detected. The second method deals directly with the collector current through an electrical isolation circuit.

IV. DESIGN CRITERIA

Because of the dead zone of short circuit detection using V_{CE} monitoring, it is better to use the collector current as the short circuit detection variable. Normally, AC or DC current transformers are used and the detected signal is processed by logic control circuit to control the pulse width until zero duty cycle (transistor ON time divided by the periodic time) is reached for solid short circuit conditions and the resultant pulse is then propagated towards the driver stage.

It should be noted that current transformer detection scheme delays the operation of the protection circuit due to;

-The current transformer time delay
-The time to change the pulse width
-The propagation time to reach the driver stage.

Our criteria in the proposed circuit is to minimize the operating time as possible. First, the current signal is taken through an opto-isolator. This choice eliminates the detection time delay accompanied by the current transformer. Second, the signal is used directly to disconnect signal of the driver stage and not processed in the control circuit. A time saving is also gained if the protection circuit elements are correctly chosen. Those elements must have high slew rate of voltage per micro-second, e.g using J-FET OP-Amps offers about 10 times faster operation than the ordinary general-purpose OP-Amps [4]. Also, solid state switches used in this application must have very short operating time and less than 1 μs; DG-200 solid state switch requires about 250 ns for operation [5]. Fig.(2) shows a block diagram of the ordinary and proposed techniques for short circuit protection.

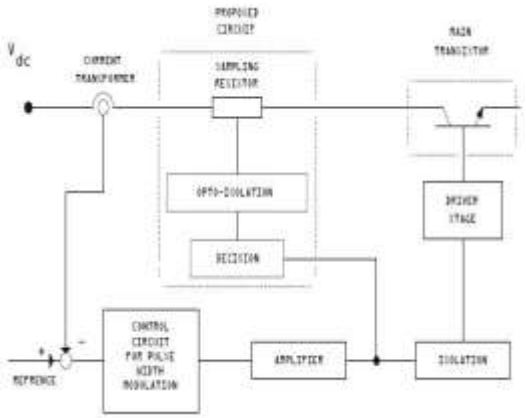

Fig.(2) Usual and proposed techniques for fault current detection

V. PROTECTION CIRCUIT

Figure (3) represents the power circuit of the transistorized DC chopper used and the locations of the sampling resistors.The DC power supply is connected to the chopper through a contactor. The contactor coil is supplied from a 220-volt AC voltage and connected in series with one normally open (N.O) contact of relay RB and one normally closed (N.C) contact of relay RA. Relay RB is used to hold the contactor of the power supply while relay RA is used to disconnect the power circuit under fault conditions by a signal from the protection circuit.

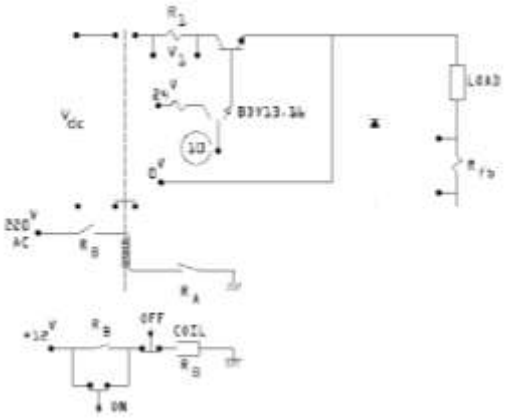

Fig.(3) Power circuit

VI. CIRCUIT OPERATIOIN

The operation of the protection circuit can be explained with the help of Fig.(4) as follows;

i. According to the specifications in [6] together with the selected resistors in both input and output sides of the opto-isolator, a voltage drop of about 1.2 volt on the photo diode terminals (2 2') of the opto-isolator will saturate the opto-isolator's transistor. Thus, by choosing the value of the sampling resistor, the current level can be selected

ii. Current scanning operation and the number of trials are chosen through one of the counter outputs and its operation is as follows;

- At normal operation each of the over current signal ($I_L x R_{fb}$) at terminal 1 or the short circuit signal (Ic x R1) at terminals (2 2') is compared with its reference value and gives a logic 1 at the output terminals 3 and 4 respectively.Hence, the output at terminal 5 is zero which is also the counter clock input.
- When a fault occurs, the signal is detected and compared with its reference. References are chosen according to the degree of saturation of the opto-isolator's transistor for short circuit current protection and the allowable current level for over load protection.
- According to fault type, either terminal 3 or terminal 4 falls to logic 0 and in accordance, the output at terminal 5 rises to a logic 1.
- As a result, the counter advances by one count and the output at terminal 6 becomes logic 0 [7].
- Since the output at terminal 6 and the base drive signal are the inputs of the equivalent AND gate (G3, G4), at fault conditions, the output at terminal 7 becomes logic 0.
- The counter output (Q1or Q2 or Q3 or Q4) performs three functions; First, it turns off the solid-state switches S1 and S2 of base drive path and light emitting diode LED indicator, respectively. Second, it actuates the relay coil of RA in the power circuit to disconnect the power supply. Finally, it holds the situation such that the circuit cannot be re-operated again unless manual reset of the counter is performed through push button (P.b -1).
- Thus, under fault conditions, if the selected number of iterations is N, where N can be 1 or 2 or 4 or 8, the base drive current signal will be zero until the fault current decreases and automatically reconnects the base current again. If the fault is cleared, the circuit will revert to its normal operation again but if not cleared, the operation of setting the base current to zero and reconnecting it will continue and each time the counter advances by one count until it reaches the pre-selected number of trials N and then both the drive signal and the input voltage are disconnected using S1 and RA.

The short circuit part of the protection circuit can also be adjusted for over load protection. This adjustment is done by setting the current level to a value smaller than the short circuit current. Under this condition, the circuit also serves for the short circuit protection.

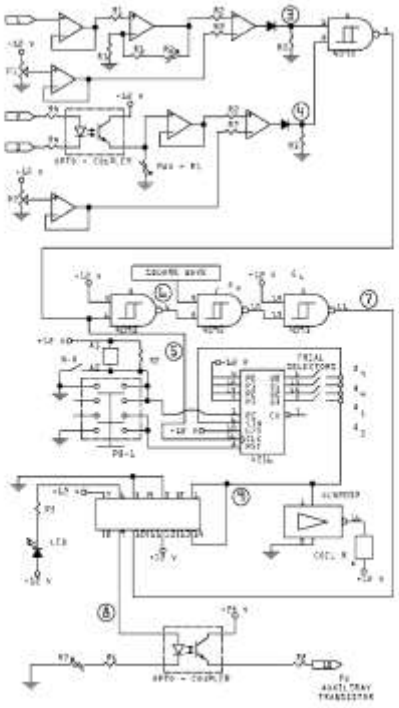

Fig.(4) Protection circuit

iii. Figure (5) represents the whole operation in a simplified flow chart

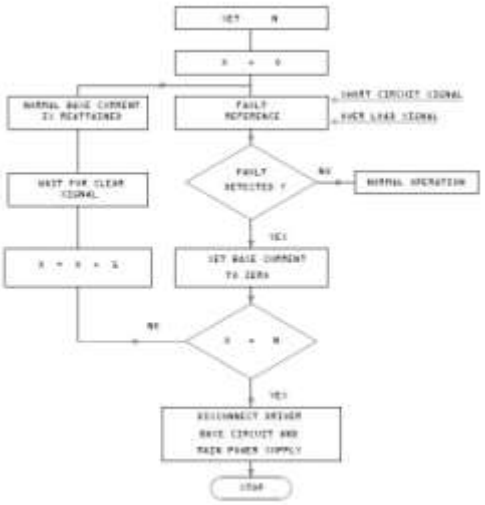

Fig.(5) Flowchart of the protection cycle

VII. EXPERMENTAL RESULTS

The circuit was built for a transistorized DC chopper feeding R L load, 80 mH, 4 Ω. It was operated and tested at 12-volt DC under over load conditions. Figures (6) to (11) show the different waveforms of the control voltage, output current, clock signal, output voltage, and collector - emitter voltage. The tests were performed at 50% ,100% duty cycle and four and eight protection trials.

7.1 OPERATION AT 100% DUTY CYCLE WITH FOUR PROTECTION TRIALS

Fig. (6) shows oscillogram for the counter clock input signal waveform and Fig.(7) shows oscillogram for the output voltage waveform. At normal operation, it must be a level DC voltage but under fault conditions, it is cut into four discontinues parts according to the preset number of protection trials.Finally, Fig. (8) shows oscillogram for the collector-emitter voltage and the delay after the fourth trial is due to the combined operating time of relay RA and the contactor.

Fig 6) Counter clock input

Fig. (7) Output voltage

Fig (8) Collector-Emitter voltage

7.2OPERATION AT 50 HZ, 50 % DUTY CYCLE WITH EIGHT PROTECTION TRIALS

Fig.(9) shows oscillogram for the output current waveform and the base drive voltage signal. Due to the load inductance, the current did not reach the fault level in the first cycle, this means that the first cycle was not detected as over load. Then eight trials of setting the base drive current to zero until complete cut-off of the power supply starting from the second cycle.Fig.(10) shows oscillogram for the output load voltage waveform with the control voltage Then the oscillogram for the counter clock signal with eight pulses is shown in Fig.(11).

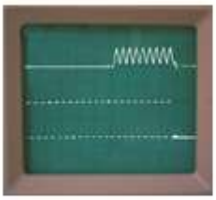

Fig.(9) Output current & base drive voltage input

Fig.(10) Output voltage& base drive voltage

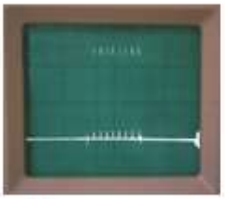

Fig.(11) Counter clock signal

VIII. CONCLUSION

Protection of power transistor, specially bipolar, is a complex task as has been shown earlier. In this paper, an over load and short circuit current protection for power transistor is presented. The short circuit current in transistors can be detected through either Ic or V_{CE}. Collector current was chosen to be the detection variable in this research for easier and more accurate detection.

The presented circuit offers an adjustable current level and a traced fault current for 1 or 2 or 4 or 8 trials, each requires about 5.25 μs to detect the fault and disconnect the base current and at the end of the last trial, it disconnects the power supply and

base current. The presented circuit is relatively simple and of low cost. It has fast response, adjusting levels in terms of over load and short circuit currents, and the number of trials. The operation of the protection circuit can be extended to inverter applications and it is suitable for both bipolar, MOSFET, and IGBT transistors

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