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Design & Implementation of 16-bit Carry Skip Adder using Reversible Computing

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ABSTRACT
Nowadays, reversible circuits are receiving immense attention because there is no loss of information bit during processing of data. These reversible circuits are better in terms of quantum cost and power consumption. This paper presents the implementation of 16-bit carry skip adder using parity preserving reversible gates. The fault tolerant full adder require to design this proposed circuit can be realized using parity preserving LCG gate and ZPLG gate. Xilinx 14.4 is used to simulate this design.
Keywords-- Reversible logic, parity preserving LCG, ZPLG, F2G, NFT, Carry Skip adder

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I. INTRODUCTION

Conventional logic circuits cannot recover the information once lost in the form of heat. R.Landauer in 1961, proved that one bit of information lost in the form of heat dissipates KTLn2 joules of energy, where k is Boltzmann's constant and T is the absolute temperature of the system [1]. But in reversible circuits, lost information can be recovered. C.H. Bennett in 1973 presented that this information recovery is possible only by using reversible logic gates in the circuit [2].

Reversible logic allows only one-to-one mapping between inputs and outputs of the circuit. Fault tolerant capability is crucial for reversible circuits, so that fault occurs inside the circuit can be detected. Parity of input and output vectors should be same to achieve the fault tolerance in the reversible circuit.

Parameters of reversible logic gates are:

i) Constant Input: Constant inputs are inputs maintained constant either at 0 or 1.

ii) Quantum cost: Quantum cost is the cost of the circuit in terms of cost of primitive gates (1*1 or 2*2). Quantum cost can be calculated by counting the number of NOT gate, CNOT gate and Controlled-V gate in the circuit [3].

iii) Garbage outputs: Garbage outputs are the unused outputs of the circuit.

Constant inputs + inputs = outputs +garbage outputs

II. SOME REVERSIBLE LOGIC GATES

2.1. F2G GATE: Double Feynman Gate (F2G) is a 3*3 gate as represented in Fig.1. Quantum cost of this gate is 2.

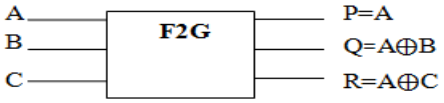


Fig.1. F2G Gate

2.2. LCG GATE: Low Complexity Gate (LCG) is a 5*5 gate as represented in Fig.2. Quantum cost of this gate is 10.

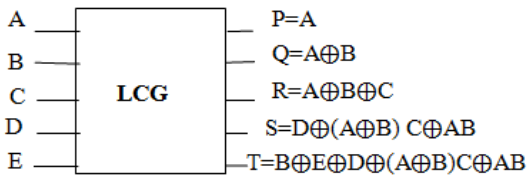


Fig.2. LCG Gate

2.3. ZPLG GATE: ZPL gate (ZPLG) is also a 5*5 gate as represented in Fig.3. Quantum cost of ZPLG gate is 8.

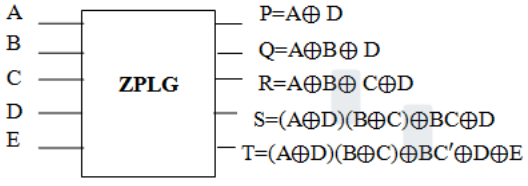


Fig.3. ZPLG Gate

2.4. NFT GATE: New fault-tolerant gate (NFT) is a 3*3 gate as represented in Fig.4. Quantum cost of this gate is 5.

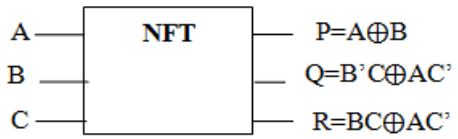


Fig.4. NFT Gate

III. LITERATURE SURVEY

Md. Saiful Islam et al. (2009**)** proposed that hardware complexity and efficiency of carry look-ahead and carry skip adder can be improved by using parity preserving IG gate. This paper presented that fault tolerant adder can be realized using this parity preserving IG gate [4].

H.R. Bhagyalakshmi et al. (2010**)** proposed a design of BCD adder using reversible SCL gate to get overflow detection in the adder. This design optimized the overall cost of the circuit [5].

Md.Selim Al Mamun et al. (2013) presented a design of reversible sequential circuits such as D latch and JK latches using proposed reversible 3*3 SAM gate. These designs improved the quantum cost, garbage outputs and delay of the circuit [6].

Ankur Sarker et al. (2014) proposed a design of fault tolerant adder and subtractor using parity preserving reversible gates. In this paper, same architecture was used for addition and subtraction. This fused addition and subtraction design had lowest complexity [7].

Neeraj Kumar Misra et al. (2015) presented designs of ripple carry adder and carry skip adder using 4*4 reversible Inventive0 gate. These designs were efficient in terms of high speed, low power and lesser complexity. These designs using Inventive0 gate were optimized as compared to existing designs [8].

Rewati D.Gatfane et al. (2015) presented a design of low power 32 bit reversible carry skip adder using MSTG gate to avoid transistor over head. Performance of carry skip adder using MSTG gate was better than the previous carry skip adders [9].

Mojtaba Valinataj et al. (2016) proposed the designs of fault-tolerant reversible adders such as RCA, CSA, CLA, BCD and CSK adder with the aim of being both low-cost and parity preserving. These adders were highly efficient in terms of quantum cost, total logical calculation and transistor count [10].

RoopShikha et al. (2017) presented that quantum cost and power consumption of ripple carry adder can be reduced by using parity preserving reversible ZPLG gate [11].

IV. PROPOSED WORK

4.1 Carry Skip Adder (CSKA) using LCG gates

Carry Skip Adder speed up the operation of the adder by allowing the carry signal to skip over several adder stages at a time.16-bit Carry Skip Adder (CSA) can be constructed using 16 LCGs, 16 NFTs and 4 F2Gs as represented below in Fig.5. LCG gate used to construct a CSKA is a parity preserving gate. Two last inputs (D and E) of LCG are set to zero to make it full adder. Quantum cost of one LCG gate is 10, F2G gate is 2 and of NFT gate are 5. Total quantum cost of CSKA can be calculated as:

Quantum cost of CSKA = n*(QC of one LCG) + n*(QC of one F2G) + n*(QC of one NFT)

where, n is the number of LCGs, F2Gs and NFTs used to construct CSA.

Total quantum cost of this proposed design of CSKA using LCG gates is 248.

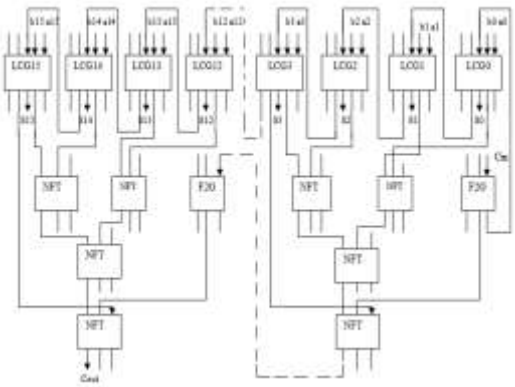


Fig.5. 16-bit CSKA using LCG gates

4.2 Carry Skip Adder using ZPLG gates

Quantum cost and power consumption of the CSKA can be improved by using ZPLG gate instead of LCG gate. ZPLG gate used to construct a CSKA is also a parity preserving gate like LCG gate. ZPLG gate acts as a full adder when its last two inputs (D and E) are maintained to zero [10].

Total quantum cost of this proposed modified design of CSKA using ZPLG gates is 216.

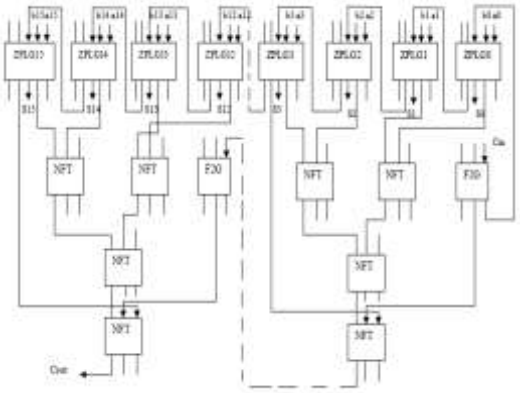


Fig.6. 16-bit CSKA using ZPLG gates

V. IMPLEMENTATION AND RESULTS

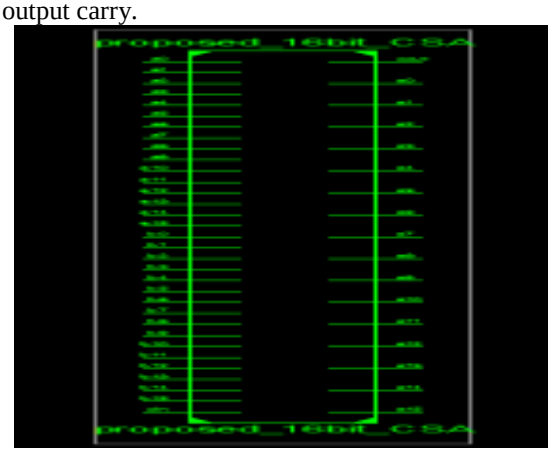
Table 1. Comparison of proposed and proposed modified 16-bit CSKA

16-bit CSKA	**Quantum cost**	**Power consumption(W)**
1st Proposed 16-bit design using LCGs	248	3.028
2nd Proposed Modified 16-bit design using ZPLGs	216	1.558

VI. SIMULATION METHODOLOGY

6.1 Simulation methodology for CSKA using LCG gates

Code for CSKA is written in VHDL language and Xilinx ISE 14.4 is used to simulate CSKA. Fig.7 shows the RTL view of proposed 16-bit CSKA. This circuit makes use of LCGs, F2Gs and NFTs. It contains inputs a, b each of which contains 16 bits and Cin as the input carry. It has output S which contains 16 bits and Cout as the output carry.



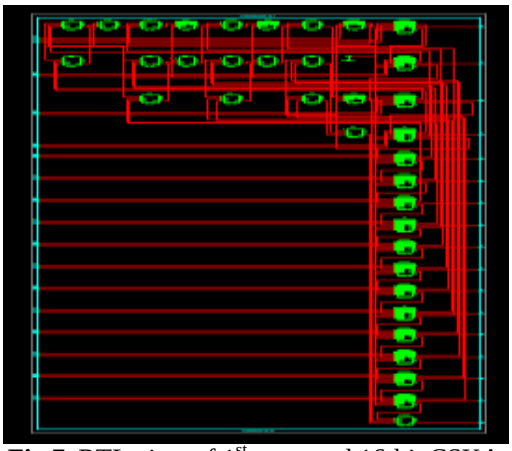


Fig.7. RTL view of 1st proposed 16-bit CSKA using LCG gates

6.2 Simulation methodology for CSKA using ZPLG gates

Fig.8 shows the RTL view of proposed modified 16-bit CSKA. This circuit makes use of ZPLGs, F2Gs and NFTs. It also contains inputs a, b each of which contains 16 bits and Cin as the input carry. It has output S which also contains 16 bits and Cout as the output carry.

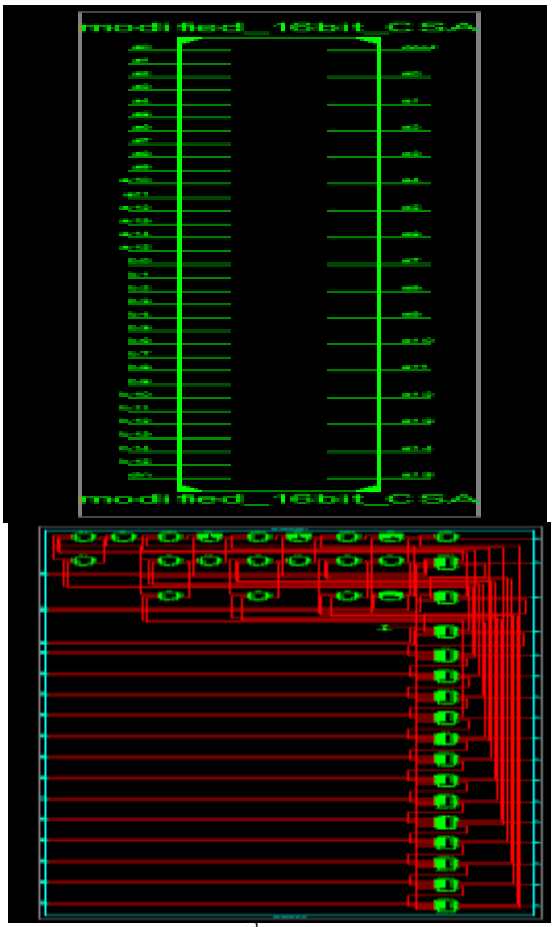
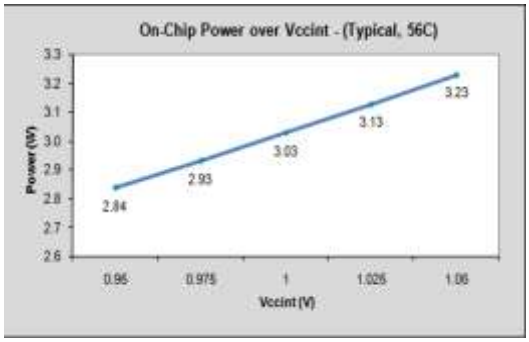
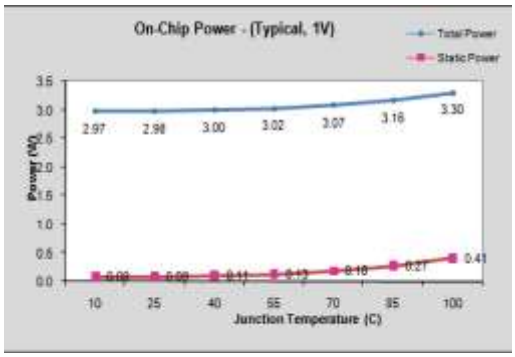


Fig.8. RTLview of 2nd proposed modified 16-bit CSKA using ZPLG gates

6.3 Power Results

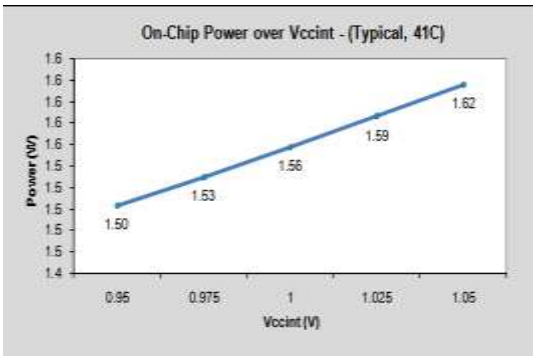


(a)

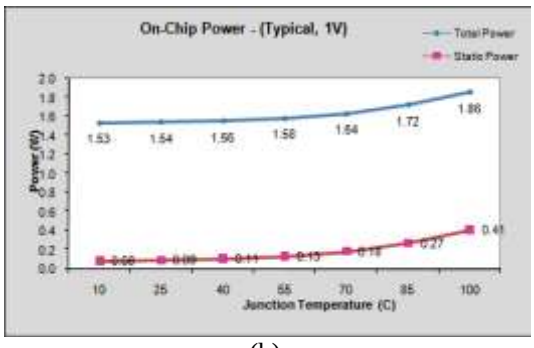


(b)

Fig.9. Graphs (a) and (b) showing power consumption for proposed 16-bit Carry Skip Adder using LCG gates

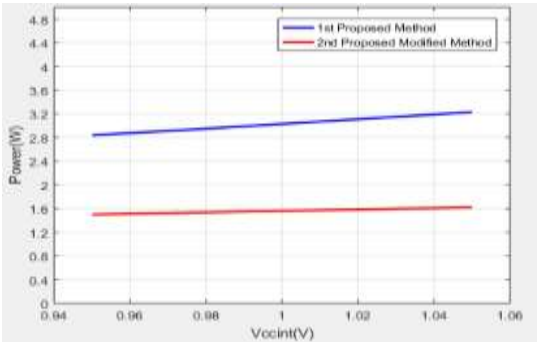


(a)

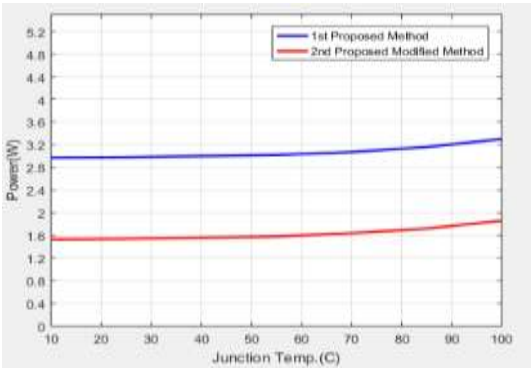


(b)

Fig.10. Graphs (a) and (b) showing power consumption for proposed modified 16-bit Carry Skip Adder using ZPLG gates



(a)



(b)

Fig.11. Comparative results of Power consumption for proposed CSKA using LCG gate and proposed modified CSKA using ZPLG gates

VII. CONCLUSION

In this paper, CSKA is presented with low quantum cost and reduced power consumption. Results of 16-bit CSKA using ZPLG gates are better than CSKA using LCG gates. For further work, these proposed designs can be extended to n-bit parity preserving adders. Other circuits such as encoder, decoder can be designed using these reversible gates.

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