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Stability Fault analysis in Sub-threshold SRAM using Wavelet transform

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ABSTRACT: Designing and testing robust SRAM memory for sub threshold systems is extremely challenging because of the reduced voltage margin and are highly sensitive to physical defects. Because of the unique architecture of sub-threshold cells, some of the detectable defects in case of conventional SRAM escape in sub-threshold SRAM cell. Therefore, stability fault analysis in sub-threshold SRAM cell is essential. In literature, various test methods have been demonstrated and all of them are based on voltage based test techniques. Voltage based test techniques may not be able to target all complete set of open defect faults; hence there is a need for parametric test method which supplement the existing test schemes. In this paper, transient current (IDDT) testing has been used as an alternative efficient testing method for both detection and localization of defective cell in an array. But since its very fast response test technique, it will be difficult to use it for online testing. Hence forth there is need for process current signal, using one of the signals processing technique. In this paper an approach of transient along with wavelet transform of the IDDT signal is proposed. By taking the wavelet transform of the transient current waveform it will be possible to cover all undetected open defect faults. The design, implementation and testing is carried using 45nm gpdk technology in cadence virtuoso EDA tool.

Keywords- 6T SRAM, 10T, Sub-threshold, IDDQ, IDDT, Stability Fault Analysis, Wavelet transforms

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I. INTRODUCTION

As the circuit complexity increases testing and localizing defects faces many challenges [17]. Sub-threshold circuits are becoming more popular in ultra-low-power applications where minimum power consumption is the major design constraint [18]. Static CMOS logic at Sub-threshold can operate while consuming very less power. But, designing and testing robust SRAM memory for sub threshold systems is extremely challenging because of the reduced voltage margin. There are various new SRAM architectures which can operate successfully at low voltage are investigated in literature. However, Sub threshold SRAMs are highly sensitive to physical defects such as resistive-open defects [15], static and dynamic Read Destructive Fault (RDF) [16], Incorrect Read Fault (IRF) and Transition Fault (TF). Resistive-opens generally cause timing-dependent faults. Resistive-open defects [16] that appear more frequently in core-cell of SRAM memories for VDSM technologies induce a modification of the timing within the memory (delay faults). The significance of resistive-open defects has considerably increased in recent technologies, due to the presence of many interconnection layers and an ever growing number of connections between each layer. In Intel reports [14] that open/resistive vias are the most common root cause of test escapes in deep submicron technologies.

Because of the unique architecture of sub-threshold cells, some of the defects which are detectable in case of conventional SRAM escapes in sub-threshold SRAM cell. Hence, detection of such resistive-open defects is the main target of this paper. The circuit of conventional (6T) SRAM cell and widely used sub-threshold SRAM cell are as shown in Fig.1 and Fig.2 respectively.

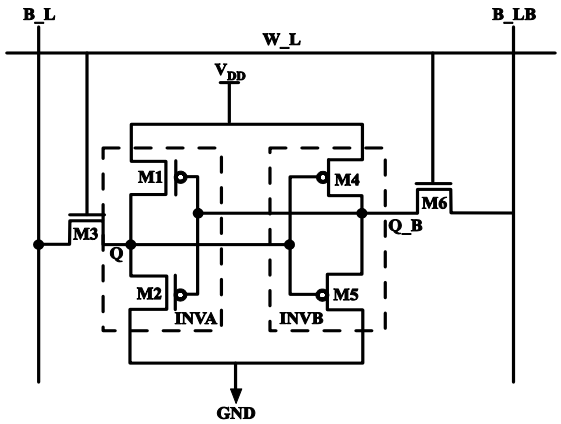


Fig.1.6T-SRAM cell architecture

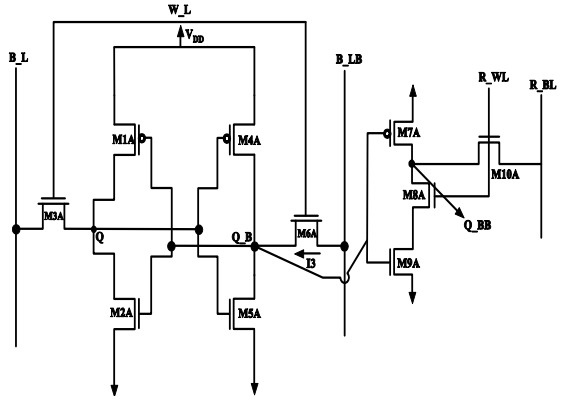


Fig.2.10T-Sub-Vth SRAM cell architecture

The stability defect analysis of conventional SRAM cell and sub-threshold SRAM is totally different. In the literature, various test methods [15,19] have been demonstrated and all of them are based on voltage based test techniques such as March Test[15], Read Equivalent Stress (RES) [19], Severe Write test[19], Low-Voltage Write/High Voltage Read[19] and data retention tests. These techniques may not be able to target complete set of open defect faults; hence there is a need for parametric test analysis. Quiescent current (IDDQ) [4] and Transient Current Testing (IDDT) [20] are two widely used parametric test schemes for defect detection [4, 20]. But IDDQ test will fail to cover most of the open defects. Moreover, IDDQ test measurements require the circuit to stabilize in the steady state resulting in additional delay, thus increasing the test time. While the many solutions have been proposed to deal with the background leakage elevation in IDDQ testing. However, transient current (IDDT) testing has emerged as an alternative or supplementary efficient testing method for both detection and localization of defective cell in an array. This technique has minimum time complexity as compared to the conventional test methods. But since its very fast response test technique, it will be difficult to use it for online testing. Hence forth there is need for process current signal, using one of the signals processing technique, in literature, FFT and DFT techniques are used. In this paper, wavelet transform is considered since Wavelet analysis has attracted attention for its ability to analyze rapidly changing transient signals. Any application using the Fourier transform can be formulated using wavelets to provide more accurately. In this paper an approach of transient along with wavelet transform of the IDDT signal is proposed. By taking the wavelet transform of the transient current waveform it will be possible to cover all undetected open defect faults.

II. STABILITY FAULT ANALYSIS

Most of the catastrophic defects cause decrease in SNM and leads in to functional failures. Such defects are easily detectable by either single read/write operation or from regular march tests. However, SRAM bit cell possess significantly high SNM for few defects and hence, the cell operates normally. Such defects escape the standard tests but result in long term reliability issues or delay faults. Such faults are known as stability faults. Here, open defects are modelled as a resistor and every possible defects are injected as shown in Fig.3. Open defects in second inverter are symmetrical, hence are not shown in figure. Some defects do alter the Static Noise Margin (SNM) of the cell and are easily detectable with simple read or write operation. However, some weak defects may not alter SNM and left undetected during testing. Therefore, for all possible defects shown in figure, the minimum detectable resistance (R_{def}) which cause failure in the cell is recorded in table1.

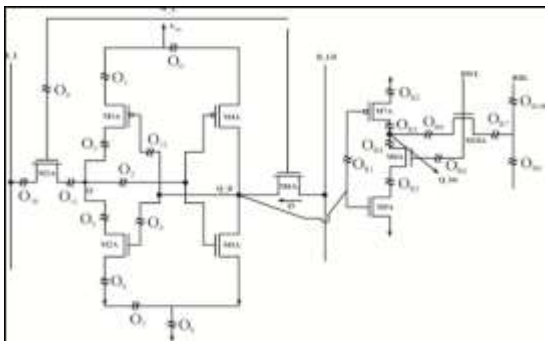


Fig.3. Possible open defects in sub-threshold SRAM cell

To find R_{def} for each defect, the following procedure is followed.

- A defect is modeled with connecting a resistor R_{def}.
- Initially set the resistance value to be very high ($\approx 500G\Omega$) and Read/Write operations are observed. If the defect does not cause failure, then minimum detectable resistance is recorded as infinite.
- Then, the R_{def} is varied up to 10 KΩ in logarithmic scale and each time Read/Write operation is performed and this is continued until read or Write failure is observed. The R_{def} which cause read or write failure is recorded as minimum resistance for the defect.
- An open defect with resistance value below the recorded minimum detectable resistance is considered as stability faults.

Some defects are highlighted in grey colour and they have very high minimum detectable resistance. Such defects are called hard to find defects or severe defects.

A. SFs in conventional (6T) and Sub-threshold SRAM cell

Defect on source/drain of driver transistor is easy-to-find defect in 6T-SRAM cell shown in Fig1. But, 10T memory cell utilizes separate path for read and write operation. Hence, weak pull down ability of driver transistor (due to defect) does not affect the voltage level of bit-line. Thus, in 10T-SRAM cell detection of open defect on drain/source terminal of driver transistor is more significant. Open defect located on gate of the access transistor is detectable only for the resistance value which is greater than or equal to 365MΩ. Any open resistance value which is less than this value will not cause any failure in the cell. For this defect, 365 MΩ is recorded as minimum detectable resistance. Fig.4 shows the schematic of 10T cell with open defect on gate of access transistor injected. Fig.5 and Fig.6 shows the write waveforms of the cell with defect resistance of 100 MΩ (less than the minimum resistance) and 400 MΩ (beyond the minimum detectable resistance) respectively. From the simulation, it is observed that write failure is observed for all resistance which is above to minimum detectable resistance (365 MΩ).

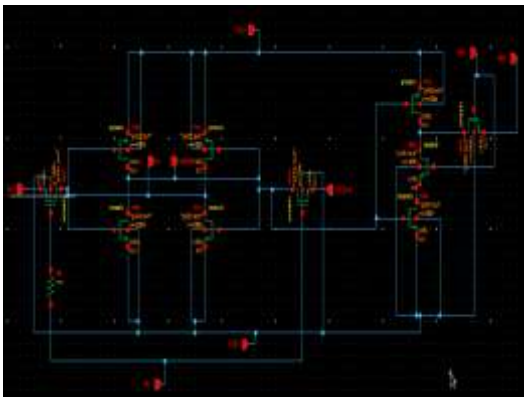


Fig.4. Open defect injected on gate of access transistor

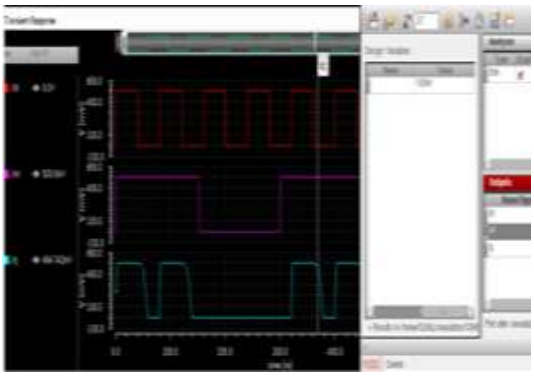


Fig.5. Write waveforms of the cell with Defect injected on gate of access transistor R_{def}= 100 M

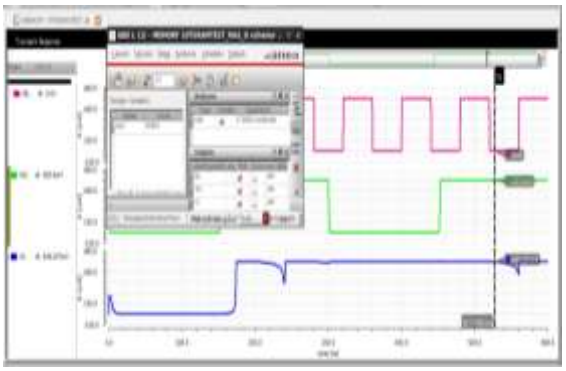


Fig.6. Write waveforms of the cell with Defect injected on gate of access transistor R_{def} = 400 M

Table 1. Stability faults in 10T sub-Vth Design

Transistor	Terminals	Faulty behaviour	Minimum detectable resistance (R_{def})
M3A	G	Write 0 Fail	365 MΩ
	S/D	Write 0 Fail	3.8MΩ
M6A	G	Write 1 Fail	500 MΩ
	S/D	Write 1 Fail	3.6MΩ
M1A	G	Write 0 Fail	1G MΩ
	S/D	Write 1 Fail	60MΩ
M4A	G	Write 1 Fail	1GΩ
	S/D	Write 0 Fail	60 MΩ
M2A (driver)	G	Write 1 Fail	220 GΩ
	S/D	No failure	100 GΩ
M5A (driver)	G	Write 0 Fail	220 MΩ
	S/D	No	100 GΩ

		failure	
MA7	G	Read0 fail	330 MΩ
	S/D	Read0 fail	3.8 MΩ
MA8	G	Read0 fail	180 MΩ
	S/D	Read0 fail	14 MΩ
M9A	G	Read0 fail	3 GΩ
	S/D	No failure	100 GΩ
M10A	G	Read0 fail	180 MΩ
	S/D	Read0 fail	3.8 MΩ

From the table 1, it can be observed that most of the defects possess high R_{def} (in Mega ohms). Hence all of the weak defects left undetected. But, in Deep sub-Micron (DSM) technologies, probabilities of occurrence of weak defects are very high. Therefore, to supplement voltage based test technique, a current based IDDT technique is applied here in order to decrease the minimum detectable resistance.

B. Capability of Severe Write (SW), RES and LVW/HVR tests

Stability faults listed in table 1 are now considered to reduce their minimum detectable resistance. From literature, it is observed that March test can be applied to increase the defect detectability. However, as application of March test algorithm is time consuming. Therefore, for better test efficiency, stress based test methods like Read Equivalent Stress (RES), Severe Write (SW); Low-voltage Read/High voltage Read techniques are applied. Minimum detectable resistance obtained from these test methods for the defects which are highlighted in table1(with grey colour) are recorded in table 2. For all defects, lower minimum detectable resistance was observed. Details of these advance test techniques are discussed in [13].

Table 2. Effectiveness of RES, SW, LVW/HVR Test methods on 10T cell

Transistor Terminal	Minimum detectable resistance ($R_{Min-det}$)			
	W + R	RES	Severe write	LVW/ HVR
M_{2A}/M_{5A} (S/D)	100G	500 M	4.3 M	∞
M_{2A} (Gate)	220G	44M	∞	∞
M_{9A} (S/D)	300M	340M	∞	∞
M_{9A} (Gate)	100M	40M	∞	∞

From table 2, we see that although, the minimum detectable resistance is reduced to some extent, it remains still in Mega ohms range.

III. CAPABILITY OF I_{DDT} TESTING

In sub-threshold SRAM cell, there are few defects those left undetected during testing (depending on their value) and usually may affect the dynamic current consumption in some way. In presence of defects, one or some of the parameters of the transient current waveform shown in Fig.8 may change and which is compared with the threshold value set by the golden cell to know the presence of defect. Parameters of the current waveforms which can be considered for fault detection are 1) waveform width at a given value of current 2) The charge provided by the waveform 3) The peak value OF the waveform 4) The time at which the waveform reaches its peak value and 5) the average value of the waveform.

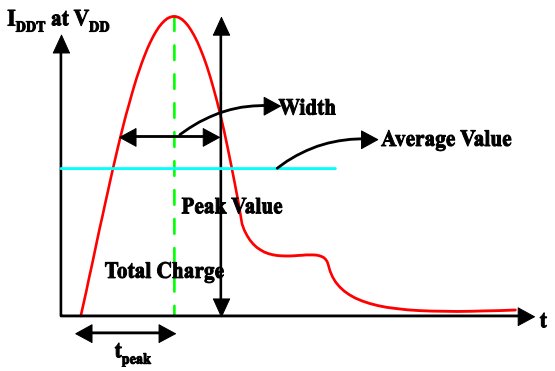


Fig.7.I_{DDT} waveform of fault free 6T-SRAM Cell

In I_{DDT} approach all possible open defects (one at a time) on each terminal of transistors are injected and power supply current is measured while cell is switching. Here also defect is injected in terms of connecting a resistor. The resistance value is varied from 10 GΩ to 10 kΩ and minimum resistance value at which current deviates from that of the good circuit is reported. The method used to decide whether the

Circuit under Test (CUT) is faulty or not is by monitoring the power supply current during switching. If variation in peak I_{DDT} waveform is more than an empirically set threshold value (≈10%), the circuit is considered faulty. The simulations are repeated for various Cell Ratio (CR) and Pull Up Ratio (PUR) [5] and IDDT test efficiency was verified. The charge carried by the signal is highly efficient for strong defect detection but except for weak defects. However, peak of the current signal has comparatively high efficiency for weak defects also. Therefore, for defect detection in memory array, peak of the current waveform is used.

Fig.7 shows the I_{DDT} waveform measured 10T cell by injecting resistive open defect on gate terminal of pull-up transistor. For the defect free cell, a transient current of 26 nA was observed. As the resistance value increases, the magnitude of the transient current increased abnormally. Moreover, the time at which the transient reaches its maximum also differs. Also there is a deviation in the average value of the current of the good and faulty circuit. A current deviation of 10 percent is set as a threshold value by taking process variations into account. Here, dynamic current variation of 10% is observed with respect to the variations in threshold voltage. The reason why only threshold voltage is considered to set the threshold is that in sub-threshold region, threshold voltage has highest impact on current. Test was conducted for all possible open defects in the cell. I_{DDT} results for stability faults in 10Tcell is tabulated in table 3. The results show that, this method reduces the minimum detectable resistance to larger extent. Further, this technique is used to locate the faulty cell in memory array.

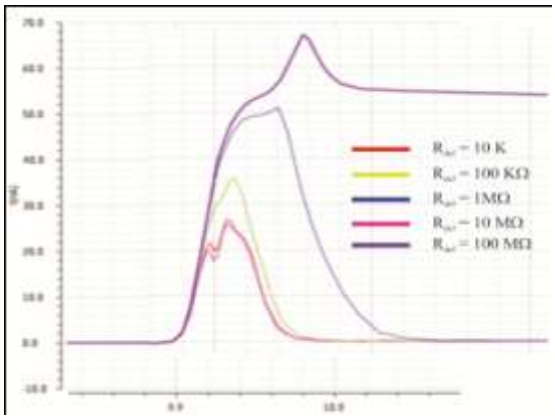


Fig.8. Transient current waveforms for different defect severity for gate open defect (M2A)

Table 3. Minimum detectable resistance recorded for hard to find defects in 10T SRAM.

Transistor	Terminals	$R_{Min-det}$
M_{2A}	(S/D)	28K
	G	18K
M_{5A}	(S/D)	28K
	G	18K

A. Localization of faulty cell in memory array

A 64-bit Sub-V_{th} SRAM array which woks under normal and test mode is depicted in Fig. 9. In test mode, all bit lines get disconnected from pre-charging circuitry and the data is written on to first cell which will be given as an input to the next cell. Thus, each bit-cell in an array is driven by previous cell. Thus, the switching activity taking place in each cell results in transient current spike at V_{DD}. It means that an array which has n number of cells causes n number of spikes in I_{DDT} waveform measured at V_{DD}. Thus, the total number of spikes at I_{DDT} waveform straightaway indicates number of cells in an array. The I_{DDT} waveform obtained for 64-bit fault free array is depicted in Fig. 10(a).

Next, one of the cells in an array is replaced by faulty cell. During test mode, when the data is written on to first cell, it activates a fault in particular depth and causes abnormal increase in transient current spike of the faulty cell. The time at which the I_{DDT} spike deviates from the good circuit depends on the depth at which the defect resides. The response of good circuit is stored in signature library and the current measurements are made using Built in Current Sensors (BICs). If an applied stimulus activates a fault in some depth, it is reflected as abnormal transient at supply current. By measuring the time, at which the current waveform of the faulty array deviates from that of the good cell, the depth at which the fault is located can be known. This information can be used by the Fault tolerance unit which can make decision to replace faulty cell with redundant cell.

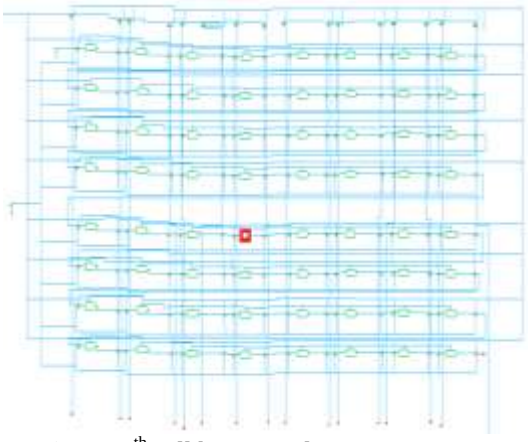
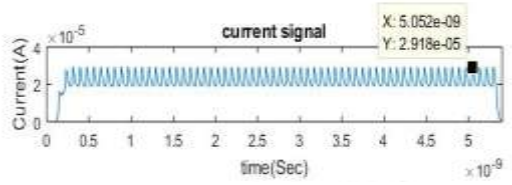


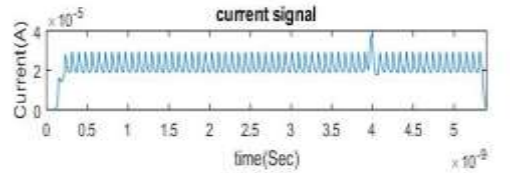
Fig.9. 36th cell being Faulty in 8 × 8 Array

Fig. 10(b) to 10(e) represents I_{DDT} waveforms of the array, when various defects are injected at different levels. the gate terminal of pull-up transistor of 47th and (27th and 58th) cell respectively. The current waveform obtained when the open fault is injected at drain terminal of the load transistor of 5th

cell and at gate terminal of the load transistor of 27th cell is depicted in Fig. 10(d). Whereas Fig. 10(e) is the waveform obtained by injecting gate open with defect resistance which is equal to 100MΩ at gate terminal of the driver transistor of 47th cell. Each spike in the waveform corresponds to transient current drawn by each cell when data transition is taking place. For example, 5th spike corresponds to transient current measured at the power supply, while data is writing in 5th cell. From Fig. 10, we observe deviation in transient current of the faulty cell. Thus, by comparing the magnitude of the transient at each spike with that of the golden cell, defect can be detected and by determining the time at which the deviated current from that of the golden cell is noticed, the exact location of the defect can be recorded. Although, I_{DDT} waveforms in time domain can be used for detection and localization of SFs, as I_{DDT} current is a very fast action [], sensing and processing is extremely difficult. Hence, signal processing techniques such as Fast Fourier Transform (FFT) and wavelet transforms (WT) are used for signal analysis. The resistive open defects are injected at different location with different strength. Then the current signal drawn from the power supply of the memory array is taken offline and processed through FFT and WT. The WT is highly effective in transient signal analysis as it allows the use of variable window length. Unlike FFT, WT facilitate to analyse localized part of the signal. Hence WT is useful in analysing the part of the signal which has shoot-ups and discontinuities. Therefore, for the present work WT is more appropriate.



(a)



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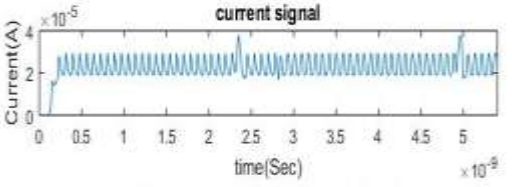

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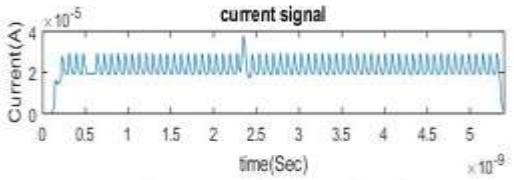

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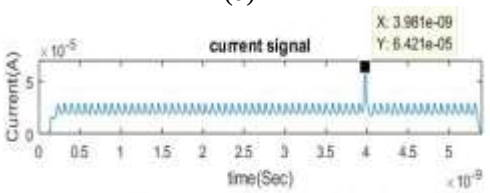


(e)

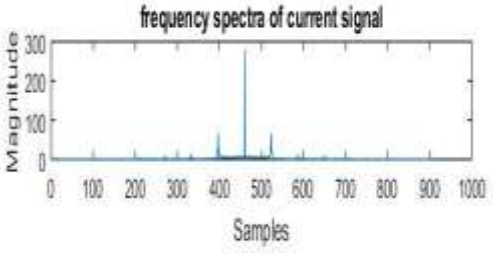
Fig.10.Transient current (I_{DDT}) waveforms for a) Fault free array b) Gate open fault at 47thc) Gate open fault at 27th and 58th cell d) Source/Drain open at 5th cell and Gate open fault at 27th cell e) Gate open with 100MΩ at 47th cell

B. Applying Signal processing techniques on obtained IDDT waveforms

Although, IDDT waveforms in time domain can be used for detection and localization of SFs, as IDDT current is a very fast action, sensing and processing is extremely difficult. Hence, signal processing techniques such as Fast Fourier Transform and wavelet transforms are used for signal analysis. The resistive open defects are injected at different location with different strength. Then the current signal drawn from the power supply of the memory array is taken offline and processed through FFT and WT.

C. Effectiveness of FFT in fault detection

The frequency spectrum of the golden array is shown in Fig.11 (a). The frequency spectrums of the current response for various defects are shown in Fig.11 (b) to Fig.11 (e). From the current waveforms depicted in Fig.11, we observe that though there is a deviation in the signal amplitude, change in frequency is very small. Therefore, FFT will not give useful information about the defect location and its severity. But, we can observe the deviation in magnitude at dominant frequency components of the faulty array and golden array. Therefore, FFT of the obtained current waveform tells only about the presence of the fault but fail in localizing the defects.



(a)

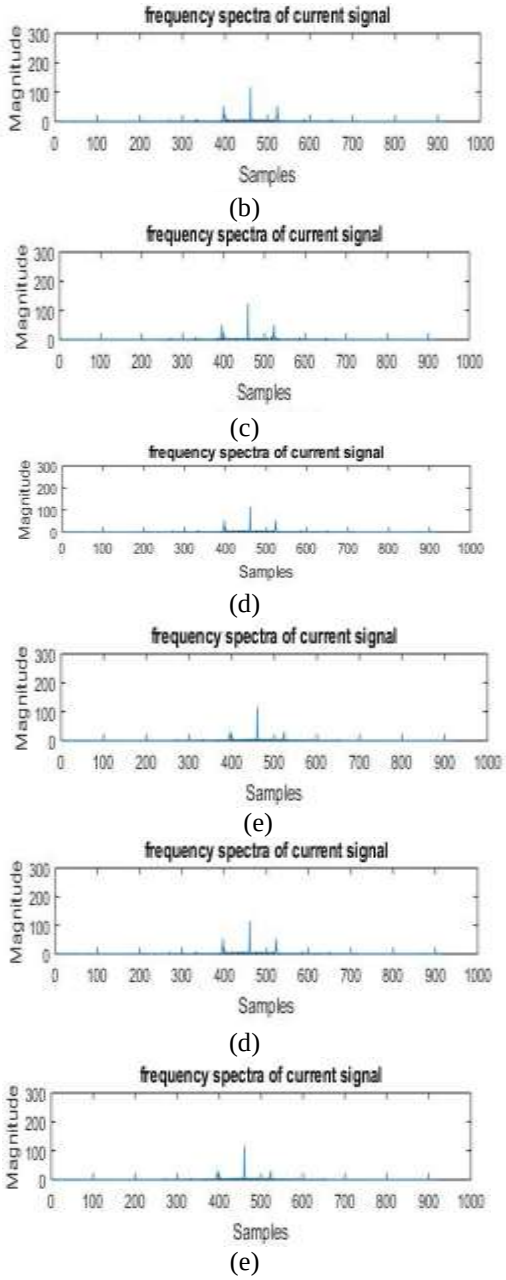
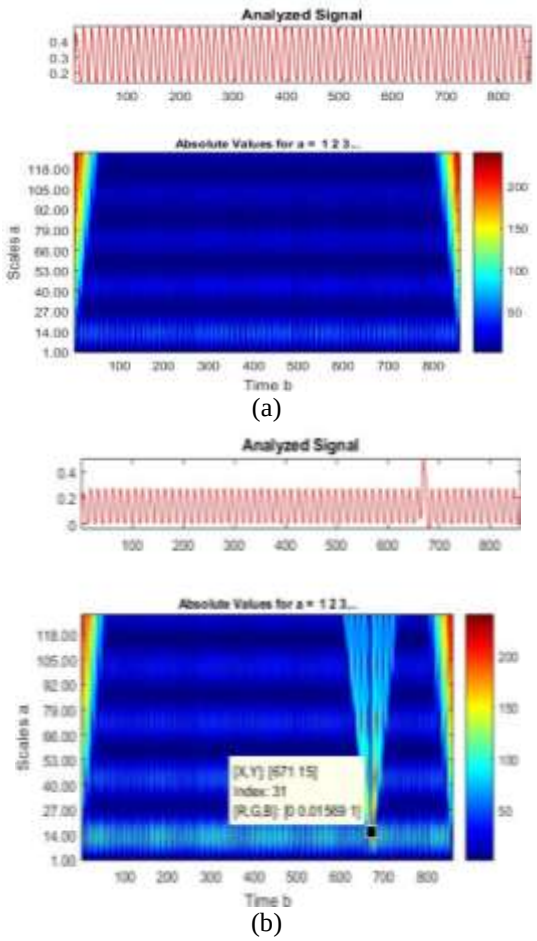


Fig.11. Corresponding frequency spectrum of current waveforms shown in Fig.10.

D. Capability of WT in fault detection and localization

The WT is a mathematical process that decompose the original signal in to time and frequency components. The signal is decomposed in to its constituent wavelet –sidebands. Such levels represent the section of the signal occurring at that particular time in that frequency band. All of the individual frequency bands are logarithmically spaced. Whereas, in case of FFT, they are uniformly spread. When interpreting CWT coefficients, cone of influence (COI) has significant role. It gives information about the CWT coefficients which are affected by the signal value at that point. Abrupt changes in a signal changes in a signal produce relatively large wavelet coefficients centered on the discontinuity at all scales. Fig.12 demonstrates the capability of WT in detecting and localizing the defects. A plot of the wavelet coefficients of golden cell is shown in Fig.12 (a). The wavelet coefficients for various defects at different level are given in Fig.12 (b) to 12(e). We know that the signal feature that wavelets are very good at identifying is a discontinuity or singularity. In the waveforms shown in Fig.12 (b) to 12(e), we can observe that the abrupt transitions in the faulty current waveforms result in wavelet coefficients with large absolute values. Now, consider the array in which 47th cell is faulty and corresponding wavelet coefficient plot is shown in Fig.12 (b). Here, we see that the set of large CWT coefficients is concentrated in a narrow region in the time scale plane centered on point 675. This region is referred to as the cone of influence of the point t=675 for db1 wavelet. Depending on this point, defect can be located. The entire current signal has 920 samples. Hence, around 15 samples correspond to one cell. If the cone of influence is between t=1 to 15, then the fault is in 1st cell. Thus t=675 indicates that in an array of 64 cells, 47th cell is faulty. The similar results are obtained for various cases shown in Fig.12 (c) to Fig.12 (e).



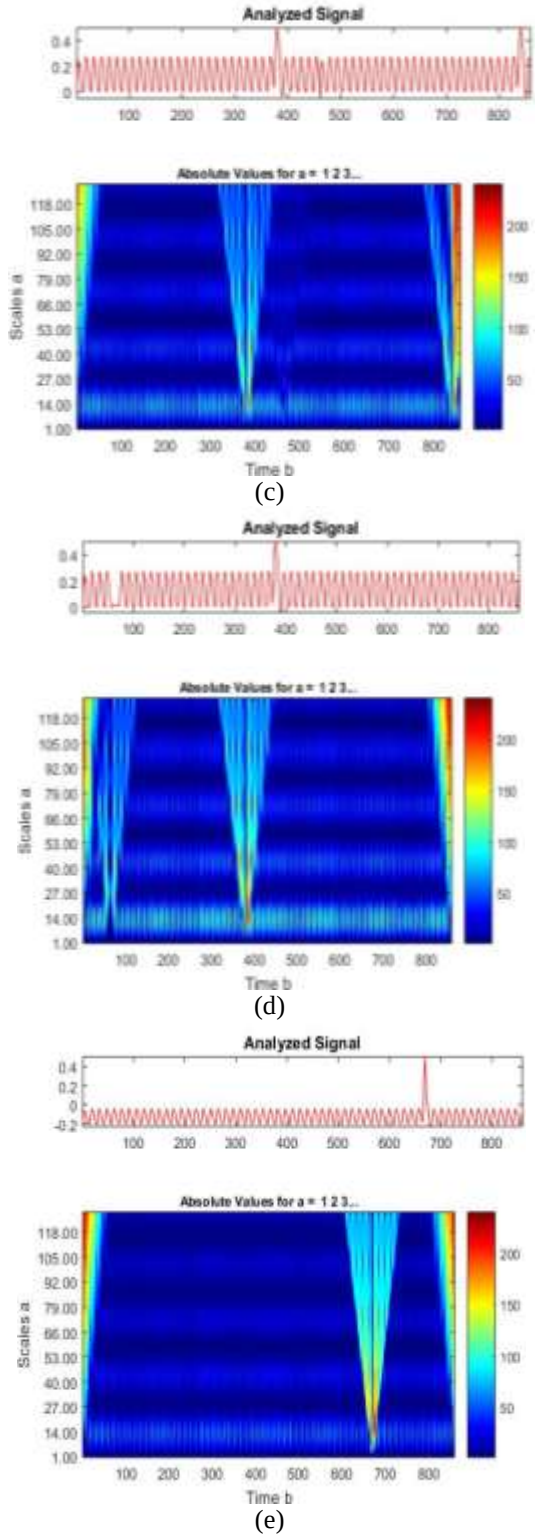


Fig.12.Wavelet Coefficients (a) no defect (b) gate open defect with Rdef = 100 KΩ at 47th cell (c) gate open defect with Rdef = 100 KΩ at 27th cell d) Drain open defect with Rdef = 100 KΩ at 5th cell and gate open defect with Rdef = 100 KΩ at 27th cell e) gate open defect with Rdef = 100 MΩ at 47th cell

E. Detection of severity of the defect

The severity of the defects can also be known by color encoding. The results discussed in previous section showed that magnitude of the spikes increases for increased defect resistances. In the wavelet coefficient plots, we can see that the magnitude of the spikes directly reflects on coefficients values. With the help of color coding one can know the severity of the defect. For example, Fig.12 (b) and Fig.12 (e) are the plots with defect of 100 KΩ and 100 MΩ respectively. Compare to first case later plot has highest coefficient value at t = 975.

Another way to find the severity of defect is through Performance Index (PI) called power spectral density of the processed defective signal. From the original current waveform, a part of the signal which corresponds to faulty cell is processed through FFT and WT to calculate the Power Spectral Density (PSD). The PSD values for drain/source terminal of driver transistor was observed to be smaller than the golden cell and PSD of gate open found to be high compared to PSD of the golden circuit. The severity of defect is measured with the injected resistance value.

Table.4. PSDs for gate open defect using FFT and WT

Defect Resistance	Gate Open (M2A/M5A)		Drain open (M2A/M5A)	
	PSD using FFT	PSD using WT	PSD using FFT	PSD using WT
No fault	7.5715 e-08	5.2462	0.3515e -08	5.2462
10 K	8.1343 e-08	5.2268	0.41343 e-08	4.9268
100 K	1.3362 e-07	5.3757	0.63362 e-07	2.346
1 M	2.8858 e-07	4.8536	0.87858 e-07	1.845
10 M	4.8117 e-07	4.1010	0.92117 e-07	0.856

PSDs for gate open defect using FFT and WT are given in table 4. The 4th column of table 4 gives the percentage deviation in PSD values of faulty signal for various fault resistances using FFT. The fifth column gives the percentage deviation in PSD values of faulty signal for various fault resistances using WT.

IV. CONCLUSION

The proposed architectures which utilizes transient current testing method along with WT to detect faults in SRAM array. The transient currents of faulty cells vary significantly from that of fault free

cells, enabling the detection of all kinds of faults. PSDs for gate open defect using FFT and WT is calculated and are compared. It can be observed that the PSD values obtained using WT are clearly distinguishable from fault free cell. Hence, WT is effective signal processing technique for not only detection and localization of the defects but also to find the severity of the defect.

REFERENCES

[1]. A. Ney, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, M. Bastian, And V. Gouin, "A New Design-For-Test Technique For SRAM Core-Cell Stability Faults," Proc. Design, Automation and Test in Europe Conf. and Exhibition, 2009.

[2]. Michel linder and Alfred Edler," An Analysis of Industrial SRAM Test Results - A Comprehensive Study on Effectiveness and Classification of March Test Algorithms". IEEE Design test conference 2014.

[3]. A. Pavlov , m. sachdev and J Pineda de gyvez, "Weak cell detection in deep submicron SRAMs: A programmable detection technique", IEEE journal of Solid state circuits (JSSC), pp. 1-10

[4]. Chin- Wen Lu, " Is IDDQ Testing Not Applicable For Deep Submicron VLSI In Year 2011?", Proc IEEE, January 2010.

[5]. Gábor Gyepes, Daniel Arbet, Juraj Brenkus And Viera Stopjaková 2011 "Comparison Of IDDT Test Efficiency In Covering Opens In Srams Realised In Two Different Technologies".2011 IEEE 14th International Symposium on April 2011.

[6]. Shuyan Jiang, Yongle Xie, Dajin Yu, "Experiment And Simulation Of Transistor Level Fault Model Of IDDT Test", Proc.of 2009 IEEE Conference On Applied Super Conductivity And Electromagnetic Devices, 2009.

[7]. R. B. Jadeja, S. A. Kanitkar, and Anurag Shyam, "FFT Analysis of a Series Loaded Resonant Converter-Based Power Supply for Pulsed Power Applications", International Journal of Plasma Science and Engineering Volume 2008, Article ID 284549, 5 pages doi:10.1155/2008/284549

[8]. K. Muhammad, M E. Amyeen, K.Roy, " Fault Detection and Location Using IDD Waveform Analysis" work supported in a part by DARPA and NSF career award- 2015

[9]. P. G. Alberto Bosio, Luigi Dilillo, Advanced Test Methods for SRAMs. Springer US, 1st ed., 2010.

[10]. D. M. Kwai, H.W. chang, H.J. Liao, C.H. Chiao, "Detection of SRAM stability by lowering array supply voltage", in proc. Of ninth Test Symposium (ATS 2000), December 2000, pp. 268-273.

[11]. Ukil, A. & R. Zivanovic "Abrupt change detection in power system fault analysis using wavelet transform. International Conference on Power Systems Transients", Montreal, Canada.June. 19-23.

[12]. Ray, P. K., H. C. Dubey, S. R.Mohanty, N. Kishor, & K. Ganesh (2010). Power quality disturbance detection in grid-connected wind energy system using wavelet and S-transform, IEEE ICPCES,1-4.

[13]. Ohileshwari M S, AnandaThirtha B Gudi," Detection of Stability Faults in Sub-threshold SRAM cell Using IDDT Waveform", Proceedings of the 2nd International Conference on Inventive Systems and Control (ICISC 2018) ISBN:978-1-5386-0807.

[14]. W. Needham et al., "High Volume Microprocessor Test Escapes – An Analysis of Defects Our Tests are Missing", Proc. Int. Test Conference, 1998, pp. 25-34.

[15]. Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, "Resistive-Open Defects in Embedded-SRAM core cells: Analysis and March Test Solution" 13th Asian Test Symposium, November 15-17, 2004

[16]. R.D. Adams and E.S. Cooley, "Analysis of Deceptive Destructive Read Memory Fault Model and Recommended Testing", IEEE North Atlantic Test Workshop, May 1996.

[17]. Ohileshwari M S, AnandaThirtha B Gudi, "IDDT-Based Fault Detection and Localization in 10- T Sub-Threshold SRAM Memory Array" International Journal of Scientific Engineering and Research (IJSER) ISSN (Online): 2347-3878, Volume 5 Issue 10, October 2017

[18]. Tae-Hyoung Kim, Jason Liu, John Keane, Chris H. Kim, "A 0.2 V, 480 kb Subthreshold SRAM With 1 k Cells Per Bitline for Ultra-Low-Voltage Computing", IEEE Journal Of Solid-State Circuits, Vol. 43, No. 2, February 2008

[19]. Chen-Wei Lin, Hung-Hsin Chen, Hao-Yu Yang, Chin-Yuan Huang, Mango C.-T. Chao, and Rei-Fu Huang, "Fault Models and Test Methods for Subthreshold SRAMs", IEEE Transactions On Computers, Vol. 62, No. 3, March 2013

[20]. Masahiro Ishida, Dong Sam Ha, Takahiro Yamaguchi, Yoshihiro Hashimoto, and Tadahiro Ohmi, "IDDT Testing: An Efficient Method for Detecting Delay Faults and Open Defects", IEEE International Workshop on Defect Based Testing, April 2001.Los Angeles, CA, USA

Ohileshwari"Stability Fault analysis in Sub-threshold SRAM using Wavelet transform "International Journal of Engineering Research and Applications (IJERA) , vol. 8, no.7, 2018, pp.38-46