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Optimized Design of Switched-Capacitor (SC) Integrator

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ABSTRACT
In this paper we present an optimized design of classical switched capacitor integrator (SC). The operational amplifier utilized in this design implementation is a two stage operational amplifier and a differential folded cascode amplifier. Therefore there is important role of capacitors used in design implementation. Optimal switching technique is used in this paper. It is also shown that the average power consumption is less and also the area is calculated depending upon the design of amplifier used. The paper is implemented using 0.18µm CMOS technology.
Keywords: Folded Cascode, tow-stage amplifier, SC integrator, noise, area.

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I. INTRODUCTION

The Switched-Capacitor circuits has, an amplifier, as the most power consuming component, which also is the most essential component in various applications. gSwitched-capacitor circuit is as shown in fig. 1, where a total of three switches are used in the circuit to control the op amp operation. C_1 is connected to V_{in} via S_1 and to ground via S_3 and unity-gain feedback is provided through S_2 [1].

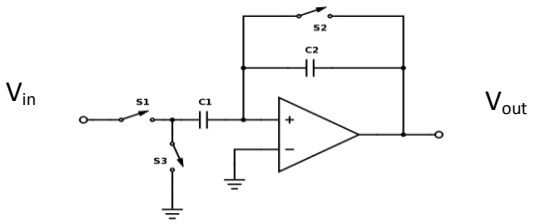

Fig. 1 Switched-capacitor amplifier

Unity gain feedback is provided by S_2. Firstly large open-loop gain of the amplifier is considered and then the circuit is studied in two phases. These two phases are termed as sampling mode and amplification mode. The idea of relizing a basic switch is using a single nMOS and pMOS. Placing a transmission gate is also a way to improve the performance which ensures low ON resistance . The basic building block of various applications, such as loop filter of Discrete-time(DT) ΔΣ modulator, is Switched-Capacitor Integrator. In CMOS technology power consumption miniaturization and speed enhancement has been crucial aspects in design considerations of analog signal circuits. Also, the basic building block of analog and mixed signal circuits are operational amplifier. In sub-micron technologies the operational amplifiers suffer from limited swing and dynamic range, low gain, high power consumptions, low stability and compensation considerations, larger chip area, etc. [2]-[5] Now, the question arises is how the circuit behaves as an integrator finds a sophisticated answer in different ways. On analyzing the ”traditional” circuit it can be noticed that the transfer function in that case would be

$$H(s) = -\frac{1}{sR_1C_2} \quad (1)$$

We know that division in the time domain means integration in the time domain. In precision, if we analyze back all the simplest integrator reasoning on the currents as shown in fig. , voltages and the charges, we can write here as

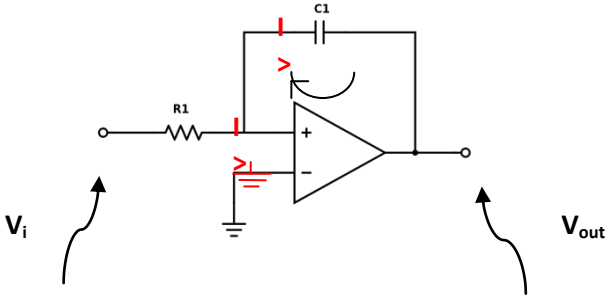

Fig. 2 Simple Integrator working

Voltage-charge relationship of capacitor together with the definition of current applied to the working of circuit configuration where a virtual ground adds to the presence and working of operational amplifier, which can be easily derived as equation (2) and (3),

$$I(t) = {}^{dQ(t)}/_{dt} \xrightarrow{Q_c(t)=C_2V_c(t)} I(t) = C_2\frac{dV_c}{dt}dt \xrightarrow{V_c=-V_o} I(t) = -C_2\frac{dV_o}{dt} \quad (2)$$

The current at the input of the op-amp circuit is similar to the current I(t) that flows across the capacitor, hence

$$\frac{V_i(t)}{R_1} = -C_2\frac{dV_o}{dt} \rightarrow \int_{V_o(0)}^{V_o(t)} dV_o = -\int_0^t \frac{V_i(t)}{R_1C_2}dt$$
$$\Rightarrow V_o(t) - V_o(0) = -\frac{1}{R_1C_2}\int_0^t V_i(t)\,dt$$
$$\Rightarrow V_o(t) = V_o(0) - \frac{1}{R_1C_2}\int_0^t V_i(t)\,dt \quad (3)$$

The above statement concludes that the output voltage at any given time t is proportional to the integration of that voltage upto that time t. Beginning from the equivalent switched capacitor circuit and in terms of charge transferred from input to output, we can say that each clock cycle runs like, C_1 is absorbing a charge $Q=C_1V_i$ when ϕ_1 is active and this charge from C1 is transferred to C2 when ϕ_2 is active [6]-[11]. At ϕ_2 active we can write that the output changes at each cycle of clock is given by equation (4),

$$V_o = -\frac{Q}{C_2} = -\frac{C_1}{C_2}V_i \quad (4)$$

A staircase waveform when approximated by a ramp signal is observed to be functioning as an integrator. This can be clearly observed from the fig. 3 and fig. 6,

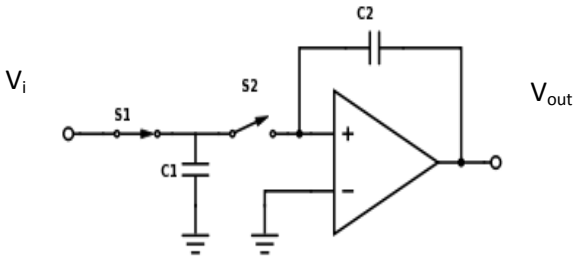

Fig. 3 Fundamental Switched-Capacitor Integrator

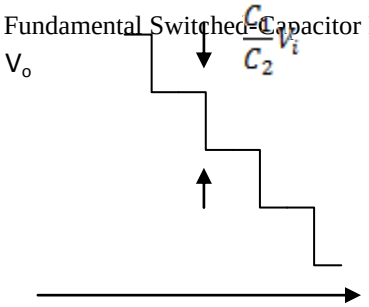

Fig. 4 Staircase resultant of Switched-Capacitor Integrator

V_o being the final value after k clock cycles T_{ck} can be written as in equation (7),

$$V_o(kT_{ck}) = V_o[(k-1)T_{ck}] - V_i[(k-1)T_{ck}].\frac{C_1}{C_2} \quad (5)$$

And as said in the beginning, here it can be justified as a **sampled system**. Based on the output sampling phase, a Switched-Capacitor Integrator can be full delay or Half delay Switched-Capacitor Integrator. The operational amplifier is (4) operational during full delay phase and partially operational during half delay phase. In partially operational switched-capacitor opamps, power reduction reaches about 50%. In current mirror opamps the transconductance can be switched off during sampling phase, in both half-delay or full-delay switched capacitor integrator. In todays technical era Switched-Capacitor Integrator circuits are finding a wide use in applications of analog digital Integrated circuits, which are formed by using components such as OTAs and OPs. In signal processing circuits majorly known as filters and modulators, and also in mixed signal circuits, switched-capacitor Integrator find a wide variety of usage [12]-18]. This can be said easily by the fact that all the implementations of these combinational circuits, such as filters, are made by the mixture of negative and positive switched-capacitor integrator.

II. SC PI INTEGRATOR DESIGN

On considering a parasitic switched capacitor integrator, we can see that the capacitor C2 having parasitic capacitance from every capacitor plate to ground terminal. Parasitic capacitor Cp1 in the left plate is charged to the input voltage in the sampling mode and is discharged by S4 to ground in the integration mode. When we talk about parasitic capasitor Cp2 in the right plate then comes the role of amplifier gain that we obtained in our previous paper. Due to amplifier gain which is finite, the capacitor Cp2 is only charged slightly in the integration mode.

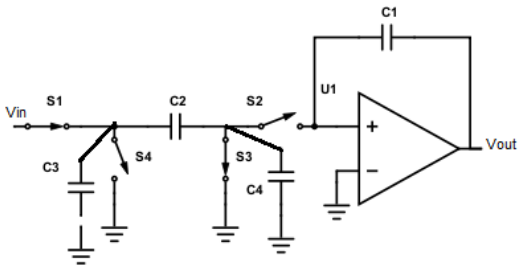

Fig.5 SC parasitic insensitive or classical integrator

Thus capacitor Cp1 deliver no charge to C1 and capacitor Cp2 deliver a very little charge to C1. Also exists a few non linearities aroused from these parasitics.

III. SIMULATION RESULTS

The above discussed SC integrator is simulated with the help of Differential folded cascode amplifier with improved gain. The results and waveforms are shown in the following figures below.

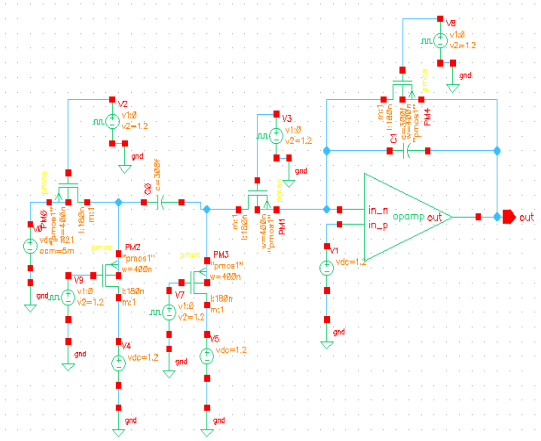

Fig.6 Schematic diagram of SC integrator

Figure 6 shows the schematic diagram of parasitic insensitive SC integrator. In this figure we can clearly see that how the switching has been done. More over the value of capacitor has been kept as low as possible. This is done to reduce the size of the circuit. By doing this the SC integrator is operated at an optimum voltage though there is a trade off between few values. Also the slew rate is found to be low in the differential folded cascode amplifier which leads to the low noise performance of the circuit implemented. As discussed previously, high amplifier gain and optimum slew rate and phase margin is necessary feature for the designing of an optimum SC integrator.

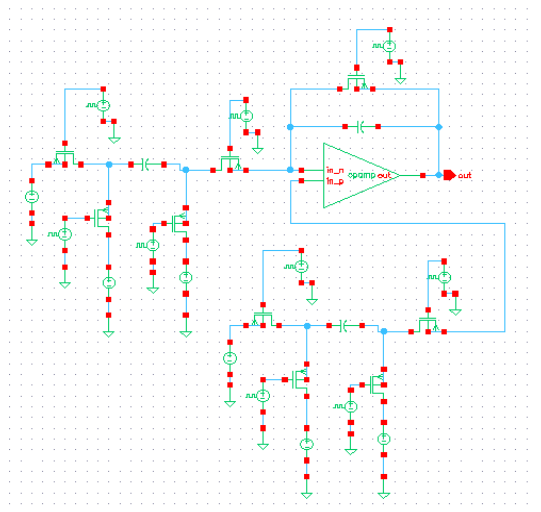

Fig.7 Schematic diagram of Modified SC integrator

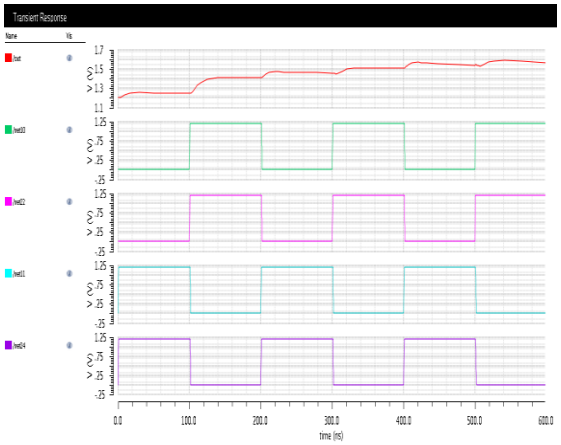

Fig.8 Transient response of SC integrator

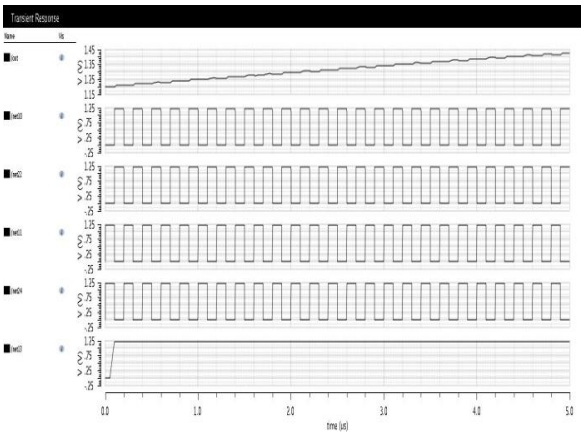

Fig.9 Voltage analysis of SC Integrator

Figure 7 shows the modified diagram of switched capacitor integrator. In this case switching technique is applied to both the terminals. Figure 8 and 9 shows the transient response of the SC integrator and Figure 10 shows the noise response of SC integrator. In this we can see that the noise is reduced and a low noise integrator has been implemented using the used design parameters.

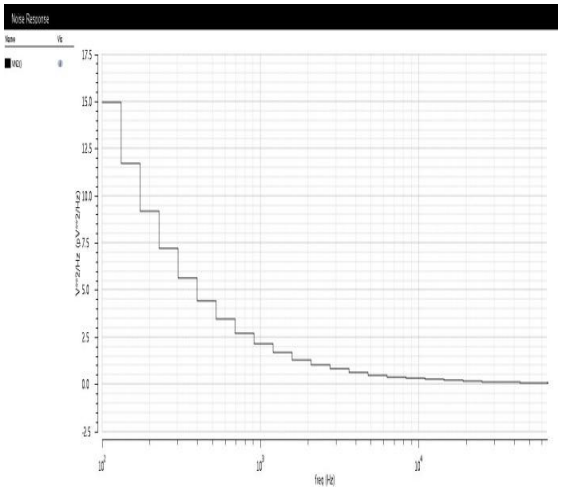

Fig.10 Noise response of SC integrator

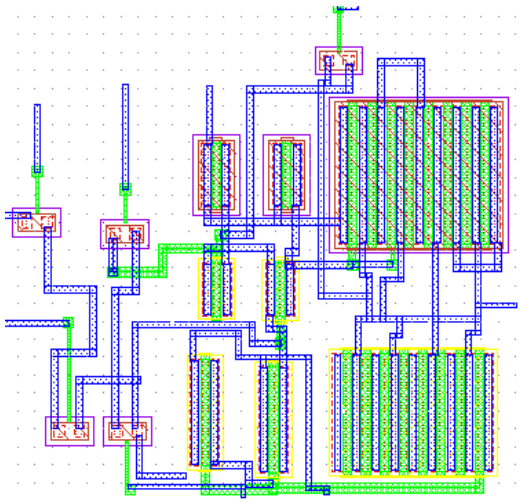

Fig.11 Zoomed layout view of SC integrator design

Figure 11 shows the layout of the Switched capacitor Integrator design. The area has been calculated and it is found that the implemented switched capacitor integrator has an area of 0.16mm2 and the minimum operating voltage is found to be 0.8V. Though there are trade offs in every design and so are present in this.

IV. CONCLUSION

A switched capacitor Integrator having parasitic capacitances have been implemented using a two stage operational amplifier and a differential folded cascode amplifier. Form the analysis this can be obtained that design implemented using amplifier provided few improvements in the Switched Capacitor design model. Also having trade offs, the design has its optimized usage. Besides having trade offs the design can be a good source for low power applications.

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