RESEARCH ARTICLE OPEN ACCESS

An Efficient ASIC Design of RRC FIR Interpolation Filter for wireless Communication Applications

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ABSTRACT:
The main objective of pulse shaping filter is to minimize intersymbol interference and shape the signal, In this paper an Application Specific Integrated Circuit (ASIC) is designed using Root Raised Cosine Interpolator Filter by employing multiplier less technique. The transposed direct form II structure of the filter is applied on the cadence platform which ultimately provides the reduced area and high speed. The HDL language is utilized for coding the provided filter specifications, thus the hardware complexity is reduced. The designed filter reduces the area by 40% which improves the hardware architecture. The maximum operating frequency is improved by 18% in comparison to previous work.
Keywords: ASIC, RRC filter, area, Maximum frequency.

Date Of Submission: 10-01-2018 Date Of Acceptance: 27-01-2018

I. INTRODUCTION

The inspiration behind developing a single terminal device is software defined radio which has the capability of providing support to the multiple wireless communication standards like UMTS , WCDMA etc. As we know that different communication standards need different carrier to noise ratio, channel bandwidth, blocking and interference profile, and sampling rates to fulfill all these requirements one reconfigurable sample rate converter is required which can easily fulfill all specifications. Up sampler is widely used by interpolators while down sampler is used by decimator. These are used by the digital baseband signal in increasing or decreasing the sampling rate. Hence, the overlapping and interference effect is seen with the use of sample rate converter in the baseband signal. Therefore, to avoid this interference and overlapping effect any pulse shaping filter is used in shaping the signal. Due to high processing speed the interpolator utilise multirate filters applying less filter taps in parallel [1]-[5]. The transmitting or receiving of signals within a provided or particular channel bandwidth, increasing data transfer rate and to decrease BER is achieved by pulse shaping filters. The most suitable pulse shaping filter is root raised cosine filter (RRC) for the modern wireless communication systems like SDR, cell phones and set top box. RRC filter has high bandwidth limitation and inter symbol interference (ISI) rejection ratio criteria, which is why it is mostly used by multiple wireless standards like UMTS, WCDMA and IS-95. The ability of reducing the BER by rejecting timing jitter makes root raised cosine filter the best option to implement on ASIC platform [6]-[12].

As stated above **Raised Cosine Filter** is used to avoid interference, rectangular pulse infinite bandwidth is not considered in such cases. Rectangular pulse is passed through a low pass filter and we can observe the shape change from rectangular pulse to a pulse with no sharp edges and smoothly outlined. Therefore it is also known as pulse shaping process. The rectangular pulse exhibits non zero amplitude and smooth pulse exhibits few ripples prior and post pulse interval. The ripples can cause decoding of data in an incorrect manner at the receiver end as this ripple interferes with the pulses. The interference can be made minimum by maintaining a time domain shape and such a filter selection that provides the desired reduction in bandwidth. It finds its application in wireless devices and cellular phones for increasing speed, reducing power consumption and area [13]-[17].

$$F(w) = \tau \qquad 0 \le w \le c \quad (6)$$
$$= \tau \{\cos^2[\tau(w-c)/4\alpha]\} \qquad c \le w \le r$$
$$= 0 \qquad w > r$$

Where
τ is the pulse period
α is roll off factor
c is equal to $\pi(1-\alpha)/\tau$
r is equal to $\pi(1+\alpha)/\tau$

The availability of logic synthesis tools came in late 1990s. With help of these tools HDL descriptions

could be compiled into gate level netlists. Below are the steps for designing, these steps sometimes overlap in practical implementation:

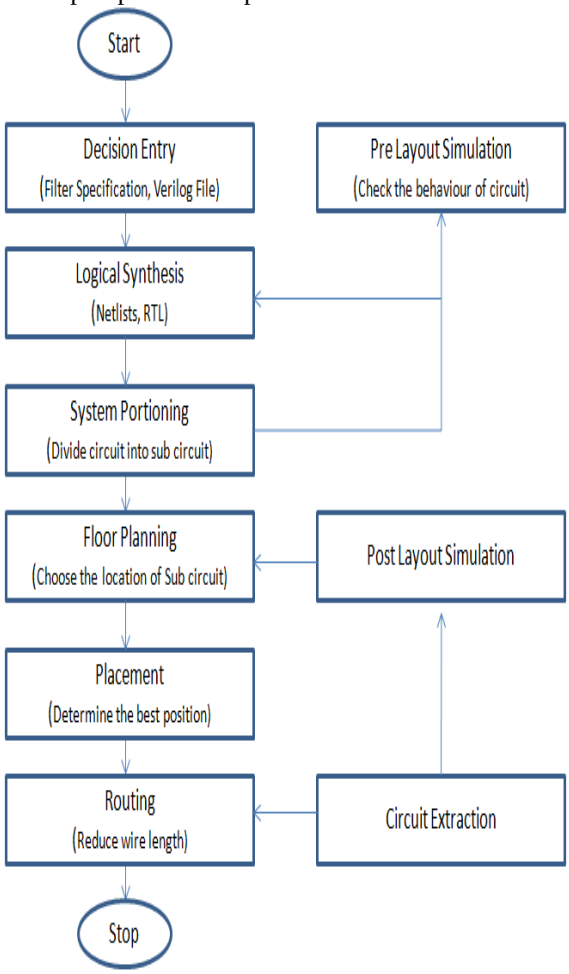

Fig. 1 Flow chart of ASIC design

Requirement analysis is done to understand the required functions of the new ASIC. Using a HDL the goals are achieved and it starts with constructing the description of ASIC. Analogous process is utilized for writing the program using high level language. This method of designing is known as Register Transfer Level (RTL)

Functional verification is conducted to understand the suitability for purpose. Many techniques are included during the process, such as – emulation, formal verification, logic simulation, or creating software model equivalent, etc. Many methods are used and each technique has its own advantages and disadvantages RTL design is transformed into large collection of lesser level constructs which are called as standard cells using the logic synthesis process. Standard cell library which contains pre characterized collection of gates provides the constructs. Typically what happens is that standard cells are specific to the ASIC for the manufacturer. The result is called gate level netlist which is nothing but collection of standard cells with required electrical connections. Now a placement tool is used process the gate level netlist, which places standard cells into final ASIC. Standard cells placement is attempted, however it is subjected to various constraints Physical placement of standard cell is taken by routing tool and is utilised to develop the electrical connection by using the netlist. This will help in developing a optimal solution. Physical Integrated Circuits can be produced by using the file output which is fed for creating a set of photo masks which enables the fabrication facility of semiconductor The final layout is used to calculate the capacitance and parasitic resistance. When there is a digital circuit further mapping is done into delay information, which in turn is used to identify the circuit performance, normally by static timing analysis. Further tests are done to ensure device works fine in case of extreme temperature, voltage, etc. For chip fabrication photomask information is provided to compete the process.

II. INTERPOLATOR

Upsampling or interpolation adds zero in between the samples of original signal to increase the sampling rate, Now this signal with high sampling rate is provided as an input to the other system where this type of signal is needed. In a way upsampling provides distorted spectral images which is further removed by filtering. This motivated us to propose an interpolation factor of 8 for a 49 tap filter design.

III. MATLAB BASED INTERPOLATOR

The impulse response of RRC filter decays in between 10 to 15 and 32 to 35 samples but after 35 samples it becomes stable the maximum variations is from 16 to 30 samples while the magnitude response decays and becomes stable at the end.

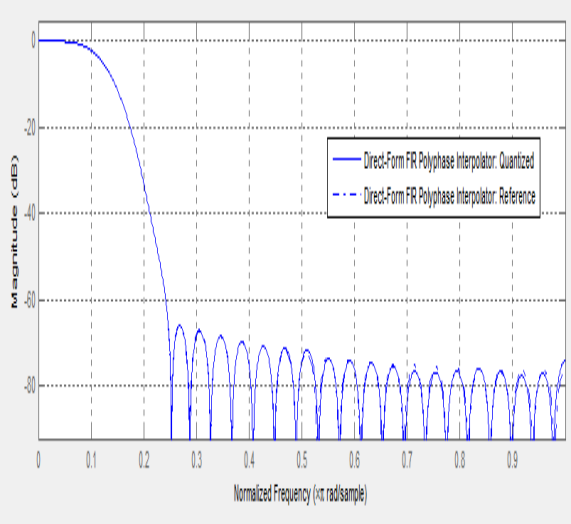

Fig 2 Magnitude response of RRC filter

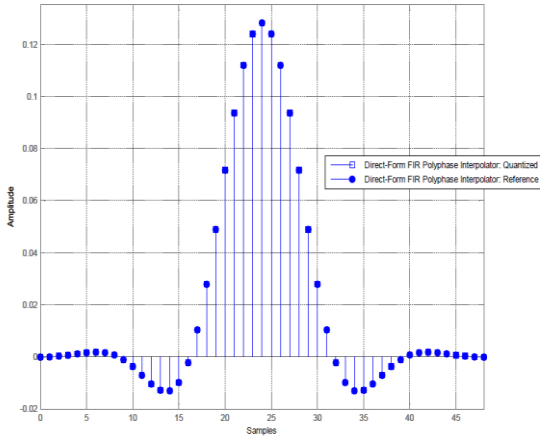

Fig. 3 Impulse response of RRC filter

The unit circle is used to represent the pole zero plot, if all the poles lie inside the circle it represents the stable response, but if poles lie on the circumference of the circle then response is marginally stable and lastly if all the poles lie outside the circle then the response is unstable. As it can be clearly depicted from the fig 4. that the response is stable as all poles lie inside the circle.

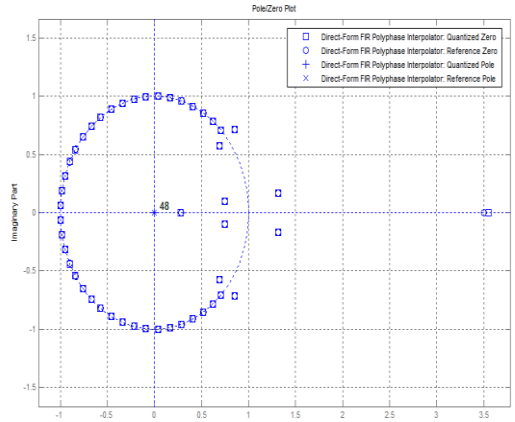

Fig. 4 Pole Zero plot of RRC filter;

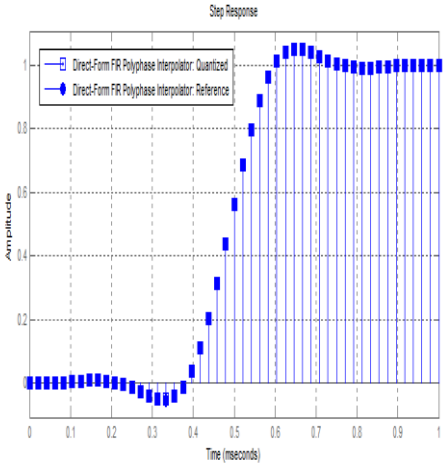

Fig. 5 Unit step response of RRC filter

As it can be seen clearly that the unit step response shows variations or transient response till 0.7ms but after the 0.7ms the unit step response provides output as unity and thus the response becomes stable.

IV. ASIC SIMULATIONS

Fig 6. depicts the waveform produced before layout . Fig 7. depicts the laypout of the designed filter. Fig. 8 is achieved after floorplanning and routing.

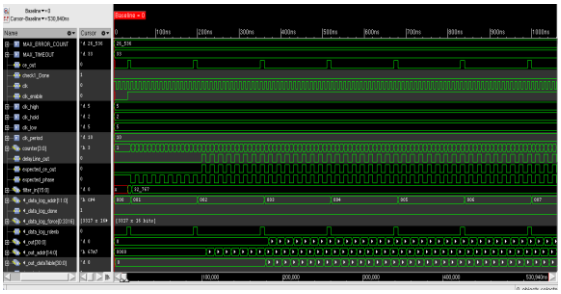

Fig.6 Filter waveform before layout

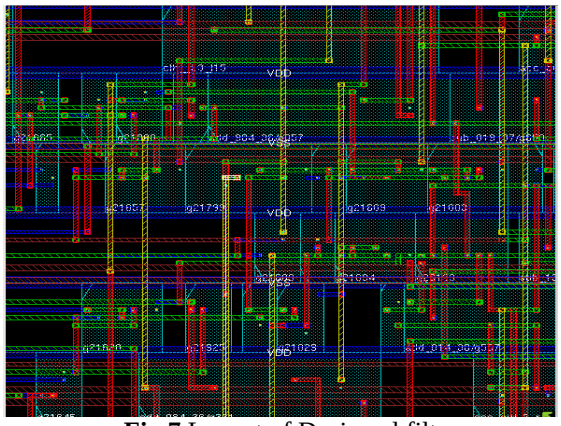

Fig.7 Layout of Designed filter

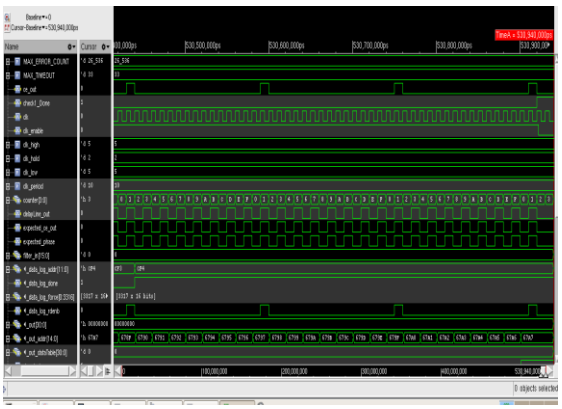

Fig. 8 Filter waveform after layout

V. SYNTHESIS RESULTS

The ASIC design of 49 tap filter is compared with the previous work and the area is

found to be reduced by 40% and the maximum frequency is increased by 18%.

Table I. Comparison results on ASIC

Parameter	Previous work[1]	Proposed work
Area($mm^{2)}$	0.1617	0.0966
Maximum frequency(MHz)	170	200

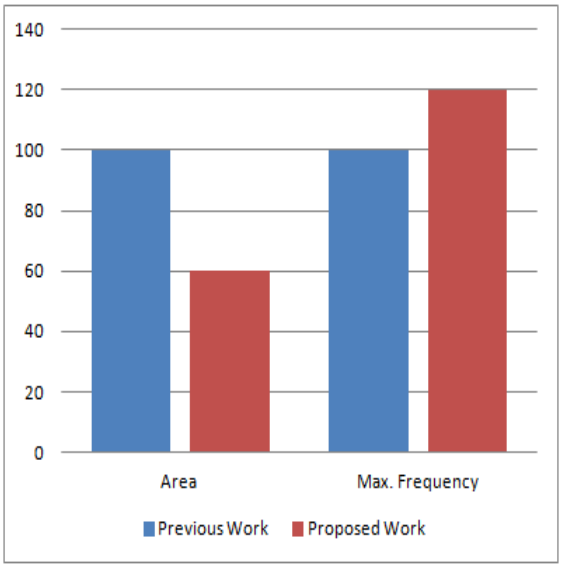

Fig. 9 Comparitive Analysis

VI. CONCLUSION

Thus the multiplier less technique used in implementing the RRC FIR interpolation filter reduces the hardware architecture and delay which is essential in wireless communication applications. The proposed transposed direct form II structure helps in minimizing the total number of nets and the connections between the devices. The architecture proposed in this paper is implemented using 180nm technology on ASIC platform. Therefore the optimization techniques makes operating frequency 18% more efficient and the area is reduced by 40% in comparison to previous work.

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International Journal Of Engineering Research And Applications (IJERA) Is **UGC Approved** Journal With Sl. No. 4525, Journal No. 47088. Indexed In Cross Ref, Index Copernicus (ICV 80.82), NASA, Ads, Researcher Id Thomson Reuters, DOAJ.

Priyanka Agrawal. "An Efficient ASIC Design of RRC FIR Interpolation Filter for wireless Communication Applications." International Journal Of Engineering Research And Applications (IJERA), vol. 08, no. 01, 2018, pp. 81–85.