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Adaptive Hold Aware Clock Gated MAC

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ABSTRACT:
This paper proposed the design of low power Multiply and Accumulate (MAC) Unit utilizing the techniques of Ancient Indian Vedic Mathematics that have been adjusted to enhance performance. The speed of MAC depends incredibly on the multiplier. The work has demonstrated the proficiency of UrdhvaTriyagbhyam–Vedic method for duplication which strikes a distinction in the real procedure of augmentation itself. Low power is the most basic issues in today's ASIC design, as the component size is downsized. Henceforth there is a critical requirement for power improvement. Clock gating is a standout amongst the most exquisite and great techniques for diminishment of dynamic power, significant supporter in all out power utilization of any VLSI circuit. Contrasted with ordinary conventional multiply and accumulate we embraced versatile hold based clock gating for decrease of clock power of gathering of registers utilized of intermitted storage.
Keywords: MAC unit, multiplier algorithm, Vedic multiplier, clock gating, ASIC design, latch base clock gating cell and clock gate enable generator

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I. INTRODUCTION

Accomplishing Low power is a standout amongst the most essential issues in today's ASIC (Application Specific Integrated Circuit) design. As the transistor downsized, power thickness turns out to be high and there is a critical need of lessening in power. The synchronous design style is utilized by a large portion of the designers these days, in such synchronous circuits, the vast majority of the power is expended in the clock arrange [1]. The clock system is in charge of flipping of the flip-flounder (FF) and handling of the combinational rationale. As the combinational rationale does not sway much, the change in FF states influences power utilization. The clock gating is standouts amongst the most key techniques, which decrease clock, arrange power [5]. By addition of clock-gating cells in a design, dynamic power and range involved has been lessened. There are three approaches to make a clock-gating cell, these are (1) Latch based clock gating cell (2) FF based clock gating cell (3) Gate based clock gating cell

1.1) M A C Operation:

The Multiplier-Accumulator (MAC) operation is the fundamental key operation in DSP applications as well as in interactive media data preparing and different applications. As specified above, MAC unit comprise of multiplier, adder and enrol/accumulator [1]. In this, we had used 64-bit Vedic multiplier. The multiply accumulate unit figures the result of two numbers and adds that item to an accumulator. The MAC unit comprises of a multiplier followed by a snake and an accumulator enlist, which stores the outcome [2]. The engineering of the designed MAC unit has appeared in the figure 1. The two information 64 bit operand to the MAC unit are A and B .The gives accumulated yield from MAC unit is Final out.

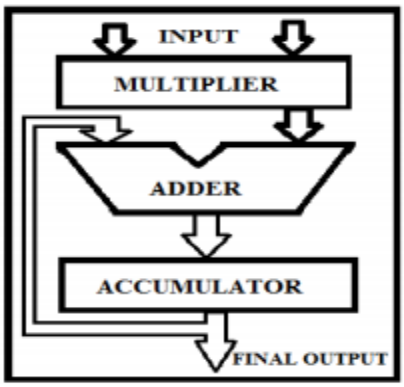


Fig.1. Architecture of MAC unit International

1.2 Latch Based Clock Gating Cell

In latch based clock gating, hook utilized as a control component, it controls the Enable stick. In negative clock cycle, hook is being allowed to mirror the change of Enable pin. In positive clock cycle, output of latch stays settled. The high output of latch allows the clock to achieve consecutive rationale. The period in which, we can detect the change in Enable signal has called as dynamic period, and other period in which we can't detect the change in Enable signal is called rest period. As appeared in Fig. 2, negative half cycle of clock is dynamic period, and positive half cycle is active period. In the event that Enable signal changes amid rest period, the change of the Enable signal can't be caught, this can prompt an off base design. Empower CLK g_clk.

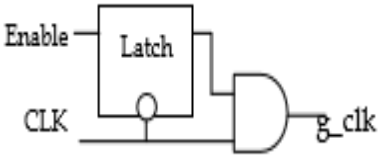


Fig.2. Latch Based Clock Gating Cell

There are two sorts of Latch based clock gating cells. One is without Reset flag, which has appeared in Fig. 2. Second is with A Latch Reset, which has appeared in Fig. 3. Enable Reset g_clk Clock.

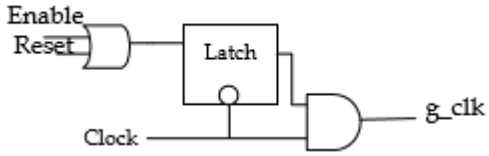


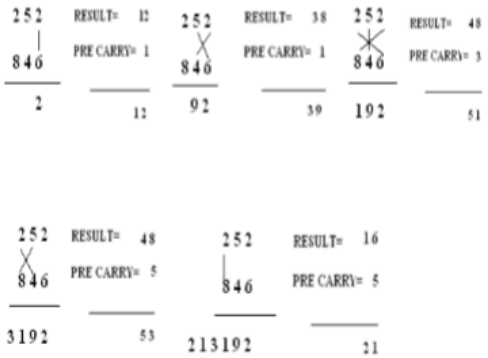
Fig. 3. Latch Based Clock Gating cell with Reset

II. MULTIPLIER DESIGN:

2.1) Vedic Multiplier:

The proposed Vedic multiplier will function based on ―UrdhvaTriyagbhyam sutra (algorithm). These have been customarily used for the duplication of two numbers in the decimal number framework. In this work, we apply similar thoughts to the binary number framework to make the proposed calculation perfect with the advanced equipment. It is a general increase equation relevant to all instances of multiplication. It actually implies ―Vertically and Crosswise‖. It has in light of a novel idea through which the era of every single incomplete item should be possible with the simultaneous expansion of these fractional items [7]. The calculation will sum up for nxn bit number. Since the halfway items and their totals computed in parallel, the multiplier is autonomous of the clock recurrence of the processor. Because of its consistent structure, it can be effortlessly format in microchips and designers can without much of a stretch evade these issues to maintain a strategic distance from calamitous gadget disappointments. [8] The handling power of multiplier can without much of a stretch be expanded by expanding the info and yield information transport widths since it has a significant standard structure. Because of its normal structure, it can be effectively format in a silicon chip. The Multiplier in view of this sutra has the preferred standpoint that as the quantity of bits' builds, gate delay and region increments slowly when contrasted with other ordinary multipliers.

2.2) Multiplication of Two Decimal Numbers 252 x 846



To show the effectiveness of our design, let us consider the multiplication of two decimal numbers 252 x 846 by Urdhva-Tiryagbhyam method. The digits on the both sides of the line are multiplied and included with the carry from the past stride. This produces one of the bits of the outcome and a carry. This carry is included the following stage and subsequently the procedure goes on. On the off chance that more than one line is there in one stage, every one of the outcomes is added to the past carry. In each progression, least significant bit goes about as the outcome bit and every single other bit go about as carry for the following stage. At first the carry is taken to be zero.

III. PROPOSED FRAMEWORK:

In proposed method, we have executed another procedure to lessen the dynamic power, as we probably am aware 30-40 % of aggregate power devoured by utilizing clocks as it were. With a specific end goal to conquer the undesirable clock exchanging we are utilizing conventional clock gating system. Be that as it may, the issue is to produce the enable for the clock gate, that can be overcome by our proposed clock gate empower/enable generator circuit. Multiplier and adder sets aside limited opportunity to achieve the last esteems mean time by exchanging of the fan-

out rationale causes undesirable power. All these can be overcome by creating the best possible low power methodologies for proposed method design. In our proposed MAC design, for duplication we utilize the quick multiplier like Vedic multiplier. We present the two low power methods to be specific operand disengagement and clock gating. With the clock gating undesirable clock exchanging can be maintained a strategic distance from, operand disconnection can keep away from undesirable exchanging of the adder circuit.

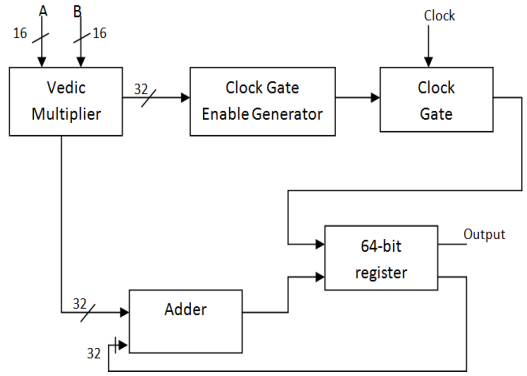


Fig.4. Proposed architecture

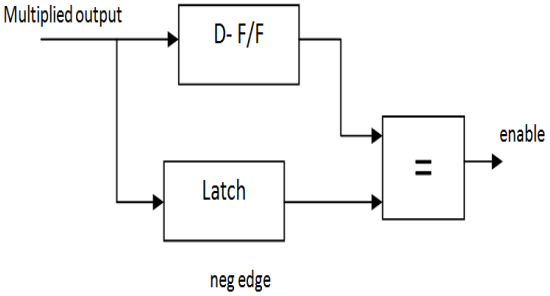


Fig. 5. Clock gate enable generator

The multiplier output has been given to the Clock gate enable generator (CGEG) circuit, CGEG comprise of D-F/F and dynamic low latch. At whatever point output of multiplier changes both F/F and latch catches the information at particular edge and level. F/F and latch outputs has been given to the comparator circuit, if both are equivalent then it creates the enable flag that is given as control and empower of adder and clock gate circuits individually. Furthermore, that can be given as control flag for power off demine likewise if necessary.

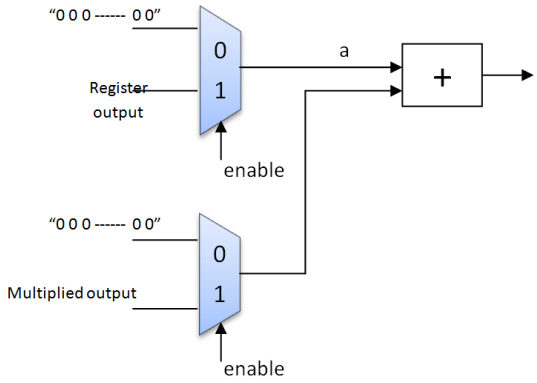


Fig. 6. Operand isolation enable adder

IV. RESULTS AND DISCUSSION:

The MAC unit is designed using digital schematic in Verilog-HDL and synthesized in Cadence 180nm RTL Complier logical synthesis. The proposed MAC unit is implemented using two different coding techniques viz., Wallace tree and Vedic technique for 32-bit multiplier. The simulation results for 32 bit multiply and unit has shown in the figure 7 and 8

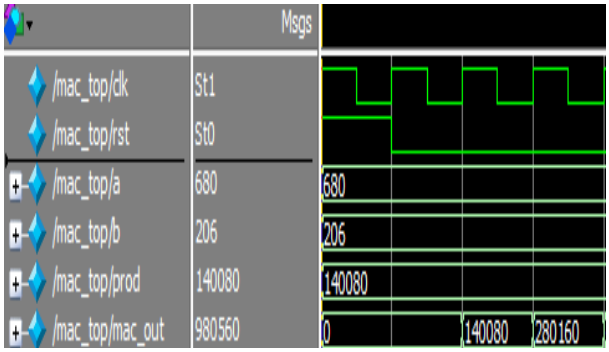


Fig.7. Simulation result of MAC Unit

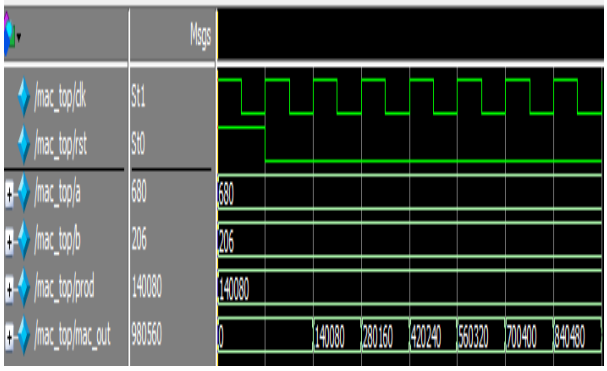


Fig. 8. Simulation result of proposed MAC unit

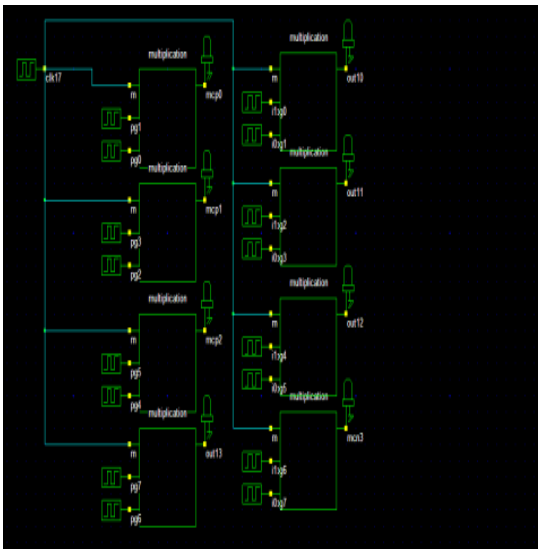


Fig. 9. 8-bit multiplication

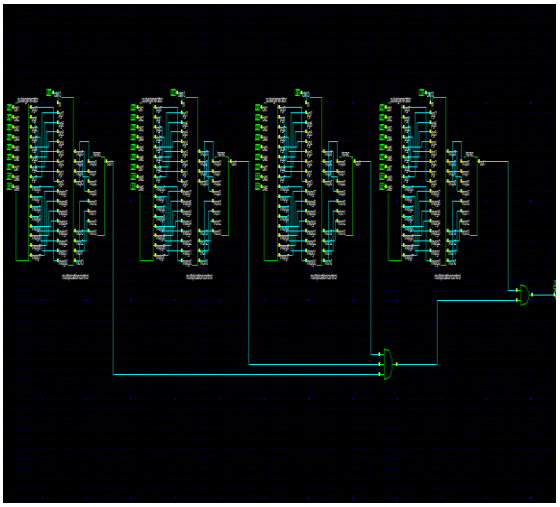


Fig. 10. 32-bit MAC

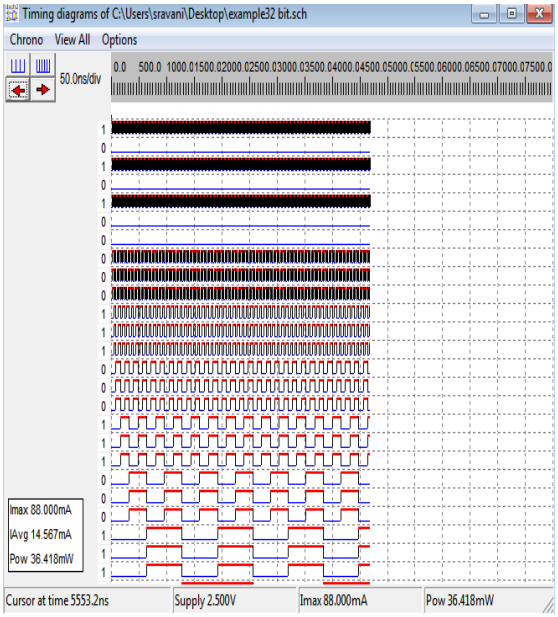


Fig. 11. 32-bit MAC result with timing diagrams

Author in [13], designed a square and multiply and accumulate (MAC) unit by using Vedic multiplication techniques. The total power dissipated by 32 bit MAC unit is 77.7 mW and the area occupied by it is 11 m2. The proposed system output figures has been shown in figure 9, 10 and 11 and we had got the less dynamic power and reduced area when compared with the conventional techniques. Comparison of dynamic power dissipated and the area occupied has given in table 1.

Table 1: Comparison of dynamic power and area values

Method	Dynamic Power (in mW)	Area (in m2)
Ref. [11]	100.88	56.28
Ref. [12]	62.88	66.28
Ref, [13]	77.7	11
Proposed	36.418	9

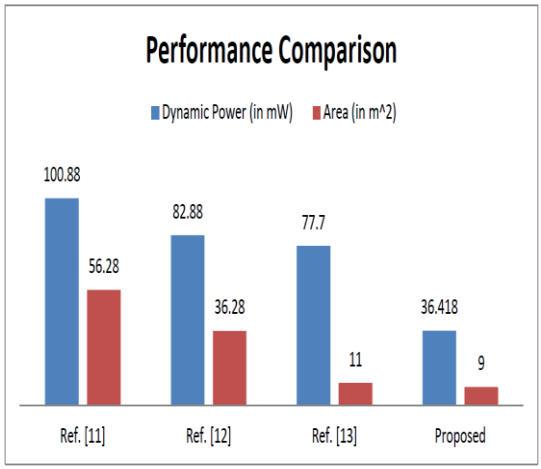


Fig. 12. Performance comparison of Power and area with existing and proposed techniques

V. CONCLUSION

In this, we had implemented Vedic multiplier based low power MAC unit, which gives us hierarchical multiplier design framework. Hence, it has reduced the complexity of the design for the number of bits and enhances the modularity. The designed algorithm with Vedic overlay high speed multiplier based MAC unit shown enhanced productivity as far as speed and area. However, the clock gating is one of low power method henceforth We produced effective control enable for clock gating by utilizing clock gate enable generator to enable the utilization of clock gating to switch off idle sections of the design and mitigated overall dynamic power consumption.

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