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Design and Synthesis of A FPGA Based Controller Dependent Analog Data Acquisition System

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ABSTRACT
This paper presents design and implementation of Analog Data Acquisition System based on Field Programming Gate Array and 12 bit Analog Digital Conversion Chip ADC128S002. Research presents soft core Universal Asynchronous Receiver Transmitter (UART) model and an additional soft core acquisition model to transmit acquired data at high data baud rate. This paper mostly focused on hardware design and system architecture. Acquisition system is developed using Very high speed integrated circuit Hardware Description Language (VHDL). This system is able to provide converted digital data to the external environment through serial data communication at baud rate 115200. In association this design leaves a choice to configure a maximum number of channels at run time through application protocol which will be used by the controller periodically.
Keywords: VHDL; Synthesis; Altera Quartus II; Model Sim; Cyclone IV, UART, SPI

Date of Submission: 03-07-2017 Date of acceptance: 01-08-2017

I. INTRODUCTION

Depends on application purposes, Digital Devices both in industrial and non-industrial sectors require Analog data. Based on the scopes of use these may take an important role. Many Sensors provides information in terms of analog data such as Sound, Gas, Temperature etc., which needs processing as soon as possible to provide a reliable safety or Controller functionalities. In multi Sensor based environment, in order to optimize Controller Processing Cycle considering embedded device platform such as microcontroller based system, this external device architecture is introduced to avoid polling method for multi-channel analog data and System delay required for Analog to Digital Conversion. Moreover, for Controller, a communication protocol has been introduced to set maximum conversion input analog channel.

II. SYSTEM ARCHITECTURE

Proposed system consists of three parts **a.** Data Acquisition Module **b.** Communication Module **c.** Controller Module. System Architecture is based on Field Programming Gate Array (FPGA) written in Very high speed integrated circuit Hardware Description Language (VHDL) and Additional Analog to Digital Converter module ADC128S002. Overall Block diagram of the system is described in Figure. 1.

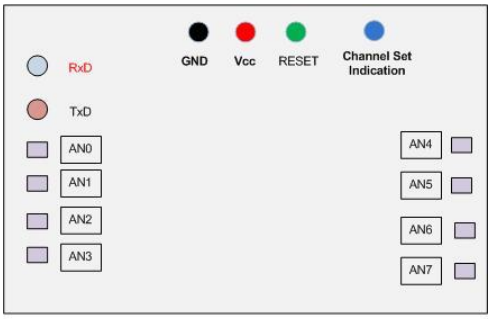

Fig. 1. Device Top View

III. DATA ACQUISITION MODULE

Analog value must be converted to Digital values in order use them in a Digital System. Therefore, Analog to Digital Converter (ADC) is needed. Proposed architecture considers 12 bit ADC128S002 converter which has eight Analog channels and able to communicate to the host device at 0.8 to 3.2 MHz speed [1]. For each channel total 16 clock cycles are needed to obtain 12 bit Data [1]. Inside the FPGA core, Serial Peripheral Interface Protocol (SPI) has been implemented which generates 2 MHz Clock for the ADC converter. Communication between ADC module and host processor based on Serial Peripheral Interface (SPI) Protocol and it is implemented in VHDL. Host processor, this case Cyclone IV FPGA generate a 2 MHz clock for slave device and turn slave chip select pin to low [2][3]. SPI protocol has been implemented can communicate to slave ADC128S002 device, have four functional input output (IO) pin describe in Table 1.

Table 1: SPI IO direction

IO	Directions
Clock	Master Provides Clock to slave.
SS/CSS	Chip Slave Select
MISO	Master In Slave Out
MOSI	Master Out Slave IN

Each 16 clock cycle one analog channel data is obtained by FPGA which will be buffered inside FPGA buffer to transfer it to external device via UART. An internal Finite State Machine (FSM) is designed to capture up to eight analog channels values periodically. However, the maximum number of Analog channels is configurable considering that device may not have eight channels attached in all use cases. Therefore, to optimize Acquisition time in a real environment, FPGA opens an option to select maximum number of channels through its Serial Communication Protocol based on Universal Asynchronous Receiver Transmitter (UART).

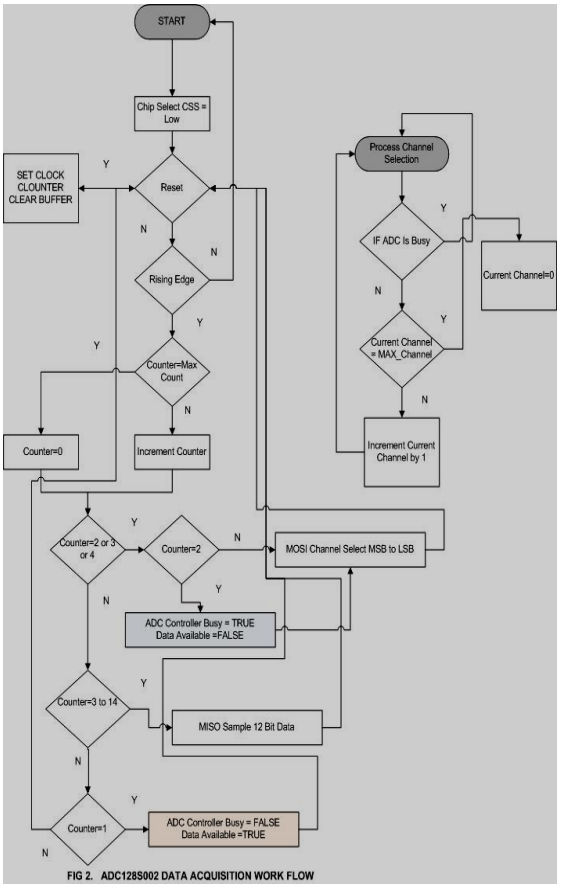

FIG 2. ADC128S002 DATA ACQUISITION WORK FLOW

IV. COMMUNICATION MODULE

Communication between FPGA and external Processor or System can be achieved through Universal Asynchronous Receiver Transmitter (UART) communication protocol. UART protocol supports full duplex communication model, provides reliable data communication mechanism [4] [6] [7]. It supports minimum wiring, indeed Receiving PIN (RxD) and Transmission PIN (TxD). UART model does not provide any clock to the external peripheral therefore; a synchronization mechanism is required for data communication. Proposed device operates at 3.3 volt TTL level logic which is compatible to low power devices. However, communication between this embedded digital device and Personal Computer (PC) can be achieved by using TTL to RS232 converter which has been successfully tested. Serial communication is well defined and operates with the configuration of 11520 baud rate, 8 bit data and No parity. This module can be divided into three parts **a.** Baud Rate Generator **b.** Transmitter Module c. Receiver Module.

A. Baud Rate Generator Module

Baud rate defines the serial data transfer speed or in other words the speed of serial data exchange between two devices. FPGA which is under consideration is equipped with 50MHz clock and Baud rate Generator generates clock to achieve 115200 baud rate and confined with the frequency drift of 10 %. To achieve reliable Communication Generated clock pulse is sixteen time higher then desired baud rate clock [5].

B. Receiver Module

Another finite sate machine (FSM) is designed and implemented to receive data from transmitter module at 115200 baud rate. Once the start condition has been detected successfully which is the Transition of RxD pin from High to Low [4] [6] [7], internal FSM then synchronize its clock, counter and FSM state to Receive Start Condition. During the simulation and real test this module able to receive data at 115200 baud rate. When data has been successfully sampled and module detect Stop condition then after end of the receiving process it generates an Interrupt to notify internal module that new data has been received.

C. Transmitter Module

A finite sate machine (FSM) is designed and implemented to transmit data to external receiver module at 115200 baud rate. Two status input output port has been used in this module, one describes the status of the UART transmitter whether it is busy or not and another one is UART Data Transmit Request. When Transmitter is not in busy state and data transmit request is received, Transmitter module then synchronize its clock, store data into internal buffer to, change its state from Ready to busy and generate Start Condition through TxD pin. During the simulation and real test this module able to send data at 115200 baud rate.

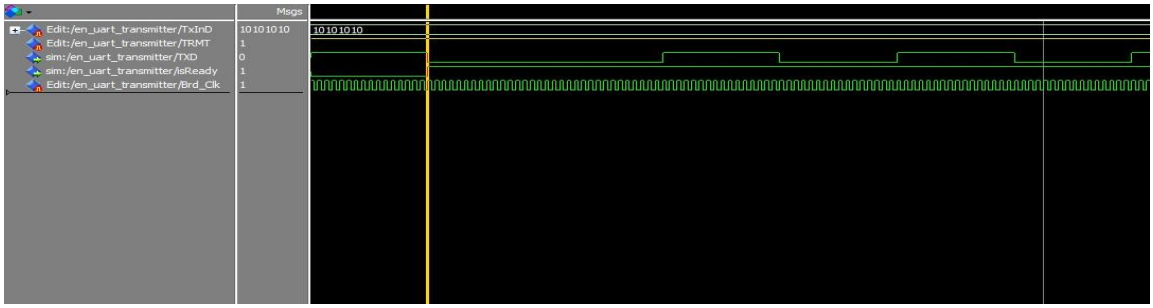

FIG 3. Uart Transmitter with Baud rate 16 times then Desired Baudrate

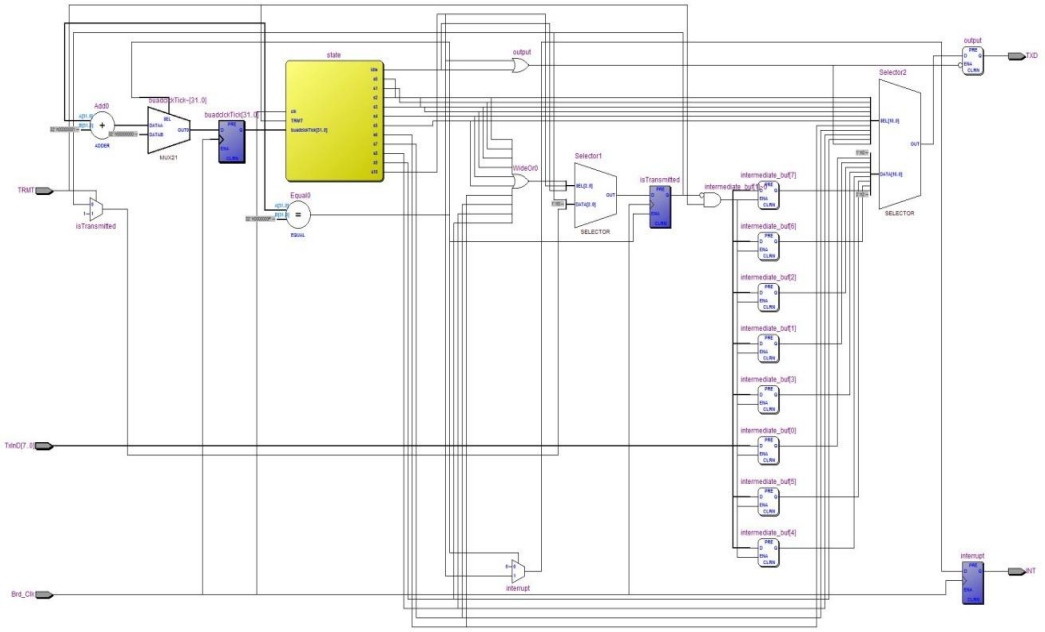

FIG 4. Uart Transmitter RTL Model

V. CONTROL LOGIC MODULE

Control Logic module a soft core finite sate machine consisting finite sate machine circuits. This module designed and implemented to transmit Analog data to external receiver module at 115200 baud rate by using Communication module. Maximum Analog channel number can be configured through serial data communication protocol. When Maximum channel is set, an external output pin goes high for indication purposes. Serial Data Protocol is defined by three bytes of ASCII Data. Where First byte indicates Start of data packet, second byte indicates data which contain value from 0 to 7, eventually analog maximum channel number starting from 0 and last byte indicates End of the Data packet.

TABLE 2: Data packet

Start Packet	Data	END Packet
0x0A	0 to 7	0x0D

When maximum channel has been set, internal FSM then initialized itself to minimum number of channel which is 0 and start sampling analog data from channel 0 to maximum number of channel. Each time the analog data received it stores analog value to its internal buffer and another Finite State Machine periodically sends analog data to external peripheral via UART module.

VI. CONCLUSION

The proposed system shows high speed data acquisition system from analog world to digital world at low power. Each analog channels data are updated at 2 MHz clock. Considering Eight Channels and Sixteen Clock Cycles per Channels, update time for any channel is 8*16/2MHz or 64 micro seconds. More generally it can be expressed as,
(Num_Ananlog_Channel*16)/ 2 MHz.

Considering Host embedded system, when the analog data is updated corresponding to previous values host system can obtain each channel data through two UART interrupt because of 12 bit ADC

data length. Therefore, it saves embedded processor clock cycles by avoiding continuous and periodically ADC data acquisition and value comparison can be benefited by adopting Interrupt driven approach. Moreover, Considering Single Processor Computing system, Processor can execute others task while proposed Hardware does ADC data acquisition. Proposed architecture therefore can take an important part considering time constrains system.

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About Author

Shahnewaz Ali earned his MSc. in Computer Engineering from Politecnico Di Milano, Italy [QS RANKINGS 2015 Top 50 Universities] and BSc. in Computer Engineering from American International University – Bangladesh. Currently he is working in Home Automation sector as an Embedded System Engineer having both hardware and software development responsibilities. He is passionate about problem formulation and solution space exploration, therefore system analysis. He prefers to identify system problems as whole, evaluate possible solutions refers to current Technology and Methods. His research and work interest mainly focused on Intelligent Electronics and Computing System thus it covers various fields such as Hardware - Software Design Methodology based on FPGA –a Hybrid System, Embedded Electronic Circuits and System, System Automation and Control, Digital Signal Processing on SoC, Microprocessor and Microcontroller System Design, Biomedical Instruments and Devices.

International Journal of Engineering Research and Applications (IJERA) is **UGC approved** Journal with Sl. No. 4525, Journal no. 47088. Indexed in Cross Ref, Index Copernicus (ICV 80.82), NASA, Ads, Researcher Id Thomson Reuters, DOAJ.

Shahnewaz Ali . "Design and Synthesis of A FPGA Based Controller Dependent Analog Data Acquisition System ." International Journal of Engineering Research and Applications (IJERA) 7.8 (2017): 06-09.