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Implementation of Low Power 8T SRAM Cell with Dynamic Feedback Control using AVLG Technique

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ABSTRACT
An 8T-SRAM cell using Adoptive Voltage Level Ground (AVLG) technique with better performance, low power consumption and less leakage power has been implemented. The proposed 8T improves the circuit performance at ultra-low power supplies. It attains less power consumption than single ended 8T SRAM cell. By using AVLG technique the circuit consumes less power, even though the no.of transistors and the area are high
Keywords: 8T SRAM, AVLG technique, Leakage Power, Pull-down Network.

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I. INTRODUCTION

In VLSI world the memory and memory cells are the main constraints, while designing any device. The memory is used to store the data and these are available as per our applications. The standard operation in sub threshold region is quite difficult in SRAM's. However it is difficult to operate 6T SRAM in sub threshold region due to leakage power is high[2]. The remaining designs like 5T SRAM and Read Decoupled 8T SRAM are consumes high power and the leakage is also high. To solve this problem the single ended 8T SRAM Cell was implemented with high data stability and achieves to operate in sub threshold region and to operate at low power supplies. The leakage power calculations, SNM calculations using butterfly curves and the comparison of 6T and 8T at 300mv have been observed [5-7]. But at the power consumption factor, it consumes little more amount of power. To overcome the high power consumption the AVLG technique is used for the 8T SRAM Cell. The circuit simulations are done in CMOS 45nm Technology.

II. SINGLE ENDED 8T SRAM CELL

A single ended 8T SRAM Cell was implemented by using Feedback Cutting Scheme. The feedback Cutting scheme is used to maintain the cell stable at all operating conditions. The SE-DFC 8T SRAM has 6 input lines called WWL, WBL, RWL, RBL, FCS1, and FCS2. By using these 6 input lines the information has been given to the circuit. To perform the read operation Read bit line (RBL) and Read Word Line (RWL) is used.

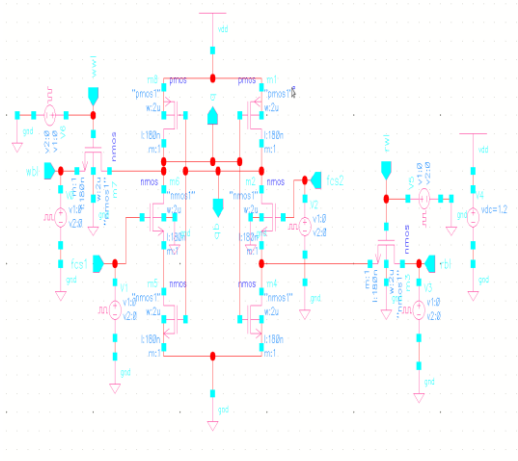

Fig. 1 Single ended 8T SRAM Cell

To perform the write operation Write Bit Line (WBL) and Write Word Line are used. Here, in this circuit there are two selection lines FCS1 and FCS2 are present**.** The 8T SRAM cell was implemented by using 2 pmos transistors and 6 nmos transistors.

Write Operation:

The write operation is performed by the Write Bit Line [1], which was connected at M7 transistor. When the WBL gets activated the write '1' operation will perform. When WBL gets deactivated the write'0' operation will perform. And at the same time the write operation will also controlled by using two cutting scheme selection lines FCS1 and FCS2. When WBL=1, the input signal transferred to the M6, M8 through the M7

transistor even though the signal'1' is transfer to the M6 due to FCS1=0, The M6 gets off and the output stored at Q as 1 due to FCS2=1. And at QB the output will be stored as 0. To perform write '0' operation WBL=0, WWL=1, and FCS1=1, by enabling FCS2 to 0, the data at output side Q will be 0 and at complementary Q (QB) will be 1. The write'0' operation is faster than write'1' operation. The power consumption is also more in write'0' compared with write'1'.

TABLE I Operation Table of Proposed 8T SRAM Cell

	READ	WRITE'1'	WRITE'0'
WWL	0	1	1
RWL	1	0	0
FCS1	0	0	0
FCS2	0	1	1
WBL	1	1	1
RBL	DIS-CHARGE	1	1

Read Operation:

Read operation is performed on the basis of RWL [1], RBL states. When RBL is getting precharged and RWL is getting activated read operation will perform. The outputs Q and QB will be 0and 1. Then at read'1' operation, if FCS1 and FCS2 made high means at the state of'1'. And RWL goes to low (0) then the outputs will be q=1 and q=0 due to positive feedback at respective states.

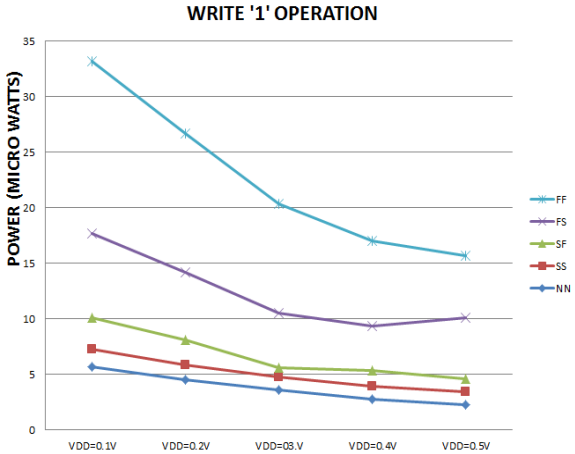

Fig. 2 Write'1'time of 8T SRAM

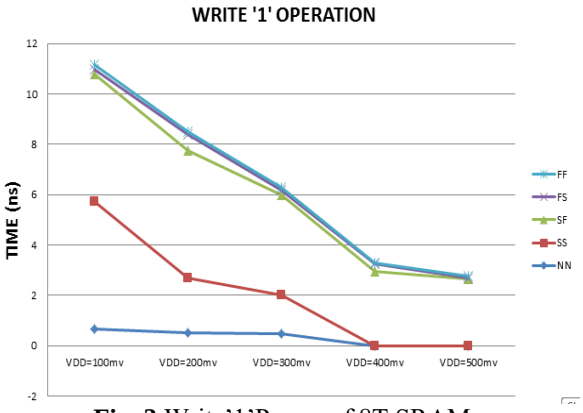

Fig. 3 Write'1'Power of 8T SRAM

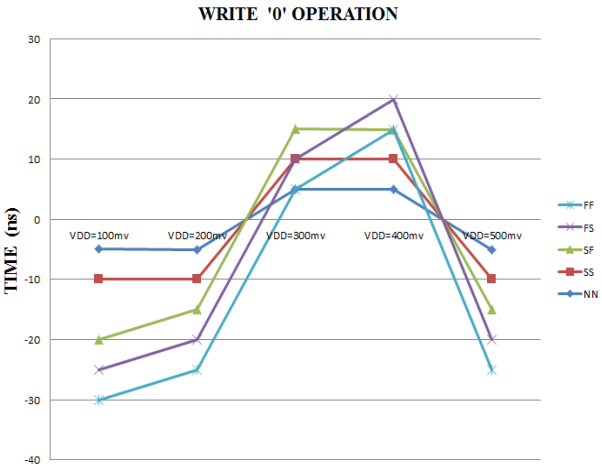

Fig. 4 Write'0'Time of 8T SRAM

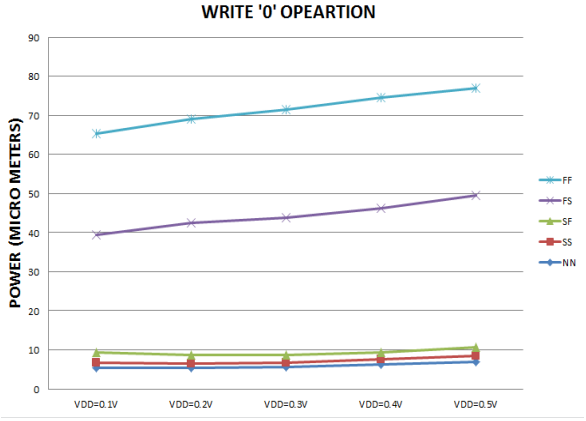

Fig. 5 Write'0'Power of 8T SRAM

III. STATIC NOISE MARGIN

Static Noise Margin is also called as "SNM" [2]. It is mainly calculated in memory cells. It is used to measure the stability of the circuit. The SRAM cell stability will be measured by using static margin calculations. The static Noise Margin will be calculated by using butterfly curves. The largest length of the square fitted in the curves will be the SNM of that particular circuit. The Write Static Noise Margin (WSNM) is calculated at write

operation, the Hold Static Noise Margin (HSNM) will be calculated at hold operation. And Read Static Noise Margin (RSNM) is at read operation.

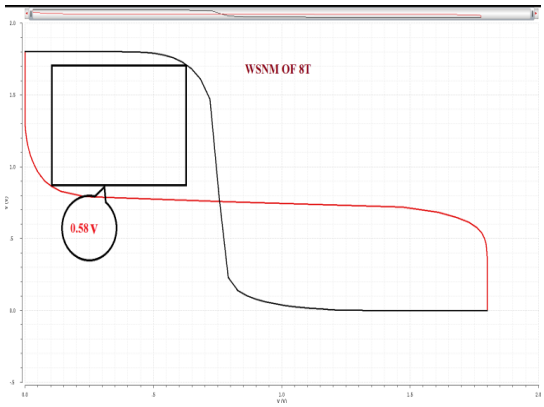

Fig. 6 Butterfly Curve of 8T SRAM

Leakage currents are mainly occurred at sub threshold region. The Leakage current is the amount of current which is dissipated by the circuit at its off state. The leakage current is observed at pmos drain terminal. The leakage current is less in 8T SRAM cell when compared with other cells. Comparison of Leakage Currents [3]-[5] is given below in tabular form.

TABLE II Comparison of Leakage at various SRAM Cells

	I_{leak}(pA) at vdd=0.2 v	I_{leak}(pA) at vdd=0.3 v	I_{leak}(pA) at vdd=0.4 v	I_{leak}(pA) at vdd=0.5 v
8T	1.705	2.102	2.954	2.252
6T	2.593	6.883	29.92	161.3
RD-8T	4.365	5.422	8.065	11.21
5T	2.206	4.001	9.624	30.77

IV. SIMULATION RESULTS&DISCUSSIONS

The 6T SRAM is advanced than 8T SRAM due to decreasing the no.of transistors. Even though it consumes less area than 8T SRAM.

TABLE III Comparison of 6T and 8T at 300mv

Cadence 45nm	Write '1' Power	Write '1' Time	Write '0' Power	Write '0' Time	Read Power	Read Time
8T	3.51	0.48	5.59	4.99	2.3	0.3
6T	17.54	0.3	19.67	3.75	17	0.2

It consumes more power to finish the particular operations. The power consumption is very high in 6T SRAM. To avoid that high power consumption an 8T SRAM cell with feedback cutting scheme was implemented. The comparison of 6T and 8T has been performed at 300mv and the comparison table has given below.

In memory cells power is the main constraint. So, that to overcome the high power consumption, AVLG circuit was connected to 8T SRAM cell circuit. The AVLG circuit was connected in between pull-down network and ground. This consists of 2 pmos and 1 nmos, which are connected in parallel. By adding that circuit we can reduce or decrease the power consumption. It would lift the ground potential of the circuit to reduce the power consumption of the 8T SRAM Cell circuit. Depending upon the input the output also varied and the usage of clock is to prevent any defect in 8T SRAM cell function during power consumption.

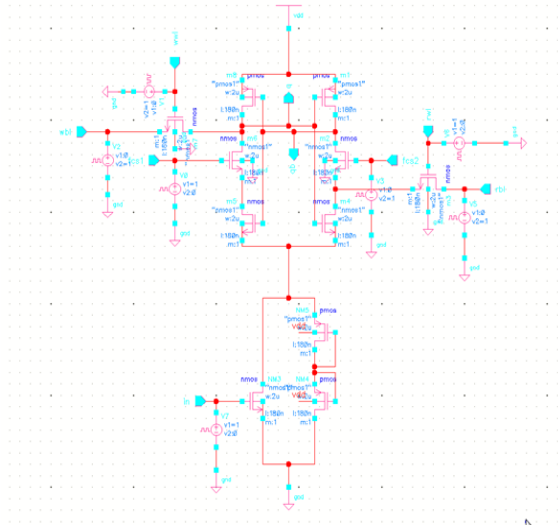

Fig. 7 8T SRAM Cell using AVLG Technique

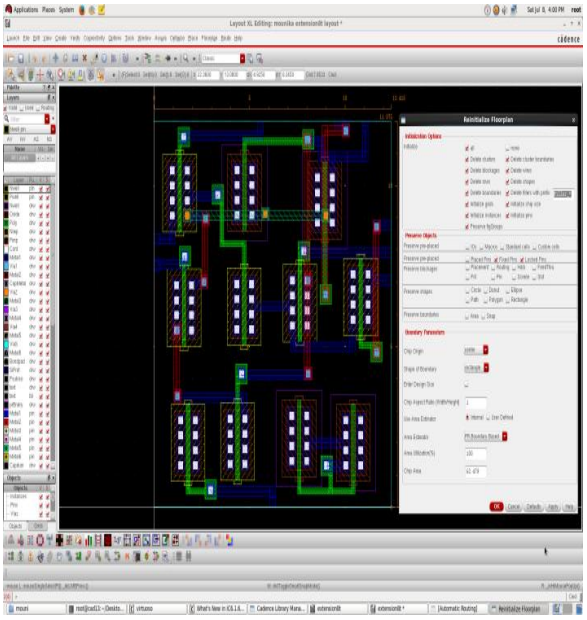

Fig. 9 Layout representation of 8T using AVLG technique

TABLE IV Comparison of Single ended 8T and 8T using AVLG Technique

Cell Type	POWER (nW)	AREA (um^2)
Single Ended 8T SRAM CELL	45.42nW	43.48 um^2
8T SRAM using AVLG	28.23nW	62.47um^2

By observing this we can say that, by using AVLG technique, we can decrease the power consumption. The comparison table was given above.

V. CONCLUSION

The AVLG 8T SRAM Cell has high stability and it consumes less power than feedback cutting 8T SRAM cell. Even though the no.of transistors and area consumption is high. These all observations have been done in CMOS 45 nm technology.

REFERENCES

[1]. C. B. Kushwah, Student Member, IEEE and S.K. Vishwakarma, Member, IEEE. A Single ended with dynamic feedback control 8T Sub threshold SRAM Cell, *IEEE transactions on very large scale integration (VLSI SYSTEMS)*, vol.24, January 2016.

[2]. C. Kushwah and S. K. Vishwakarma, "Ultra-low power sub-threshold SRAM cell design to improve read static noise margin," in *VLSI Design and Test (Lecture Notes in Computer Science)*, vol. 7373.

[3]. B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 680–688, Mar. 2007.

[4]. J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based sub threshold SRAM," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.

[5]. C.-H. Lo and S.-Y. Huang, "P-P-N based 10T SRAM cell for low leakage and resilient sub threshold operation," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 695–704, Mar. 2011.

[6]. V.V.M.Krishna, M. Venkata Subbarao, and V.Venkatarao, "Glitch Reduction in Low Power TG-Multiplier", International Journal of Engineering Research & Technology (IJERT), Issue 6, Volume 2, pp. 2138-2142, June, 2013.

[7]. A.Srinivasarao, M. Venkata Subbarao, "Implementation of 64-Bit Low Power Arithmetic Logic Unit using Multiplexers and Full adders for DSP Applications" International Journal of Research Trends in Engineering and Technology (IJRTET), Volume VI, Issue III, pp. 278-282, Nov, 2015.

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