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A Survey on VLSI Architectures for Wavelets

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ABSTRACT
In this paper we are discussing the various approaches for implementing discrete wavelet transform using VLSI architectures .A comparison is done with the Coherent 9/7 Lifting based 2D-Discrete Wavelet Transform **.** The execution results expose that the suggested architecture is enhanced in area competence, multipliers and adders are also decreased. Therefore by decreasing the hardware exploitation the power consumption also reduced.
Keywords: Discrete wavelet transform, VLSI, word length, Xilinx, FPGA, area, power consumption

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I. INTRODUCTION

The DWT requires lot of mathematical operations to be performed for its implementation .As the number of computations are more, it is required to study the hardware requirements for such complex computations .Basically there are two approaches are there for executing DWT. One is by Convolution method where filter bank structures are used, but such implementations need large number of arithmetic operations to be performed which slows down the speed and increases the hardware required and also the storage space required to accommodate such computations is also large. For lossy and lossless compression correspondingly [3] the (9/7) and (5/3) wavelet filters are placed as the default filters The second method is called as Lifting scheme which reduces the number of computations[4] and avoids the need of multiple additions along with multiplication processes required during any convolution operations . That means the hardware requirement and memory requirement is also decreased with the help of lifting based method for implementing DWT.

II. LITERATURE SURVEY

The coding competence and the quality of image restoration with the DWT are superior than those with the traditional discrete cosine transform. The VLSI architectures to calculate a 1D DWT for real-time multichannel streaming data under stringent area and power constraints are suggested in traditional methods. The executions are based on the lifting scheme for wavelet computation and integer fixed point precision arithmetic, which minimize the computational load and memory obligations. A high-level compilation tool is suggested in a new recent work [5], which produces VLSI architectures at the register transfer level [2].

At different frequencies DWT examines the data with dissimilar time resolutions. The fundamental DWT can be understood by convolution by means of the FIR filter banks to do the transform. The DWT decomposition engages low-pass 'L' as well as high-pass 'H' filtering of an image in both horizontal and vertical directions. The output will be down-sampled to two after each filtering. Additional decomposition is made by employing the above process to the LL sub-band.

An efficient VLSI architecture for lifting-based discrete wavelet transform by Wei Zhang *et al.* [1]. They proposed high-speed and reduced-area 2-D discrete wavelet transform (2-D DWT) architecture. Earlier DWT architectures were frequently based on the modified lifting plan or the flipping structure. At last the number of registers had decreased to 18 without widening the critical path. Besides, the two-input/two-output parallel scanning architecture was implemented in our plan. The suggested architecture only needs three registers among the row and column filters for a 2-D DWT with the size of $N \times N$, as the transposing buffer, and a higher competence had attained.

Chengjun Zhang *et al.* [11] have designed pipeline VLSI architecture for fast computation of the

2-d discrete wavelet transform. For the calculation of the 2-D discrete wavelet transform (DWT), they brought in a scheme for the design of high-speed pipeline VLSI architecture. The intra-stage parallelism was improved by splitting the 2-D filtering operation into four subtasks that can be carried out independently in parallel and reduce the delay of the critical path of bit-wise adder networks for carry out the filtering operation. Suggested scheme, a circuit was proposed, simulated, and executed in FPGA for the 2-D DWT computation. It demonstrated that the presentation in terms of the processing speed of the architecture designed based on the suggested scheme was superior to those of the architectures designed by means of other existing schemes, and it had same or lower hardware utilization.

Efficient multi-input/multi-output VLSI Architecture for two-dimensional lifting-based discrete wavelet transform was implemented by Xin Tian, Lin Wu *et al*. [3] to construct MIMOA. In their effort they construct the MIMOA, which was a high-speed architecture with computing time as low as N^2/M for an N × N image with controlled increase of hardware cost. When multiple row data samples were practiced at the same time high processing speed could be accomplished. And time multiplexing technique was implemented to manage the increase of the hardware cost for the MIMOA. For any lifting-based DWT this architecture was appropriate. A 2D DWT contains horizontal filtering along the rows followed by vertical filtering along the columns. The MIMOA contains M SISO modules, M/2 TITO modules, some multiplexers, and delay registers. Computing time of MIMOA was decreased when compared this architecture with other 2D DWT architecture, and it had least utilization of hardware cost and on-chip memory.

Basanth K. Mohanty *et al.* [11] designed memory efficient modular VLSI architecture for high throughput and low-latency implementation of multilevel lifting 2-d DWT. They improved a modular and pipeline architecture for lifting-based multilevel 2-d DWT, without employing line-buffer and frame buffer. By suitable partitioning and programming of the computation of individual decomposition-levels the general area-delay product was decreased. Cascaded pipeline structure was employed for processing dissimilar levels that could be maximizing the hardware consumption competence. The output latency of this method had $O\left(8R \times 2^{L}\right)$ cycles, which was very little when compared to the latency of the presented methods. It had improved slice-delay-product for higher throughput of implementation as the on-chip memory of this structure continues almost unaffected with input block size. When compared with presented method it had 17% less SDP.

Efficient VLSI architecture for discrete wavelet transform was proposed by Usha Bhanu. N *et.al* [9]. This architecture comprises a transform module, a RAM module and a multiplexer. Polyphase decomposition and coefficient folding method were employed in transform module which was applied for decimation filters of stage 1 and 2 correspondingly. The main benefits of this method was it presented 100% hardware utilization, fast computing time, regular data flow and low difficulty.

Yusong Hu *et al.* [7] developed a memory-efficient scalable architecture for lifting-based discrete wavelet transform. In this technique novel parallel lifting-based 2-d dwt architecture was proposed with high memory competence and short critical path. A new scanning method was applied to achieve memory competence which facilitates tradeoff of external memory bandwidth and on-chip memory. Among the presented one, this architecture was the most memory competent design and in addition it had stable latency. Its hardware resource requirement and computation time are better than other presented method. This architecture used a total of only 3N+24S words of transposition memory, temporal memory, and pipeline registers for an N×N image. It attained better area-delay products by 32.3%, 31.5% and 27.0% when S was 2, 4 and 8 correspondingly.

Basant Kumar Mohanty and Pramod Kumar Meher [10] developed memory-efficient high-speed convolution-based generic structure for multilevel 2-d DWT. This method engaged line-buffers of size 3(K-2) M/4 which was independent of throughput-rate, where K indicates the order of Daubechies/biorthogonal wavelet filter and M is the image height. The structure could be executed for higher throughput because of this. It had usual data flow, small cycle period Tm and 100% hardware utilization competence. In this design Daud-4 filter was employed it requires 152 more multipliers and 114 more adders, however had 82412 less memory words and took 10.5 times less computation time when compared to the presented method. This method accumulated memory higher than the arithmetic components. This architecture engages 2.6 times less ADP and uses 1.48 times less EPI when compared to other presented method.

Performance analysis of modified lifting based DWT architecture and FPGA Implementation for speed and power was designed by C. Chandrasekhar & Dr. S.Narayana Reddy [8]. They proposed hardware efficient, high speed and power efficient DWT architecture based on modified lifting scheme algorithm. The design was modeled by employing HDL and was executed on FPGA. This

design was interfaced with SIPO and PISO to decrease the number of I/O lines on the FPGA. The interfaces necessary for data processing are also proposed and were employed to synchronize the data transfer operation. It was executed on Spartan III device and is compared with lifting scheme logic. For this design 280 MHz frequency was employed and the power consumes would be less than 42 mW. It was appropriate for real time data processing. This plan could be more optimized for video signal processing.

III. SIMULATION AND SYNTHESIS

The figure 3.1 shows the simulation result of, a new lifting-based DWT architecture for 9/7 filter which has lowest temporal memory, achieved with a modified overlapped-scanning method and recalculation of one intermediate DWT coefficient. It requires only 2N temporal memory to process N X N sized image. The architecture has the lowest temporal memory of 2N as compared to other architectures.

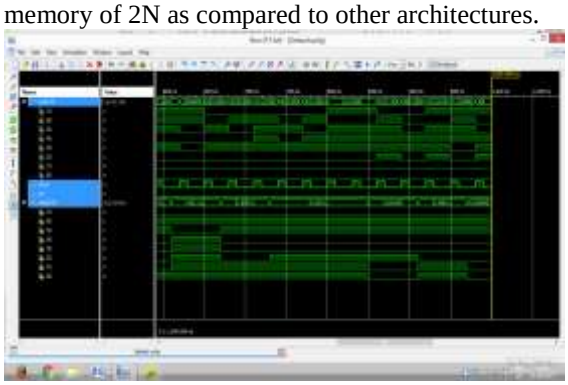

Fig 3.1 Simulation of lowest temporal buffer DWT

The synthesis of the above architecture is shown in Fig 3.2

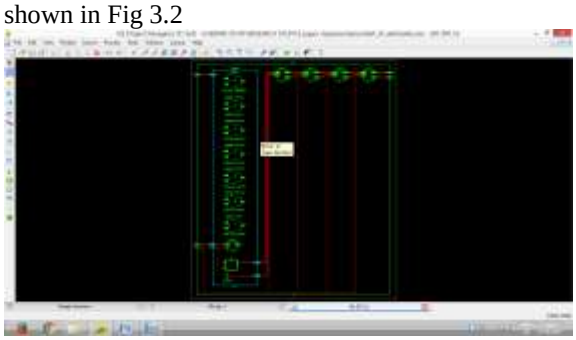

Fig 3.2 Synthesis of lowest temporal buffer DWT

Figure 3.3 shows a simulation of parallel lifting-based 2-D DWT architecture with high memory efficiency and short critical path. The memory efficiency is achieved with a novel scanning method that enables enhancement of external memory bandwidth and on-chip memory. Figure 3.4 show the synthesis of above architecture.

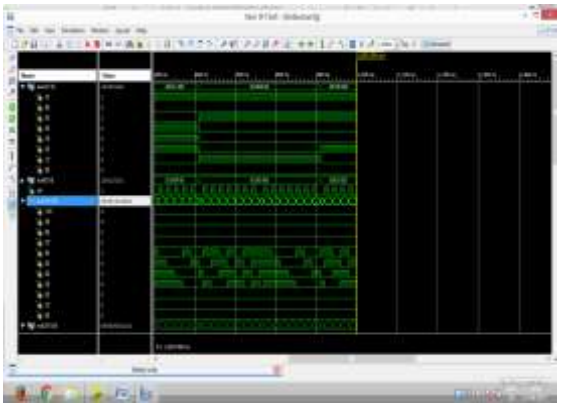

Fig 3.3 Simulation for parallel lifting-based 2-D DWT architecture

Fig 3.4 Synthesis for parallel lifting-based 2-D DWT architecture

Figure 3.5 shows the simulation results for good performance and memory-efficient pipeline architecture which performs the one-level two-dimensional (2-D) discrete wavelet transform (DWT) in the 5/3 and 9/7 filters.

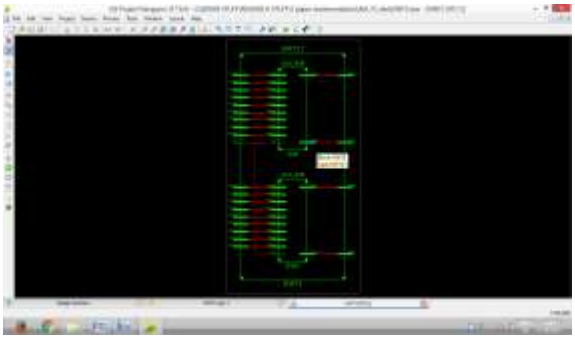

Fig 3.5 Synthesis for Memory efficient lifting-based 2-D DWT architecture

In general, the internal memory size of 2-D architecture highly depends on the pipeline registers of one-dimensional (1-D) DWT. Based on the lifting-based DWT algorithm, the primitive data

path is modified and efficient pipeline architecture is derived to shorten the data path. The other pipelined architectures with direct implementation operate at less speed when compared with 1-D DWT pipeline architecture.

Fig 3.6 Synthesis for Memory efficient lifting-based 2-D DWT architecture

The following table shows the comparision of other architectures with coherent 9/7 lifting based DWT

Architecture	Multiplire	Adder	Registers	Buffer
Darji, A. D, and Ankur Limaye	8	24	75	12
B. Wu and C. Lin,	7	5	22	0
C. Xiong, J. Tian, and J. Liu,	10	20	48	4
Coherent 9/7 filter	10	3	20	4

IV. CONCLUSION

The coherent 2D-DWT lifting based 9/7 wavelet is superior in area and power while compared with traditional methods. Various implementations are simulated and synthesized and it is observed that the number of adders and multipliers are varied and the hardware utilization can be improved and power consumption is decreased in order to improve the performance of the discrete wavelet transform.

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