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Optimization of Temperature Coefficient and Noise Analysis of MOSFET- Only Voltage Reference Circuit

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ABSTRACT
The optimization of temperature coefficient and comparison of output noise of two MOSFET only voltage references are introduced. The circuit behavior is analytically described and the performance of the proposed circuits are confirmed through 180nm CMOS technology in virtuoso and the simulation results are presented. Both the circuits can be operated with supply voltage varies from 0.5-1.2V.The output voltage references varied over a temperature range of -25℃ to 50℃.

I. INTRODUCTION

The widespread use of battery-operated systems, the relatively slow progress of battery performance/cost ratio and the need to minimize simple maintenance procedures, such as battery replacement, are pushing the design of very low voltage and low power systems, both digital and analog. Here we focus on a ubiquitous component of such systems, the voltage reference generator, which in turn has to be "power scaled", in order to be able to operate with a very small fraction of the total power budget.

Voltage references are fundamental circuit blocks ubiquitously used in analog, mixed-signal, RF and digital systems, including memories. Mobile and energy harvesting applications require ultra low power designs, which should be extended to all circuits, including the analog ones. Resistor-less analog blocks have the advantage of implementation in standard digital processes. Basically, voltage references can be divided into three fundamental functions: the generation of two voltages (or currents), one proportional and the other complementary to absolute temperature (PTAT and CTAT, respectively) and biasing.

In this paper we propose two MOSFET only voltage references, optimizing their temperature coefficient and performing the comparison of noise analysis. The voltage reference is analysed over a temperature range of -25℃ to 50℃.

The text is organized as follows: Section 2 presents the proposed system. Different types of noises and noise analysis of voltage reference circuits is proposed in section 3 ,followed by the simulation results of output voltage, noise analysis and layout of one of the proposed voltage reference are discussed in section 4. To conclude, we analysed the performance comparison of both the voltage references.

II. VOLTAGE REFERENCE USING SELF CASCODE PTAT GENERATOR

A voltage reference based on the sum of two almost linear temperature dependent terms is proposed here. A threshold voltage extractor provides the CTAT voltage, and the PTAT voltage is generated by two PMOS unbalanced differential pairs operating in weak inversion. The sum of these two linear terms results in a significant reduction of the thermal coefficient over a wide temperature range.

In ACM model,

The relationship between current and voltage is given by

$$\frac{Vp-Vs(D)}{\emptyset t} = F(i_{f(r)}) = \sqrt{1} + i_{f(r)} - 2 + \ln(\sqrt{1} + i_{f(r)} - 1) \quad (1)$$

Where V_S and V_D are the source and drain voltages (all terminal voltages are referenced to the transistor bulk), and VP is the pinch-off voltage, approximated by

$$V_P \approx \frac{VG - VTO}{n} \quad (2)$$

Where V_{T0} the threshold voltage for zero bulk bias. The first term (the square root one) in the right side of (1) is related to the drift component of the drain current, being predominant under strong inversion. The last term (the logarithmic one) is related to the diffusion component, being predominant under weak inversion operation. In forward saturation $I_F \gg I_R$ and consequently ID $\cong$IF = $SI_{SQ}i_f$.

A. V_{T0} Extractor

The proposed VT0 extractor circuit, shown in Figure 1.From this proposed circuit we are extracting the threshold voltage of transistors M1 and M2. A saturated nMOS-FET with grounded source and operating under a constant inversion level equal to 3 (i_f = 3) will have a gate voltage V_G equal to the threshold voltage V_{T0} from (1) and (2). It happens because under these conditions, the right side of (1) becomes zero. Here M1 is made to operate in the moderate inversion region. M2 is designed with the same geometry of M1, kept saturated too and sharing the same gate voltage, but with a source voltage different from zero. Using (1) and (2) for M2, knowing that V_{G2} = V_{G1} = V_{T0}, leads to (3)

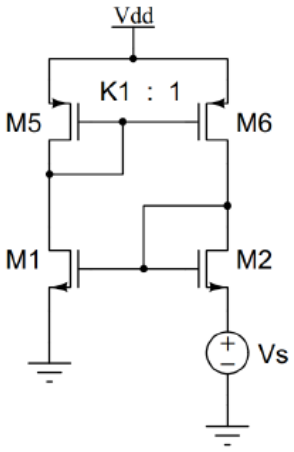

Fig.1. Threshold voltage extractor

$$-V_{s2} = \emptyset_t F(i_{f2}) \qquad (3)$$

So, we can conclude that if the resulting M1 current I_{D1} is also used to control the drain current I_{D2} (through the M5-M6 current mirror), M2 also operates under a constant inversion level, making $F(i_{f2})$ constant. Thus, if a voltage proportional to ∅t is attached to the source terminal of M2, with the right proportionality factor $F(i_{f2})$ adjusted (using the current mirror aspect relation K1), the equality of (3) can be satisfied. A non-zero equilibrium point is then reached in this circuit, that keeps V_{G1} = V_{G2} = V_{T0} for any temperature. Since M2 operates with higher source voltage than M1, its inversion level has to be lower, or F(if2) < 0. So in this circuit M2 operates in the weak inversion region. The temperature dependence of the threshold voltage V_{T0} can be approximated by the linear equation (4).

$$V_{TO}(T) = V_{TO(nom)} + k_T(T - T_{nom}) \qquad (4)$$

Where T is the absolute temperature,V_{T0}(nom) is the threshold voltage at the nominal temperature T_{nom} and K_T is the thermal coefficient of the threshold voltage.

B. Self Cascode Ptat Generator

To generate a PTAT voltage independent of process parameters a self-cascode MOSFET, introduced by Vittoz in 1977 is shown in Fig.2. Transistor M3 has higher drain current thanM4 but smaller aspect ratio which leads to different inversion levels on each transistor. Transistor M4 must be in saturation while M3 can be in saturation or in triode. The difference between their gate-source voltages appear across the drain-source terminals of M3.

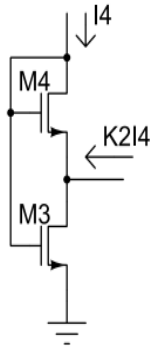

Fig. 2. Self Cascode PTAT Generator

This voltage is proportional to the thermal voltage. It is given by

$$V_{SC} = V_{DS3} = \emptyset_t [F(i_{f3}) - F(i_{if4})] \qquad (5)$$

Usually both transistors operate in weak inversion, but (5) shows that as long as the inversion levels of both transistors are kept constant over temperature, they generate an ideal PTAT voltage under any inversion level. This can be achieved by biasing them with current I_4 = K_3I_{SQ}, where K3 is constant with process and temperature. (5) then becomes

$$V_{SC} = \emptyset_t [F(K_3 \div S_3)(K_2 + 1) - F(K_3 \div S_4)] \qquad (6)$$

PTAT voltage generated by the self-cascode MOSFET depends only on geometrical factors, and not on fabrication process parameters.

C. Unbalanced differential pair ptat generator

From unbalanced differential pair PTAT generator introduced by Tsividis in 1978, that operates in weak inversion, we are generating the PTAT voltage. Here K4 and K5 are the aspect ratio relations of M8-M9 and M11-M10, respectively.

Transistors M8 and M9 share the same source connection, and the PTAT voltage develops across the two gates. By using the ACM model, it is possible to extend the operation of this circuit to all inversion levels, as was done for the self-cascode structure. Assuming that all transistors are in saturation and using (1) and (2), the PTAT

voltage generated by the differential pair V_{DIFF} is given by (7).

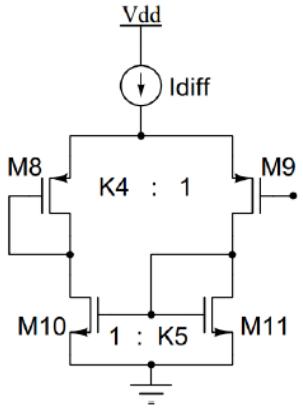

Fig. 3. Differential pair PTAT generator

$$V_{DIFF} = V_{G9} - V_{G8} = n \emptyset_t [F(i_{f9}) - F(i_{if8})] \quad (7)$$

Since the M8-M9 pair is biased by the M10-M11 mirror, $i_{f9} = i_{f8} = K_4K_5$. This circuit generates a PTAT voltage independent of the inversion region, as long as the inversion levels i_{f8} and i_{f9} themselves are kept constant. This can be achieved by biasing the differential pair with a current $I_{DIFF} = K_6I_{SQ}$, that can be obtained by mirroring the current I_{D1} of the V_{T0} extractor of Eq. (7) then becomes

$$V_{DIFF} = n\emptyset_t [F((K_4K_5K_6 \div (1+K_4)S_8)) - F((K_6 \div (1+K_4)S_8))] \quad (8)$$

Since sub threshold slope n varies slightly with process and temperature, this voltage is less ideal than that generated by the self-cascode (6).

D. Voltage Reference Circuit

The proposed voltage reference can be seen in Figure.4 which composed of transistors M1-M7 which forms the threshold voltage extractor, transistors M3-M4, the self-cascode PTAT generator and the unbalanced differential pairs which are made of transistors M8-M17, and they are sized exactly the same to produce a total PTAT voltage that is twice that of a single cell. Since we choose $i_{f1} = 3$, $I_{D1} = 3S_1I_{SQ}$, and this current is mirrored to bias the rest of the circuit through PMOS transistors M5-M7, M12 and M17.[9]

The reference voltage V_{REF}, at the gate of M13, is the sum of a CTAT term given by (4) and twice the PTAT term given by (7),

$$V_{REF} = V_{G1} + 2V_{DIFF} = V_{T0} + 2\, n\emptyset_t [F(i_{f9}) - F(i_{if8})] \quad (9)$$

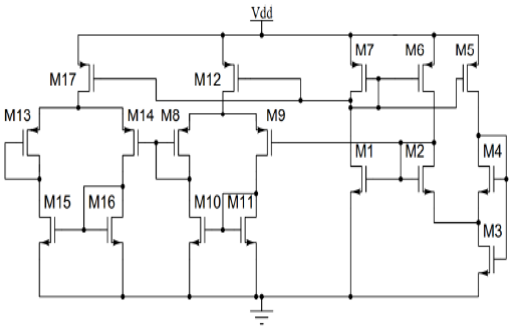

Fig 4. Proposed voltage reference circuit

III. CMOS VOLTAGE REFERENCE USING CURRENT COMBINATION CIRCUIT

The proposed circuit consist of three parts. The first part is composed of transistors M1, M3and R1for generating the current with negative temperature coefficient (I_{CTAT}), second part is composed of transistors M2and R2forgenerating the current with a positive temperaturecoefficient (I_{PTAT}) and the last part is current mirror circuitwhich is consisted of transistors M4, M5and M6. The M4isdefined for summing the current of $I_{CTAT}$and I_{PTAT}which is independent of temperature and mirrored to the M6for generating the voltage reference (V_{ref}).

Transistors M1 and M3 are defined to operate in saturation and weak inversion region, respectively. Then, the drain current of M1 is given by

$$I_{DM1} = \frac{1}{2} m_p C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \quad (10)$$

The gate-source voltage of M3 (Vgs_{M3}) is given by

$$V_{gs\,M3} = nV_T \ln [I_{ds3} L_3 \div I_t W_3] + V_{th} \quad (11)$$

Where V_T is the thermal voltage,

$$V_T = \frac{kT}{q} \quad (12)$$

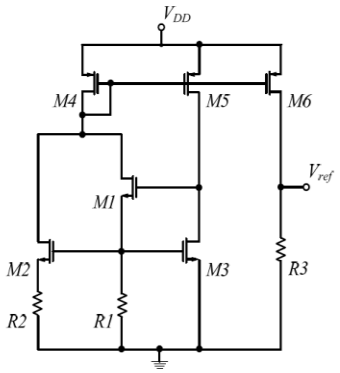

Fig.5. Voltage reference circuit using current combination circuit

Where kis the Boltzmann's constant (1.38 x10-23 J/K), qis electric charge (1.6 x10^{-}19C)and Tis absolutetemperature. The drain current of M3which is in termof exponential can be expressed as

$$I_{ds3} = I_t \frac{W3}{L3} e^{q(V_{gsM3} - V_{th}) \div nkT} \quad (13)$$

Where $V_{th}$is the threshold voltage, W3and L3is channel width and channel length of MOS transistor, respectively

$$I_t = 2nm_n c_{ox} (kT/q)^2 \quad (14)$$

Where $I_t$is the saturation current of the MOS transistor, *n* is the slope factor, Coxis the gate oxide capacitance per unit area and $\mu$is the electron mobility, Substituting equations of V_T, I_{ds3} and I_t into$V_{gs\ M3}$, then differentiation can be written as

$$\frac{\partial VgsM3}{\partial T} = \frac{VgsM3}{T} - 2n\frac{k}{q} \quad (15)$$

The Vgsof MOS transistor M3will be decreased when increasing the temperature which is called $V_{CTAT}$and the $I_{CTAT}$is expressed by

$$I_{CTAT} = \frac{VgsM3}{R1} \quad (16)$$

Transistor M2is operates in weak inversion region and VR1= VGS2+ VR2. Therefore the voltage drop across R2can be written as

$$V_{R2} = nV_T \ln m \quad (17)$$

I_{R2} is proportional to $V_T$and m is aspect ratio of MOS transistors M2 and M3

$$I_{PTAT} = I_{R2} = \frac{nKT}{R2q} \ln m \quad (18)$$

The current mirror circuit is composed of transistors M4, M5 and M6. The MOS transistor M4 is defined for summing the current of $I_{CTAT}$and I_{PTAT} which is independent of temperature, can be written as

$$I_{ref} = I_{CTAT} + I_{PTAT} \quad (19)$$

Substituting I_{PTAT} and I_{CTAT} into I_{ref} can be obtained

$$I_{ref} = \frac{VgsM3}{R1} + \frac{nVT}{R2} \ln m \quad (20)$$

The current $I_{ref}$is mirrored from M4 to M6, then the reference voltage can be written as

$$V_{ref} = I_{ref} R3 \quad (21)$$

By adjusting the resistance value of R3, we will be able to achieve low temperature coefficient [12].

IV. NOISE ANALYSIS

Thermal noise results from the use of the feedback resistors, MOSFET and bipolar transistors. Flicker noise is exclusively introduced by the MOSFET transistors, where it is directly proportional to their transconductance and to the squared closed-loop gain. Shot noise results from the use of bipolar transistors to generate the output bandgap voltage reference, and increases proportionally to the number of charges passing through the junctions. In this work, shot noise can be negligible because of absence of bipolar transistors. Not only thermal and flicker noise is present in resistors and MOSFET transistors, but the bipolar transistors also introduce shot noise due to their potential barriers, along with thermal noise. Noise reduction effort must target specially the bandgap core. In the remaining blocks it is important to use large transistors and minimize the use of resistors in order to reduce flicker and thermal noise.

V. RESULTS

In this section results of the proposed voltage reference circuits and the plot of the noise analysis of two different voltage reference circuits are presented. These circuits are implemented in cadence software. The performance of the proposed circuits is analysed through 180nm CMOS technology in virtuoso. Both the output voltage reference is varied over a temperature range of -25℃ to 50℃.

A. Simulation Results Of Voltage Reference Circuit Using Self Cascode Ptat Generator

Figure 6 shows the simulation result of VRC using self cascade PTAT generator. The design methodology and simulation results for a 180nm CMOS process are presented. It allows a reference voltage of 632mV achieving a temperature coefficient of 72ppm/℃ for the temperature range of -25℃ to 50℃.

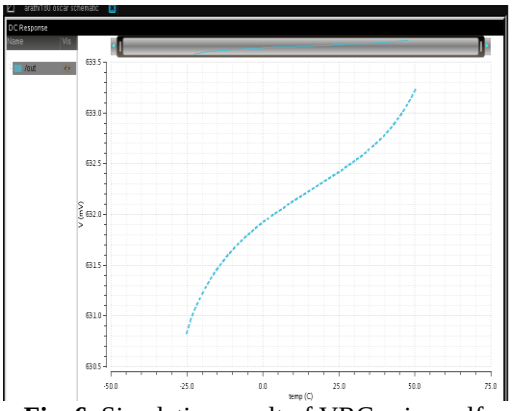

Fig. 6. Simulation result of VRC using self cascaode PTAT generator

B. Simulation results of voltage reference circuit using current combination circuit

Figure 7 shows the simulation result of VRC using current combination circuit. The design methodology and simulation results for a 180nm CMOS process are presented. It allows a reference voltage of 519mV achieving a temperature coefficient of 7ppm/℃ for the temperature range of -25℃ to 50℃.

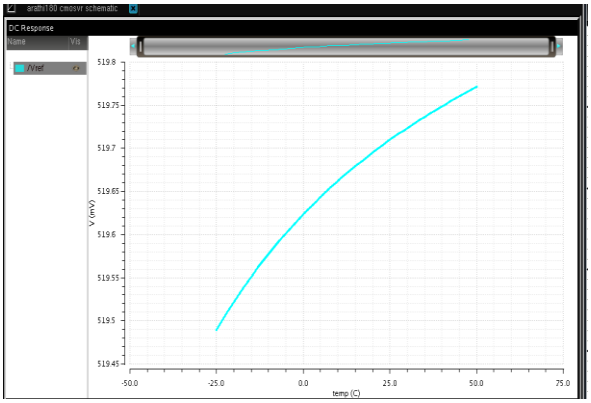

Fig. 7. Simulation result of VRC using current combination circuit

C. Simulation result of i_{ptat}

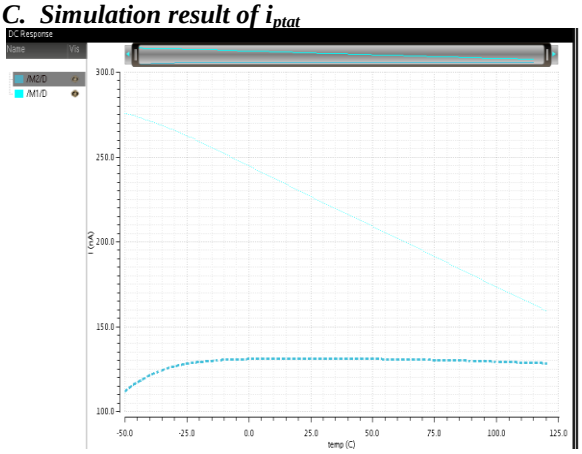

Fig. 8. Simulation result of I_{PTAT}

D. Simulation result of i_{ctat}

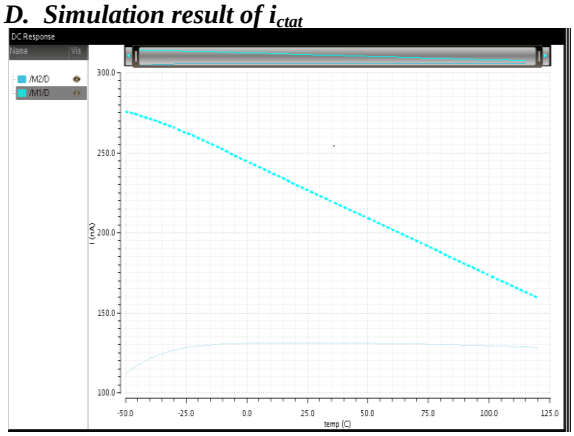

Fig.9. Simulation result of I_{CTAT}

E. Simulation results of noise analysis of vrc using self cascode ptat generator

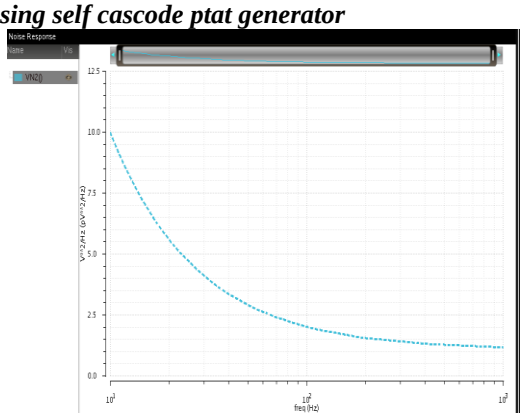

Fig.10. Noise analysis of VRC using self cascode PTAT generator

F. Simulation Results Of Noise Analysis Of Vrc Using Current Combination Circuit

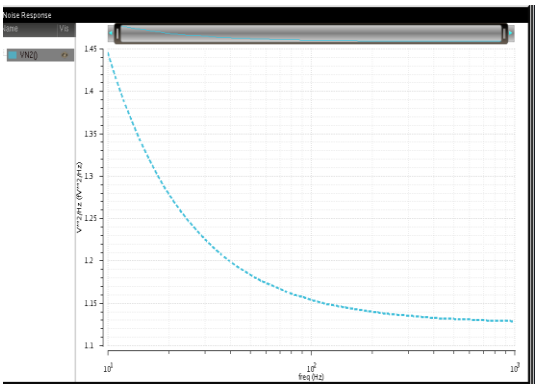

Fig.11. Noise analysis of VRC using current combination circuit

Table I Performance Comparison

	VRC using self cascade PTAT generator	**VRC using current combination circuit**
Technology	**180 nm**	**180nm**
Temperature	**-25 to 50℃**	**-25 to 50℃**
V_{REF}	**632mV**	**519mV**
Temperature coefficient	**72 ppm/℃**	**7 ppm/℃**
Vdd	**0.7-1.2V**	**0.5-1.2V**
Output Noise	**2.5-10Pv^2/Hz @10-1000Hz**	**1.15-1.45Fv^2/Hz @10-1000Hz**

VI. CONCLUSION

This paper focuses on the optimization of temperature coefficient and noise analysis of voltage reference circuits. From the simulation results, it is clear that the temperature coefficient can be reduced to a great extend in one voltage

reference. When comparing the noise analysis of both the circuits, noise of voltage reference circuit using self cascode PTAT generator is more. Therefore voltage reference circuit using current combination is better in terms of both temperature coefficient and noise.

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