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Design Of High Performance CMOS Dynamic Latch Comparator

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ABSTRACT
High performance analog to digital converters (ADC), memory sense amplifiers, and Radio Frequency identification applications, data receivers with less area and power efficient designs has attracted a broad range of dynamic comparators. This paper presents an ameliorate design for a dynamic latch based comparator in attaining high performance. The comparators accuracyis mainly defined by two factors they are speed and power consumption. The latch based comparator has two different stages encompassing of a dynamic differential input gain stage and an output latch.The output node in the differential gain stage of proposed comparator requires lesser time to regain higher charge potential. The proposed comparator hasbeen designed and simulated using 130nm CMOS 1P2M technology by using mentor graphics tools with a supply voltage of 1V. Proposed dynamic latch comparator iscompared with existing conventional dynamic latch comparator and with other comparators and the results are discussed in detail.

Keywords:Analog to digital comparator (ADC), Dynamic latch comparator, memory sense amplifiers.

I. INTRODUCTION

Due tohighspeed,less-power consumption, high-input impedance and full-swing output, CMOS dynamic latched comparators are very attractive for many applications such as high-performance analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. A small input-voltage difference is converted into full-scale digital level in a short time by using the positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in conventional dynamic latched comparators. However, the accuracy and the performance of the dynamic latched comparators is restricted by the random offset voltage witch results from device mismatches such as threshold voltage Vth, current factor β(=μCoxW/L),and internal-parasitic/external load capacitance mismatches [2–4]. The most important design parameterin designing dynamic latched comparator is offset voltage which shows a large effect on performance of the comparator. Fig. 1 shows the block diagram of high speed comparator which consists of pre-amplifier and regenerative latch stage.The pre amplifier stage is used to decrease the latch offset voltage and it can also amplify a small input voltage difference to a large output voltage. This large output voltageis to overcome the latch offset voltage which in turn reduces the kickback noise [5]. There will be large static power consumption for large bandwidths because of the preamplifier stage and the intrinsic gain also reduced due to the reduction of the drain-to-source resistance ($r_{ds)}$ due to the continuous technology scaling [6]. Therefore, for the high-performance CMOS applications, a dynamic comparator without pre-amplifierstage is highly desirable. The conventional comparators suffer a lot of accuracy issues like random offset errors and internal parasitic/external load capacitances mismatches [14] [15] [16]. To overcome this inaccuracy issues and to improve the performance dynamic latch based comparators without preamplifier stage are preferred [17]. For an analog to digital converter with a feature of high-performance, a comparator without the preamplifier is preferred since it suffers from high static power dissipation[18].

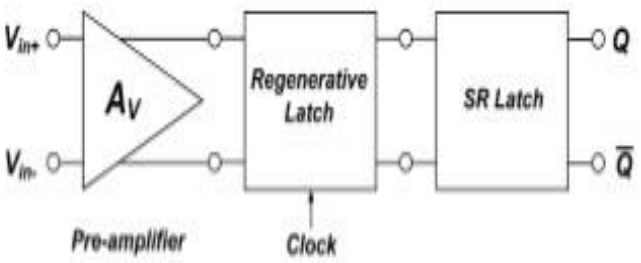

Figure1: Typical block diagram of a high speed voltage comparator.

In the paper the sections are considered as fallows: Section 2 offers an overview of the dynamic latch comparators and also disscuss about their advantages and downsides, and Section 3 describes the proposed dynamiclatched comparators and their operation. Section 4 discusses the overall architecture of high-performance 3-bit flash analog to digital converter(ADC). Section 5 discusses about simulation results and section 6 concludes the paper.

II. DYNAMIC LATCH COMPARATORS

The dynamic latch comparator shown in figure 2(a) is most widely used because it has many advantages such as high-speed, zero static-power consumption, high input-impedance and fullswing output [10, 11]. During the pre-charge phase both the output nodes are charged to power supply voltage and during the evaluation phase the output of the comparator depends on the differential input. The main drawback of this comparator is it consists of only one tail current transistor M11 which is used to control the currents flowing through both the differential input pair (M10 and M5) and the latch (M3,M4,M8,M9). The size of the tail transistor M11 should be increased to increase the drive currents of the latch. But, if we increase the size of the tail transistor M11, the time duration of the input transistors which operate in the saturation region will be reducedbecause the transistors operate less time in saturation region full amplification of input voltage is not achieved.

To avoid these downsides, the comparator is designed using separate differential input-gain stage and output-latch stage which are shown in Fig. 2(b) [12]. Due to this stage separation the comparator will be operated at low supply voltage (VDD) and can also have stable offset voltage and increased speed. When the clock is low both the output nodes discharges to ground and when the clockis high the output depends on the differential input node voltages. The main pitfall of this comparator is it uses both clock (clk) and clockbar(clkb) signals, for proper operation of the circuit accurate timing relation must be maintained. Due to the effect of clock skew between Clkb and Clk signals the performance of the circuit is affected. In additional to the clock signal clkb signal is used which an additional inverter to generate the clock needs signal Clkb which leads to increase in area, power and delay. If Clkb is lagging the Clk, it leads to increased delay and If Clkb is leading the Clk, it results in increased power dissipation.

The comparator from [7] is shown in Fig. 2(c), where the Clk skew problem is eliminated by replacing Clkb with differential nodes. With the elimination of clock skew problem the performance of the comparator is not affected and the load due the clock is also reduced. Due to the presence of large differential nodes capacitance and double transconductance (gm) the noise and input referred offset voltage are reduced. But the main drawback is increased delay due to the weak current driving capability of the output load due to the fact that the transistors M1and M2 uses differential node voltage, which shows the slow exponential decaying shape. Since the single tail-current transistor (M1) in the comparator1 of Fig. 2(b) is divided into two transistors (M1 and M2) in the comparator 2 of Fig. 2(c) the drive current of the output node is reduced to half.

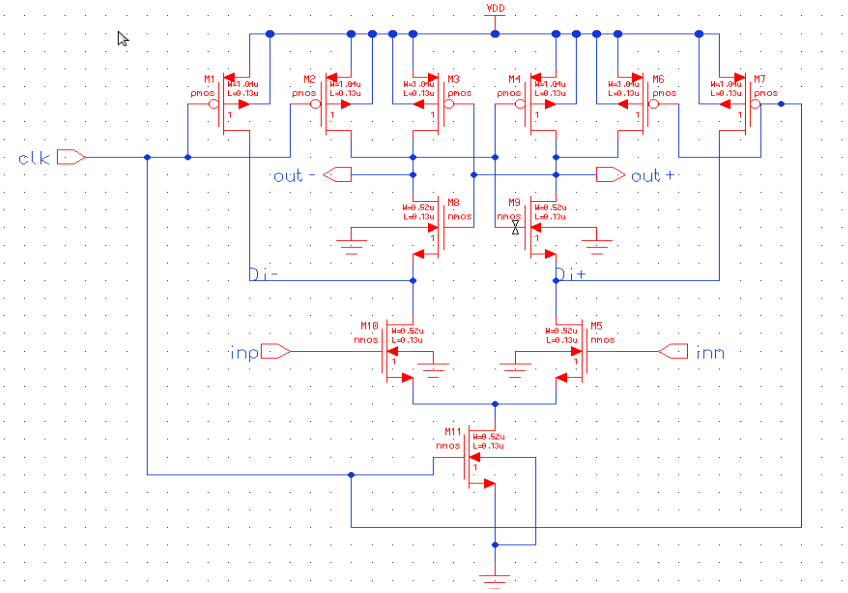

Figure 2 (a): Conventional dynamic latch comparator [10, 11]

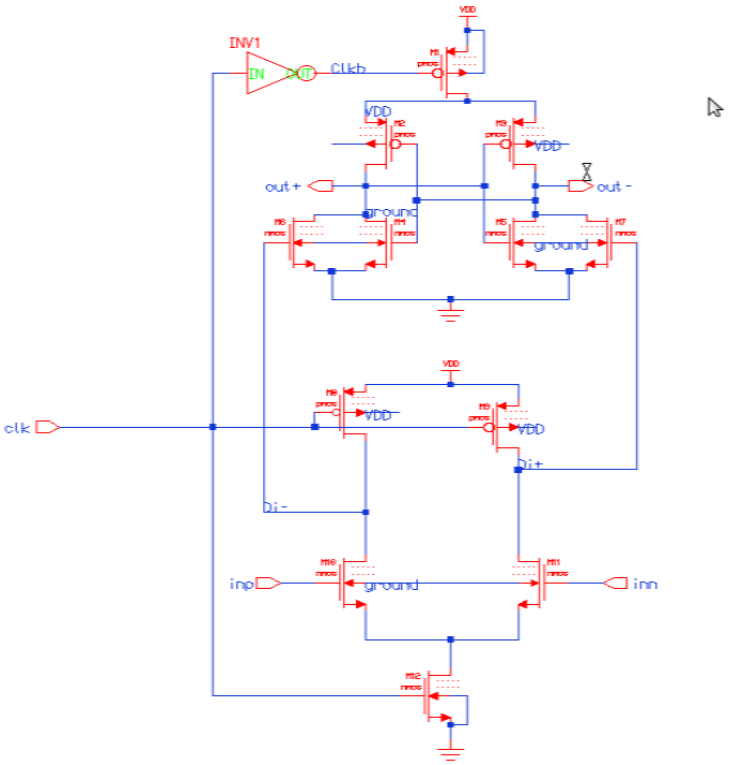

Figure 2(b): Comparator 1[12]

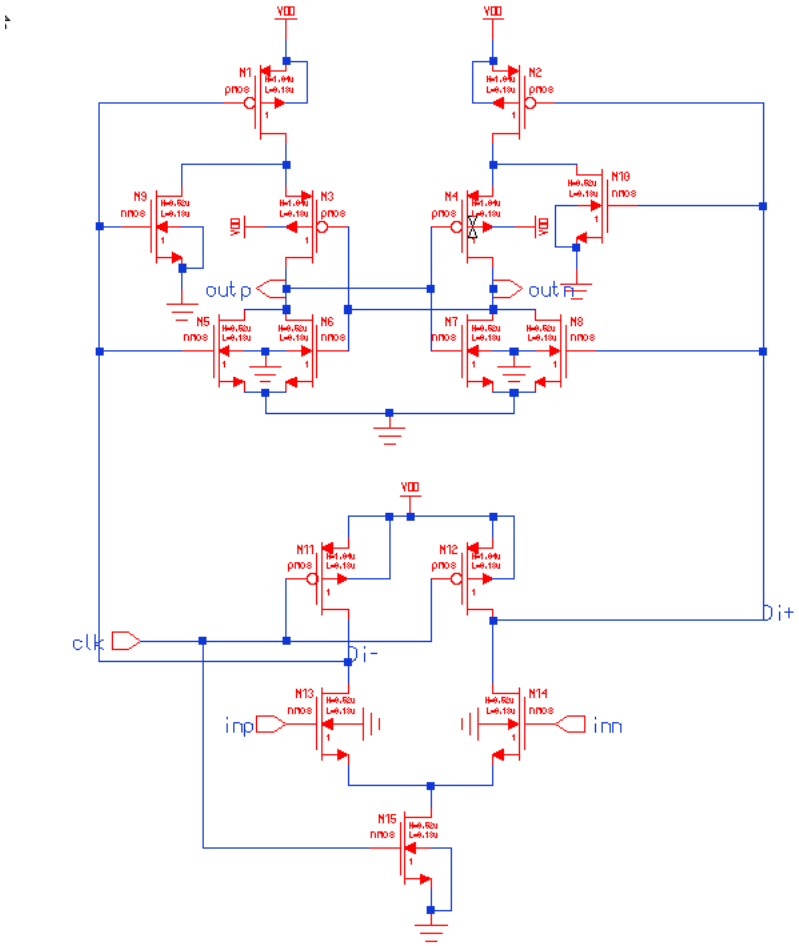

Figure 2(c): Comparator 2[7]

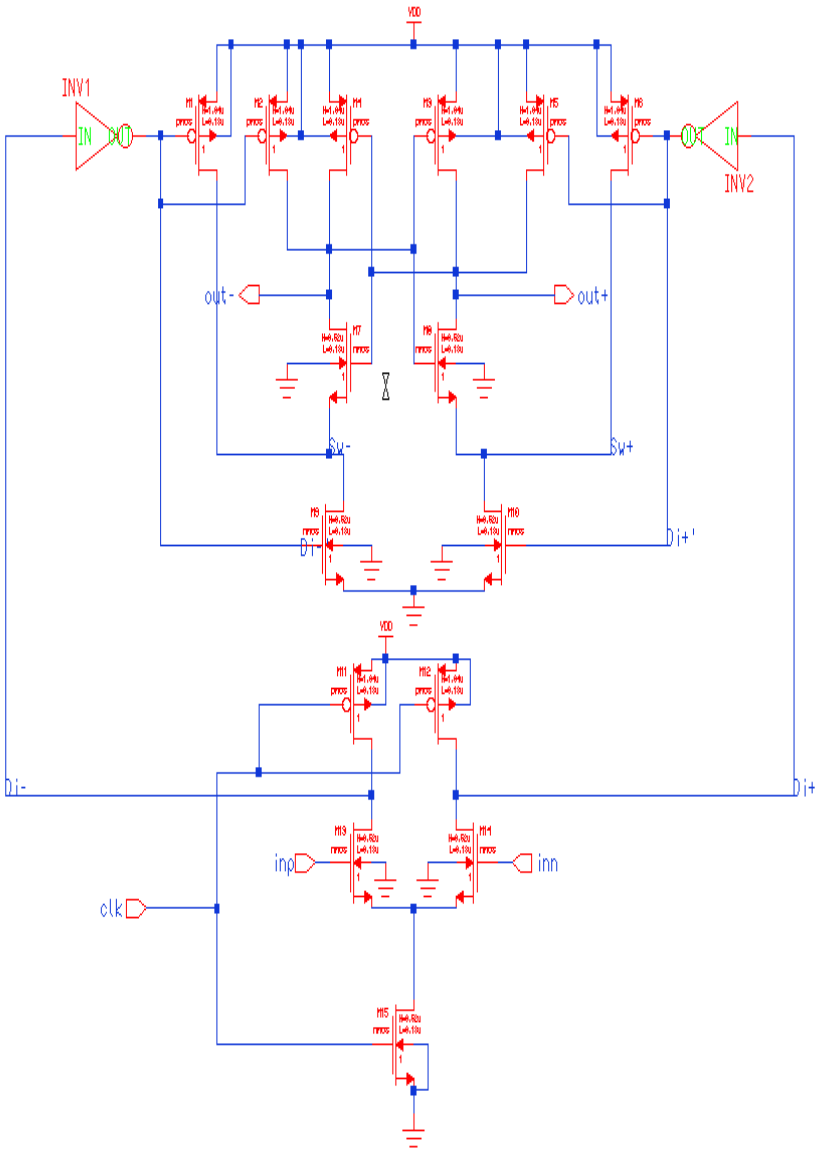

Figure 2(d): Comparator3 [1]

Thecomparator3 [1] provides less input offset voltage and used to attain high performance when compared with the previous comparators. The output nodes of the comparator are charged to VDD during pre-charge (or reset) phase (Clk= 0 V). During the evalution phase comparison of the input voltage takes place and the output depends on the magnitude of input voltage. The main advantage of the comparator3 is it can deliver bigger load currents and can also operate at lower power supply voltages. The main drawback of this comparator is it require more time to reset the output nodes to supply voltage which slower the process of comparison which in turn limits the speed of comparator.

III. PROPOSED COMPARATOR

The proposedcomparatoris shown in figure3 (a). The major advantage of thecomparatorsis they offer high performance and remove the dead time issues. The dynamic power consumption of the circuit is reducedbecause of the switching transistors M16, M18and the control transistorsM12, M13are used to charge the output nodes to VDD. During the reset phase the output nodes are charged to VDD. During the evaluation phase the output depends on the magnitude of the differential input voltages.

During the evaluation phase the transistor which has the higher input voltage will make one of the control transistors high and the other control transistor is off. As one of the differential nodes ishigh always this in turn keeps the one of the output nodes charged to VDD. The main advantage of the proposed comparator is enhanced latch transconductance.

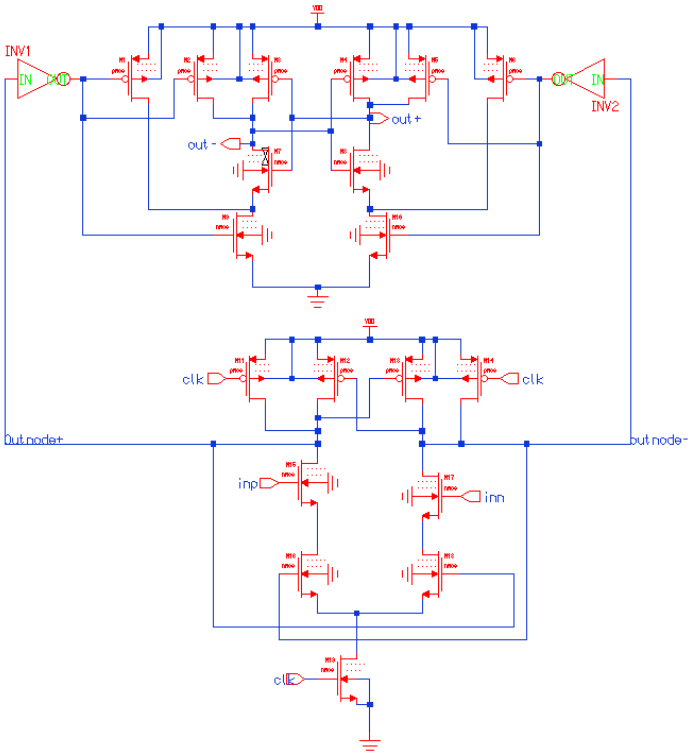

Figure 3(a): Proposed comparator

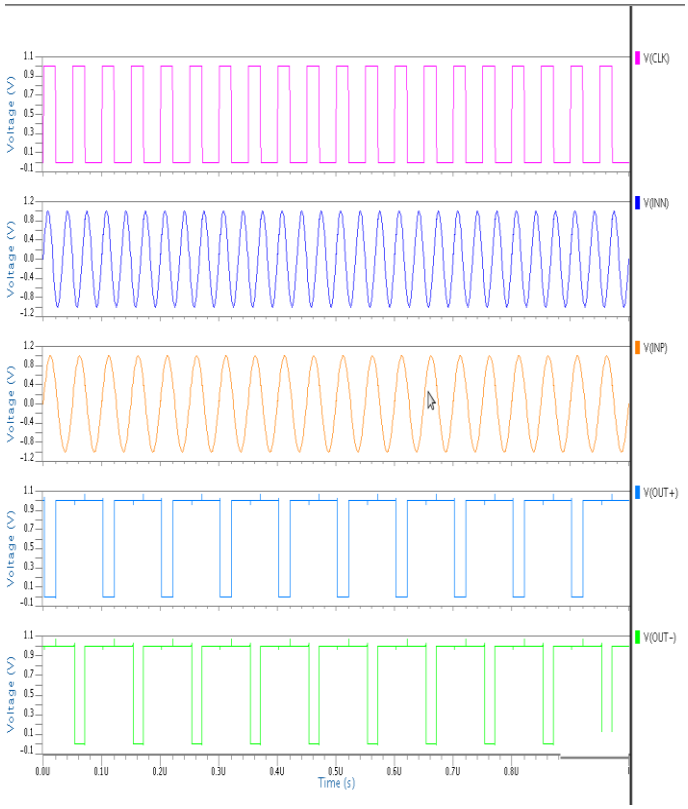

Figure 3(b): Signal behaviour of proposed comparator

Figure 3(b) shows the transient response of the proposed comparator, sinusoidal signal is given as input for both inputs INN and INP with variable frequency and same amplitude. During pre-chargephase both the output nodes charge to VDD and during evaluation phase the output depends on the differential input voltage.

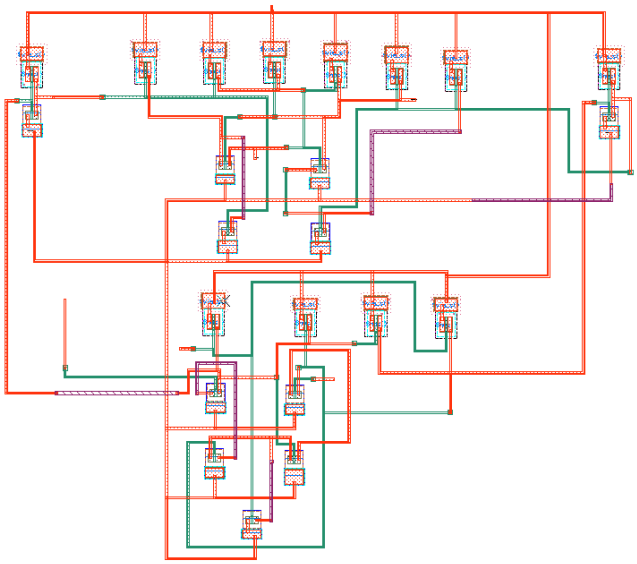

Figure 3(c). Layout of proposed comparator

IV. APPLICATION

4.1 Flash A/D Converter Design

The flash ADC architectures are also called as parallel ADCs, in which the input signal is sampled simultaneously by using multiple comparators to digitalize the analog signal. The flash A/D converters are considered as fastest due to their parallel architecture and they are also suitable for high bandwidth applications. The flash A/D converter architecture consists of 2^N resistors ,2^N-1 comparators and the thermometer to binary code converter which is used at the output of an A/D converter is used to convert the data into more compact binary code before transmitting as data to the external circuits, where" N" is the number of bits. Due to the presence of large number of resistors and comparators it consumes a lot of power and occupies large area. As the resolution of the converter increases the power consumption also increases. The power consumption can be reduced by using a low power comparator because the converters speed and power consumption mainly depends on the comparator design. Few applications of flash ADCs are satellite communication, radar processing, data acquisition, samplingoscilloscopes, and high-density disk drives. A typical 3-bit flash ADC block diagram is shown in Figure 4(a), the resistor ladder network is formed by 2^N resistors, which is used to generate the positive reference voltages for each comparator.

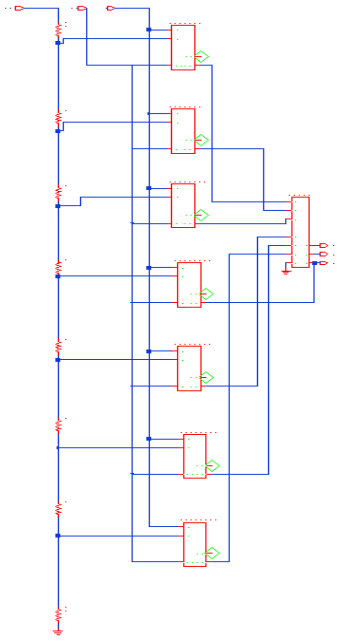

Figure4(a): 3-bit Flash A/D converter

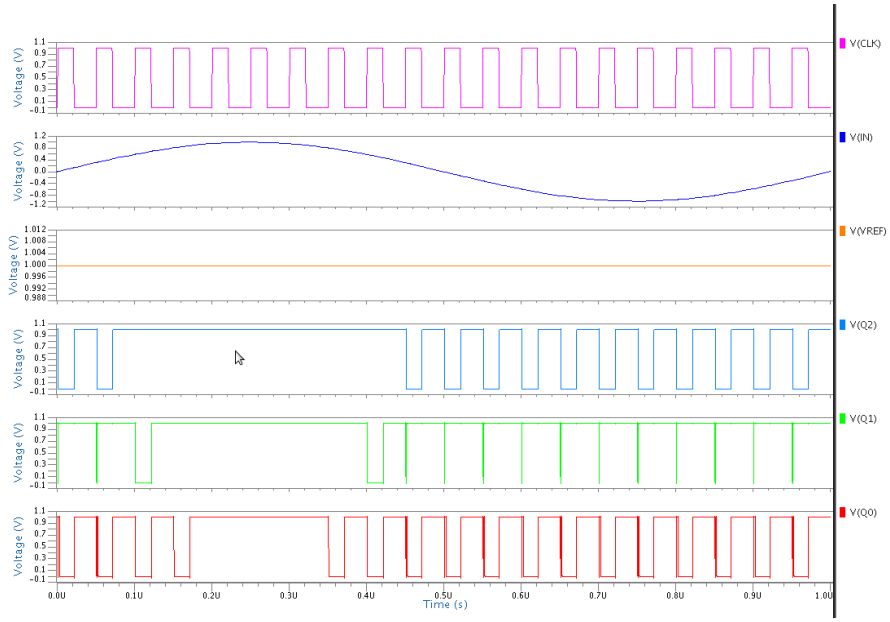

Figure 4(b): Flash A/D converter output waveforms

Figure 4(b) shows the Flash A/D converter output waveforms, When clock is low the output of all comparators is high and Flash A/D converter output is also high i.e. bits Q2, Q1, Q1 are high, when clock is high comparison is done and according to the output obtained by the comparator which is fed to the thermometer to binary encoder respective output (Q2 Q1Q0) is obtained.

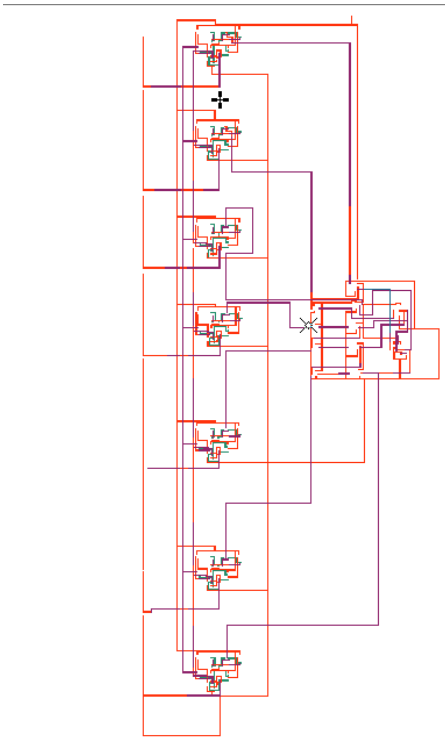

Figure 4(c): Simplified layout of the Flash A/D converter

V. SIMULATION RESULTS

In order to compare the proposed comparator with the conventional dynamic latch comparator and other comparators, all circuits have been simulated in 0.13µm CMOS technology with VDD =1V. Table I compares the performance of the proposed comparator with differentcomparators. Table IIsummarizes the performance of the Flash A/D converter design using proposed dynamic latch based comparator.

TableI: Comparison of different comparators

Specification	Conventional dynamic latch comparator	Comparator1	Comparator2	Comparator3	Proposed comparator
Technology	130 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS
Supply voltage	1V	1V	1V	1V	1V
Number of transistors	11	14	15	19	23
Delay	22.43ns	3.35ns	3.07ns	3.39ns	2.392ns
Power dissipation	0.49nw	1.725nw	0.9nw	3.099nw	3.098nw

Table II: Performance of Flash A/D Converter

Specifications	Proposed comparator
Technology	130nm CMOS
Supply voltage	1V
Resolution	3 bit
Delay	1.25ns
Power dissipation	142.89µw

VI. CONCLUSION

The proposed comparator isdesigned and simulated using 130nm CMOS 1P2M technology. Different architecture of comparators were studied and analysed as per the power consumed, speed and size of the comparator. The proposed comparator can be used to drive large capacitive loads by using only one phase clock signal. The dead time required to reset the output nodes was also removed by the proposed design in the input differential stages. The performance and the conversion speed of the Flash A/D converters also increases by using the proposed comparators. The simulation results show that the proposed comparator achieves high performance when compared to the conventional comparators at approximately same area.

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