RESEARCH ARTICLE OPEN ACCESS

Effect of Threshold Voltage on Various CMOS Performance Parameter

Mr. Abhishek Verma[1], Dr. Anup Mishra[2], Archana Singh[3], Ankita Agrawal[4]
[1]Assistant Professor, [2]Professor, [3,4]Scholar Bhilai Institute of Technology, Durg (C.G.)

Abstract

SiO_2, once thought of as the most precious element in the design of CMOS circuits has not lived up to the expectations of being the perfect gate oxide. Efforts have been made to replace it with High K oxides such as Lanthanum Oxide (La_2O_3), Hafnium Oxide (HfO_2) and many more. This review covers the problems faced by the High K oxides, one of them being escalation in threshold voltage which results in increased power dissipation. The solution to the above stated problem is to reduce the threshold voltage by several techniques, also covered in the review. Effect of threshold voltage on leakage current and power and reliability of CMOS are also taken under consideration.

I. Introduction

As the semiconductor industry approaches limits of traditional silicon CMOS scaling, the introduction of performance boosters such as novel materials and innovative device structures has become necessary for the future of CMOS scaling.

The progress in complexity and efficiency of CMOS circuits has been achieved throughout the last decades by scaling the geometric dimensions of the metal oxide semiconductor field-effect-transistor. This scaling has to be accompanied by a decrease in the gate oxide thickness in order to maintain electrostatic control of the charges induced in the channel[1].With technology scaling, power supply and threshold voltage continue to decrease to satisfy high performance and low power supply.[2].

In energy- constrained system, low power design is essential for system lifetime and extending battery. Lowering voltage supply decreases energy dissipated quadratically, but causes increase in delay. In order to satisfy aggressive performance requirements demanded by applications, the threshold voltage should also be lowered, to have both low power operation and high performance. However there is a cost of higher static power dissipation due to high leakage current.[2].

The main problem in scaling is, since leakage currents are set by the transistor's threshold voltage, there is a limit to how low one can make a transistor's V_{th}. With V_{th} fixed, changing V_{DD} simply trades off energy and performance. [4]

Poor future power scaling and previously applied performance scaling techniques has made power the number one problem in modern chip design. Designers can no longer focus on creating the highest performance chips because it is nearly guaranteed that the highest performance circuit will dissipate too much power. Instead, designers must now focus on power efficiency in order to achieve high performance while staying under their power constraints. [4]

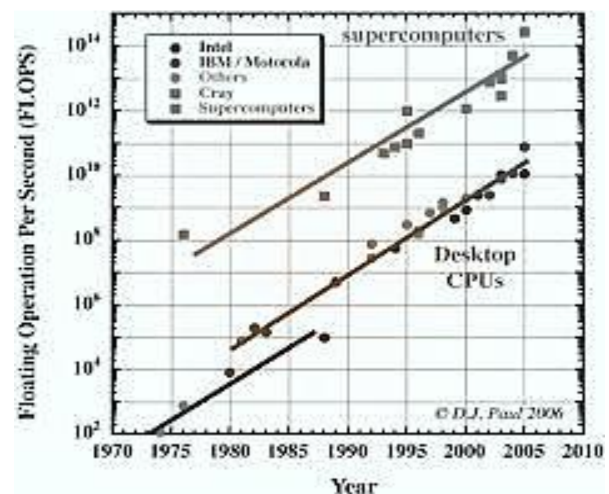

Figure 1. The scaling of feature size, gate length, and oxide thickness according to the 2003 Semiconductor Roadmap.[3]

II. Threshold voltage

Threshold voltage is the minimum voltage level at which the transistor turns ON and drain to source current (I_{ds}) starts flowing. It is the gate voltage leading to strong inversion as shown in figure2. The term inversion means that the surface is inverted from P to N type or has become electron rich. With the CMOS scaling it is becoming more and more difficult to sustain supply and threshold voltage scaling to provide required performance increase, to limit energy consumption, control power dissipation and maintain reliability. It has become

necessary to replace the SiO_2 with a physically thicker layer of oxides of higher dielectric constant (high κ) such as aluminium oxide (Al_2O_3), titanium dioxide (TiO_2), tantalum penta-oxide (Ta_2O_5), hafnium dioxide (HfO_2), hafnium silicate ($HfSiO_4$), zirconium oxide (ZrO_2), zirconium silicate ($ZrSiO_4$), and lanthanum oxide (La_2O_3).

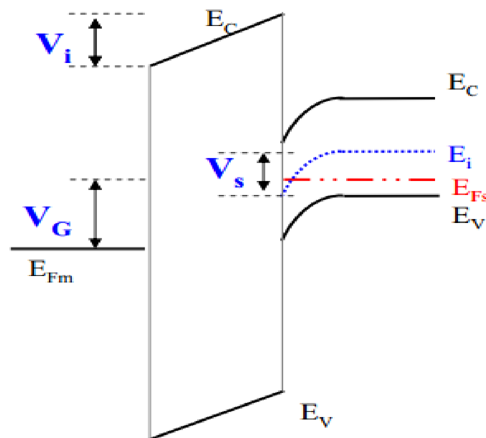

Figure 2: Energy band diagram of MOS system at inversion condition.[5]

The major problem with high κ oxide is that it results in high threshold voltage. This high V_{TH} is due to flat band voltage roll off at lower EOT. Flat band is the bias condition where the energy band i.e. conduction band and valance band of the substrate is flat at the Si–SiO_2 interface as shown in Figure 3 [5].

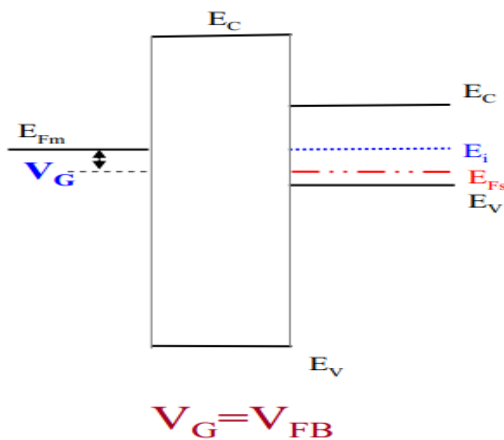

Figure 3: Energy band diagram of the MOS system at the flat-band condition.[5]

By Poisson's equation, the FB voltage measured for a range of film thickness t obeys

$$V_{FB} = \emptyset_{ms} + \frac{Qt}{K\varepsilon_0} \quad (2.1)$$

Where,

$\emptyset_{ms}$ is the difference in work functions of the Si and the gate electrode, Q is the interface fixed charge (or trapped charge) density in the film, and K is its dielectric constant.[6].

$$V_{GS} = V_{FB} + V_S + V_i \quad (2.2)$$

Where,

is gate to source voltage, V_S is the surface potential, V_i is the voltage drop across oxide/insulator.

$$V_i = \frac{Q_d}{C_i} \quad (2.3)$$

Q_d is capacitor charge and C_i is capacitance.

$$V_S = \frac{qN_A W^2}{2\varepsilon_S} \quad (2.4)$$

$$Q_d = qN_A W = (2\varepsilon_S qN_A V_S)^{\frac{1}{2}} \quad (2.5)$$

At strong inversion, $V_{GS}=V_{TH}$, $V_s=2\Phi_b$,
From equations (2.2),(2.3),(2.4)&(2.5),threshold voltage[5] is given as:

$$V_{TH} = V_{FB} + 2\emptyset_b + (2\varepsilon_S qN_A 2\emptyset_b)^{\frac{1}{2}}/C_i \quad (2.6)$$

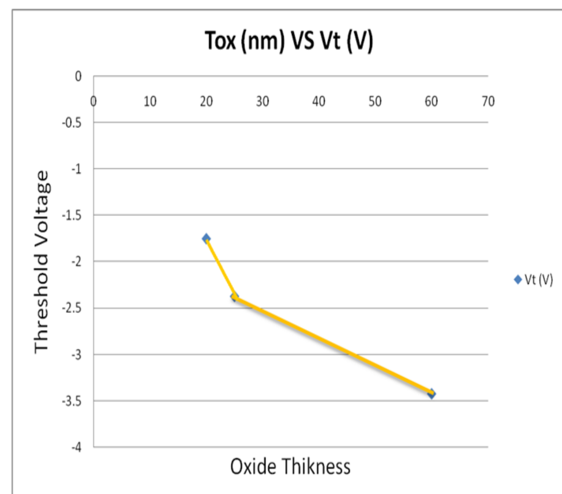

Figure 4: Threshold voltage variation at different oxide thickness [7]

III. Effect of Threshold Voltage Reduction on Power and Leakage Current

The first order model of energy and delay of CMOS circuit showed that lowering the threshold voltage is generally advantageous, especially when

transistors are velocity saturated and the nodes have high activity factor [10].

Power dissipation reduction has great importance in design of digital circuits. One technique for reducing power is to reduce supply voltage but for CMOS circuits, the cost of lower supply voltage is lower performance. Threshold voltage scaling can limit this performance loss but results in increased static power dissipation [10].

Static current which results from resistive path between power supply and ground, and dynamic power which results from switching capacitive loads between different voltage levels are two main sources of power dissipation in CMOS circuits. Short circuit current which results from both transistors in a CMOS inverter being on at the same time while input switches, is the third source of power dissipation in CMOS. The short circuit component is small and therefore we ignore it. Current sources and leakage current is responsible for static power when a transistor is nominally off. [1]
For a CMOS gate, the dynamic power is-

$$P=aCV^2f \quad (3.1)$$

Here, 'a' is activity factor of output node, C is total capacitance of the output node, V is the supply voltage and f is the operating frequency.
For a complex chip, the total dynamic power is sum of dynamic power of all gates. The resulting equation will be same as above. The submicron technologies with low threshold voltage will be very attractive for low power applications. By simply moving to a low V_{th} process, a designer could reduce the supply voltage and power without requiring a major change of the design, since the gate speed would not change .
The leakage current for a gate can be written as-

$$I_t=WI_ze^{(V_{th}/V_{st})} \quad (3.2)$$

Here W is the effective transistor width of the cell, V_{th} is the threshold voltage, I_z is the zero-threshold leakage current and V_{st} is the subthreshold slope. The dependence of I_t on drain voltage is ignored and also the leakage current in the reverse biased diodes [10].

IV. Effect of Threshold Voltage Variation on Reliability of CMOS Gates

Process variations are expected to have significant effects on performance of transistors. These variations affect the characteristics of transistors by changing their parameters. With rapid scaling in CMOS technology, there has been drastic change in process parameters. One of the essential parameter of transistor is threshold voltage. So far we have discussed the effect of variation of threshold voltage on power consumption. Another considerable effect associated with this variation is reliability of logic gates. A logic gate may either become faster or slower in performance depending upon change in its characteristics. In nanoscale CMOS devices, the reduced average number of dopant atoms in the channel of a transistor increases the effect of random dopant fluctuations on its threshold voltage to increase[8]. Figure 5 illustrates the effects due to process variations.

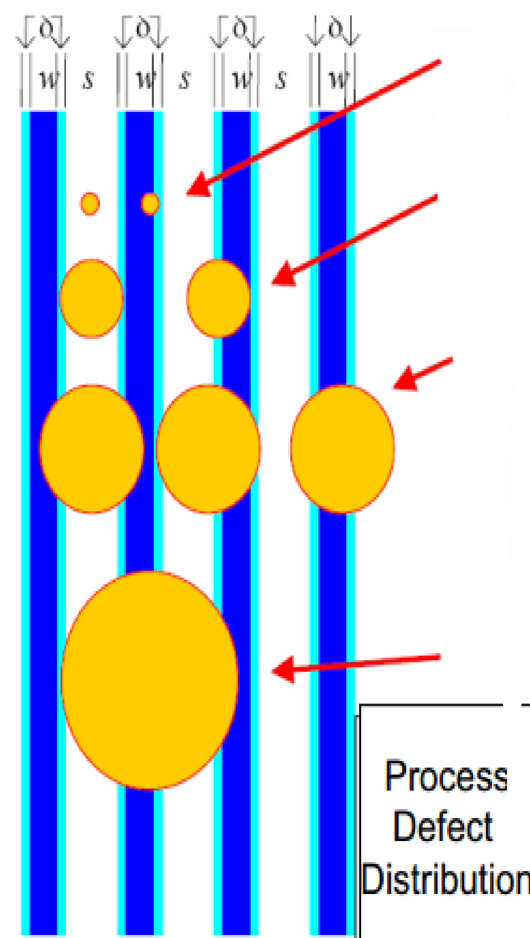

Figure 5: Illustration of process induced defects: size, location and impact on semiconductor reliability [9]

Depending on the defect size, location and distribution, technology scaling will increase the failure rate induced by the random defects, even with process improvements, which reduces defect size produced during semiconductor fabrication. This is because the same size of defects which are safe for older technologies may cause reliability concerns for

advanced technologies simply because of the physical scaling [9].

Monte Carlo simulations on CMOS technology, compares the effect of threshold voltage on reliability of gates. The results of the simulation are shown in figure 6 and 7.

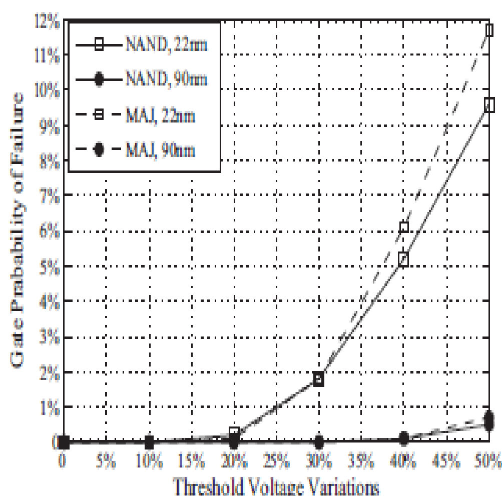

Figure 6: Average reliability of NAND-2 and MAJ-3 [10]

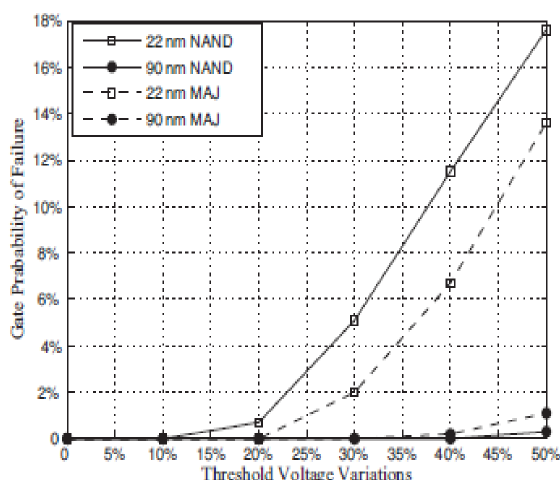

Figure 7: Worst case reliability of NAND-2 and MAJ-3 [10]

According to results of simulation, these gates can tolerate 40% of threshold variations at 90nm and 20% of threshold variations at 22nm.[10]

V. Threshold Voltage Scaling Technique

For the purpose of scaling, the conventional SiO_2 had been replaced by high k oxides. However these oxides when used in CMOS will lead to increase in threshold voltage levels. And it is desired that a device must have a low threshold voltage level such that supply voltage can be scaled down without degrading the speed. If both threshold voltage and supply voltage are scaled down.

Die-to-die parameter variations are caused by lot-to-lot and wafer-to-wafer differences in the processing temperatures, wafer polishing, the power dissipation and propagation delay of a CMOS circuit can be reduced simultaneously.

However with the threshold voltage scaling comes a primary limitation of exponential rise in sub threshold leakage current as well as increasing effects of die-to-die and within g, wafer placement, and the properties of the equipment used in the lithography process [9]. As gate length also reduces beyond 193nm, within-die parameter variations also become significant. These variations are difficult to control and do not scale.

Various threshold voltage scaling techniques have been proposed such that the effect of threshold voltage scaling on leakage current, die-to-die and within-die parameter variation is reduced. One such technique discussed in this paper is body bias circuit technique. In this technique the threshold voltage of the transistors is dynamically changed by varying the voltage of the body terminals during circuit operation.

The threshold voltage is typically adjusted during the fabrication by variation in doping concentration in the channel area. The body bias circuit technique can dynamically modify the threshold voltage during circuit operation. The threshold voltage can be increased or decreased depending upon the polarity of the voltage difference between the source and the body terminal. Depending on which the body bias can be of following types:

A. Reverse body bias.
B. Forward body bias.
C. Bidirectional body bias.

A. Reverse Body Bias

In this technique the threshold voltage is increased by applying a negative voltage across the source to substrate p-n junction as shown in figure 8. The variations of charge distribution under zero body bias and reverse body bias condition are depicted in figure 9.

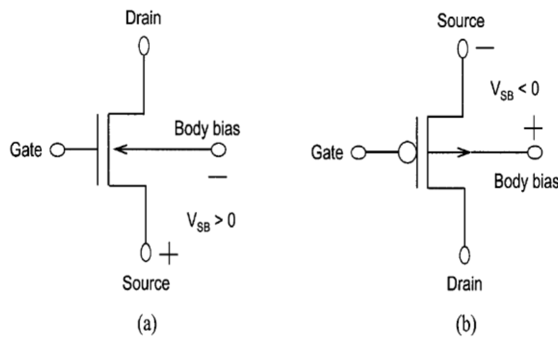

Figure 8: Reverse body bias technique.
(a) A reverse body biased NMOS transistor.
(b) A reverse body biased PMOS transistor.

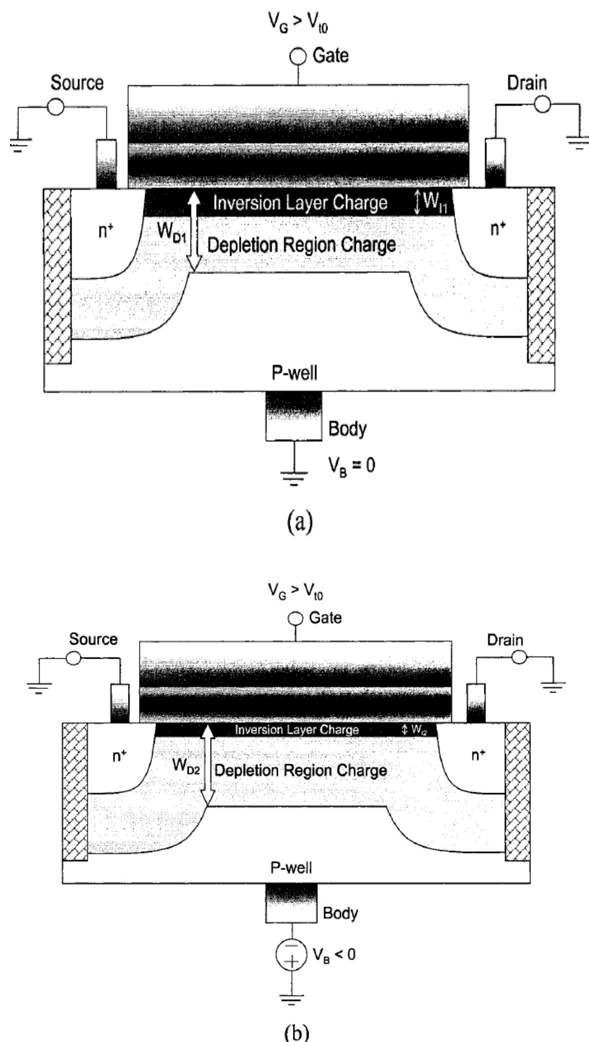

Figure 9: Effect of reverse body bias on the depletion region & inversion layer charge.
(a) A zero body bias NMOS transistor.
(b) A reverse body biased NMOS transistor.

In reverse biased condition, the width of the depletion region increases as shown in figure9.b. This increase in depletion width corresponds to an increase in the ionic charge in the semiconductor plate of the MOS capacitor [9]. To maintain the charge balance, the mobile charge in the inversion layer decreases, due to which the gate voltage needs to be increased to achieve a similar level of inversion as before. Thus the threshold voltage of a reverse body biased CMOS increases.

The reverse body bias technique also reduces the variations in speed and power characteristics due to fluctuations in supply voltage, temperature and die-to-die process parameters.

B. Forward Body Bias

Using this technique the threshold voltage can be reduced by applying positive voltage across the source to substrate junction as shown in figure10. The variation of charge distribution in depletion region and inversion layer is shown in figure11.

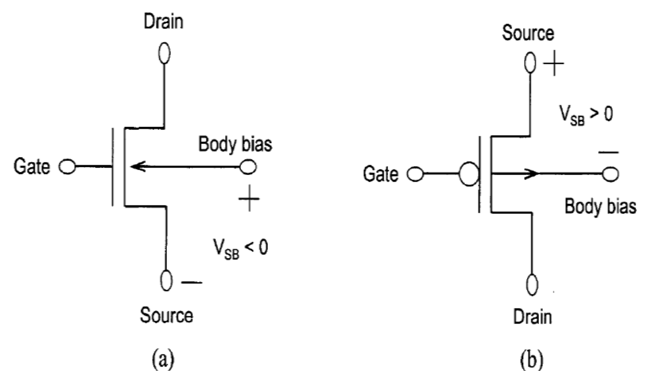

Figure 10: Forward body bias technique.
(a) A forward body biased NMOS transistor.
(b) A forward Body Biased PMOS transistor.

In this technique the width of the depletion region decreases which corresponds to a decrease in the ionic charge in the semiconductor plate of MOS capacitor. For maintaining the charge balance, the mobile charge in the inversion layer increases, as a result the gate voltage needed to achieve similar level of inversion as compared to zero biased MOSFET is hence reduced.

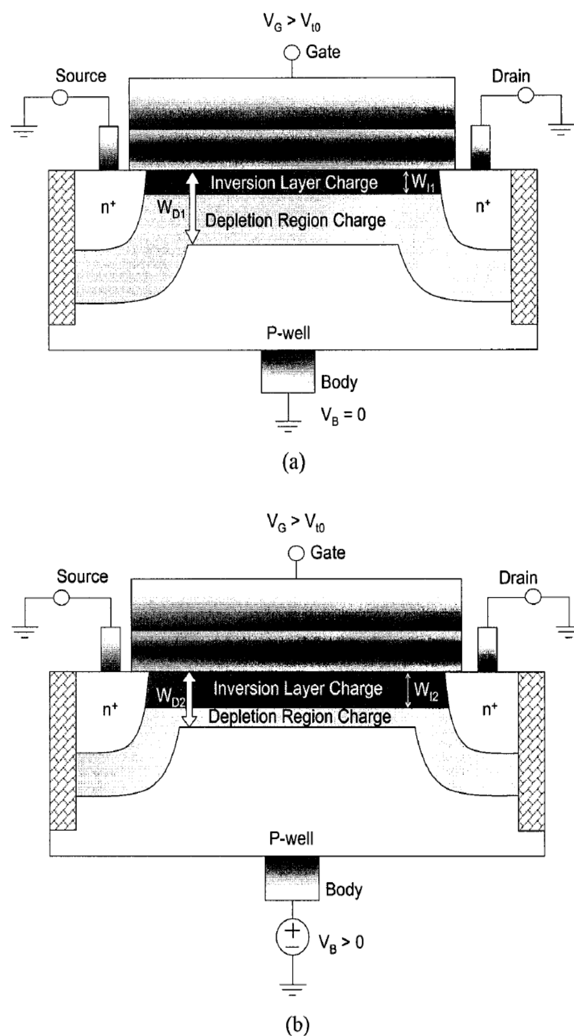

Figure 11: Effect of body bias on the depletion region and inversion layer charge in MOSFET.
(a) A zero body biased NMOS transistor.
(b) A zero body biased PMOS transistor.

This technique has more benefits as compared to reverse body bias technique. It is expected to become more common as compared to the previous method in future technology.

C. Bidirectional Body Bias

In this technique the zero body bias V_T of the transistor can be set to an intermediate value. This technique possesses the benefits of both the forward and reverse body bias techniques. For increasing the speed the threshold voltage can be reduce by forward body biasing and similarly to reduce speed and leakage power, the threshold voltage can be increased by reverse body biasing. This technique offers a wider choice of threshold voltages since the transistors will be initially set to an intermediate threshold voltage.

VI. Dependence of threshold voltage on various parameters

Four physical components of the threshold voltage are:

(i) The work function difference between the gate and the channel,
(ii) The gate voltage component to change the surface potential,
(iii) The gate voltage component to offset the depletion region charge, and
(iv) The voltage component to offset the fixed charges in the gate oxide and in the silicon-oxide interface.

- The work function difference between the gate and the channel reflects the built in potential of the MOS system, which consists of the p-type substrate, the thin silicon dioxide layer, and the gate electrode. Depending on the gate material the work function difference is
  for metalgate
  $$\varphi_{GC} = \varphi_F(\text{substrate}) - \varphi_M(\text{gate}) \quad (6.1)$$
  for polysilicon gate
  $$\varphi_{GC} = \varphi_F(\text{substrate}) - \varphi_F(\text{gate}) \quad (6.2)$$

This first component of the threshold voltage accounts for part of the voltage drop across the MOS system that is built-in.

- The externally applied gate voltage must be changed to achieve surface inversion i.e. to change the surface potential by $-2\varphi_F$ .This will be the second component of the threshold voltage.
- Component of the applied gate voltage is necessary to offset the depletion region charge which is due to the fixed acceptor ions located in the depletion region near the surface. We can calculate the depletion region charge density at surface inversion ($\varphi_S = -\varphi_F$)

$$Q_{BO} = -\sqrt{|-2\varphi_F| 2qN_A\varepsilon_{Si}} \quad (6.3)$$

If the substrate (body) is biased at different voltage level than the source, which is at ground potential (reference) then the depletion region charge density can be expressed as a function of source to substrate voltage V_{SB}.

$$Q_{BO} = -\sqrt{|-2\varphi_F + V_{SB}| 2qN_A\varepsilon_{Si}} \quad (6.4)$$

The component that offsets the depletion region charge is then equal to $\frac{-Q_B}{C_{ox}}$ where C_{ox} is the gate dioxide capacitance per unit area.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (6.5)$$

- Finally, we must consider the influence of a non-ideal physical phenomenon which we have neglected until now. There always exists a fixed positive charge density Qox at the interface between the gate oxide and the silicon substrate,due to impurities and/or lattice imperfections at the interface. The gate voltage component that is necessary to offset this positive charge at the interface is - Qox/ C_{ox}.

- We can combine all of components to find the threshold voltage. For zero substrate bias, the threshold voltage V_{T0} is expressed as follows :

$$V_{TO} = \varphi_{GC} - 2\varphi_F - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (V_{SB} = 0) \quad (6.6)$$

- For non-zero substrate bias, on the other hand, the depletion charge density term must be modified to reflected the influence of V_{SB} upon that charge, resulting in the following generalised threshold voltage expression.

$$V_{TO} = \varphi_{GC} - 2\varphi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (6.7)$$

- The generalised form of threshold voltage can also be written as

$$V_T = \varphi_{GC} - 2\varphi_F - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$V_T = V_{TO} - \frac{Q_B - Q_{BO}}{C_{ox}} \quad (6.8)$$

- In this case, the threshold voltage differs from V_{T0} only by an additive term. This substrate-bias term is a simple function of the material constants and of the source-to-substrate voltage V_{SB}.

$$\frac{Q_B - Q_{BO}}{C_{ox}} = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}}\left(\sqrt{|-2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|}\right) \quad (6.9)$$

Thus the most general expression of threshold voltage V_T can be found as follows:

$$V_T = V_{TO} + \gamma\left(\sqrt{|-2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|}\right) \quad (6.10)$$

Where the parameter

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}} \quad (6.11)$$

is the substrate-bias (or body-effect) coefficient. The threshold voltage expression given in eqn(6.10) can be used both for n-channel and p-channel MOS transistors. One must be careful, however, since some of the terms and coefficients in this equation have different polarities for n-channel and p-channel case. The reason for this polarity difference is that the substrate semiconductor is p-type in an n-channel MOSFET and n-type in an p-channel MOSFET.

Typically, the threshold voltage of an enhancement-type n-channel MOSFET is a positive quantity, whereas the threshold voltage of p-channel MOSFET is negative.

VII. Conclusion

This paper reviewed the choice of materials which could replace silicon dioxide and show the variations of threshold voltage with oxide thickness. In this paper we have explained the effect of threshold voltage variation on reliability of CMOS and threshold voltage reduction on power and leakage current. We also cover techniques for threshold voltage scaling and explain body bias circuit technique as the one. Further research can be carried in finding methods to reduce threshold voltage in CMOS which is desirable.

VIII. References

[1] Author-K. F. Albertin, M. A. Valle, and I. Pereyra., "Study of MOS Capacitors With TiO_2 And SiO_2/TiO_2 Gate Dielectric" , Publication-Journal Integrated Circuits And Systems 2007.

[2] Author-Alice Wang, Anantha P. Chandrakasan, Stephen V. Kosonock "Optimal Supply And Threshold Scaling For Subth]reshold CMOS Circuits", Publication-IEEE.

[3] J. Robertsona, Engineering Department, Cambridge University, Cambridge CB2 1PZ, UK Received: 27 August 2004 / Accepted: 20 September 2004 Published online: 2 December 2004.

[4] Mark Horowitz, Elad Alon, Dinesh Patil, Stanford University Samuel Naffziger, Rajesh Kumar, Intel Kerry Bernst

[5] MOS Capacitor.cheming huch-5

[6] J. Robertson, "High dielectric constant oxides", *The European Physical Journal*, Publisher, UK, 2 Dec 2004

[7] Anil Kumar, Arpita Bharti,A.K. Jaiswal,Anjani Kumar, "Optimization of Threshold Voltage for 65nm PMOS Transistor ein, IBM, 'Scaling, Power, and the Future of CMOS".

[8] Mahmoodi H., Mukhopadhyay S., Roy K. "Estimation of delay variations due to random-dopant fluctuations in nanoscale CMOS circuits". IEEE Journal of Solid-State Circuits 2005; 9:1787-96.

[9] Volkan Kursun "Supply and Threshold Voltage Scaling Technique in CMOS circuits", University of Rochester, New York, 2004.

[10] Author-Ricardo Gonzalez, Benjamin M. Gordon, and Mark A. Horowitz, "Supply and Threshold Voltage Scaling For Low Power CMOS".