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Design of Mergable Flip-Flop for Low Power VLSI Circuits

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Abstract
Lowering power is one of the greatest challenges facing the IC industry today. This paper reduces the clock power by using the multi-bit flip-flop. First we perform coordinate transformation to identify those flip-flops that can be merged and their legal regions. Manhattan distance is used to minimize the total wire length. Combination table is used to find the possible combination of flip-flop. Application of the multi bit flip-flop in an 8-bit adder also included in this paper.
Key Words-Clock power reduction, merging multi bit flip-flop, wire length**,** Manhattan distance, coordinates transformation

I. INTRODUCTION

According to Moore's law the number of transistor doubling every eighteen months so reducing the total power consumption is the major issue in modern VLSI design. We know that the power is directly proportional to area and frequency hence the reduction in power can also reduce the chip area. Reducing the power consumption not only can enhance the battery life, but also can avoid the overheating problem ,which would increase the difficulty of packaging ,cooling [2][3]. In modern VLSI design power consumed by clocking has taken a major part of the whole design [4]. Several methodologies [5] [6] have been proposed to reduce the power consumption of clocking. This paper reduces the clock power by using the multi bit flip-flop. Here several flip-flops can share a common clock to avoid unnecessary power waste. The fig 1 shows the block diagrams of 1 and 2 bit flip-flop. If we replace two 1-bit flip-flop by a 2-bit flip-flop. The total power consumption can be reduced because the two one bit flip-flop can share the same clock buffer after the replacement the location of the flip-flop would be changed. So to find the new location of the flip-flop coordinate transformation is used. To minimize the wire length Manhattan distance is used.

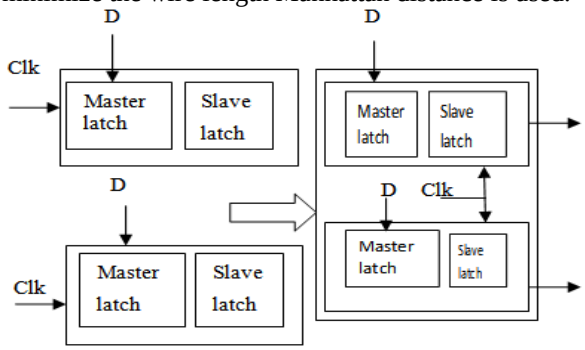

Fig 1. 2 bit flip-flop before and after merging

II. MULTI BIT FLIP-FLOP

When a common clock is shared by the several flip-flops the k-bit flip-flop becomes k-bit multi bit flip-flop. The use of common clock may reduce the power consumption. This paper includes 2, 4, bit multi bit flip-flop as shown in fig.

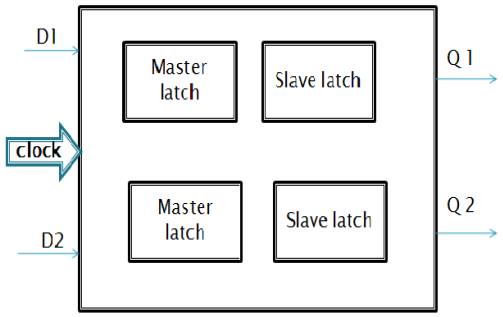

Fig 2. 2bit flip-flop

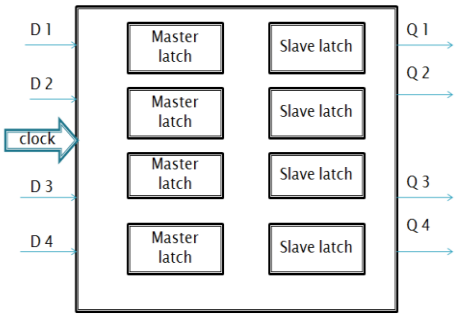

Fig3. 4bit flip-flop

A. *Coordinate transformation*

A coordinate system is a system which uses one or more numbers or coordinates to uniquely determine the position of a point or other geometric element on a manifold such as Euclidean space. It is not easy to identify the location of flip-flop if their

shapes are diamond. If we rotate each segment 45^0, the shapes of all regions would become rectangular which makes the identification of overlapping regions become very simple

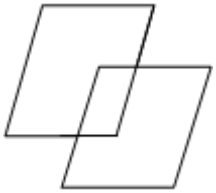

Fig4. (a) Overlapping region before transformation

The overlapping region in diamond shape requires 8 coordinates to find the location of flip-flop. This makes the calculation as complex. The following fig shows the overlapping region in rectangular shape. This is done by means of coordinate transformation. The rectangular shape only requires 4 coordinates to find the location of flip-flop. So the difficulty to calculate the location is overcome here.

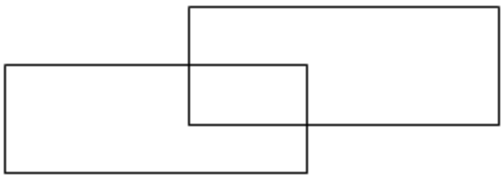

Fig4. (b) Overlapping region after region merging

To denote the coordinates of transformed location we use X'' and Y''

$$X' = \frac{x+y}{\sqrt{2}} \quad (1)$$

$$Y' = \frac{-x+y}{\sqrt{2}} \quad (2)$$

$$X'' = \sqrt{2}.\, X' \quad (3)$$

$$Y'' = \sqrt{2}.\, Y' \quad (4)$$

Then we can find which flip-flops are Mergable according to whether their feasible regions overlap or not. To determine whether two flip-flops overlap or not we use equation 7 and 8

$$DIS\_X\ (f1, f2) < \frac{1}{2} W\ (f1) + W\ (f2) \quad (7)$$

$$DIS\_Y\ (f1, f2) < \frac{1}{2} H\ (f1) + H\ (f2) \quad (8)$$

Where W (f1) and H (f1) [W (f2) and H (f2)] denote the width and height of the flip-flops f1 and f2. DIS_X (f1, f2), DIS_Y (f1, f2) calculate the distance between centers of f1 and f2 in X and Y direction.

B. Manhattan distance

The distance between two points in a grid based on strictly horizontal and vertical path as opposed to the diagonal or "as the crow flies distance" The Manhattan distance is the simple sum of horizontal and vertical component where as the diagonal distance may be computed by applying the Pythagorean Theorem.

C. *Merge of flip-flop*

This design flow can be roughly divided into three stages. In the beginning, we have to identify a legal placement region for each flip-flop fi. First, the feasible placement regions of a flip-flop associated with different pins are found based on the timing constraints defined on the pins. Then the legal placement region of the flip-flop fi can be obtained by the overlapped area of these regions. However, because these regions are in the diamond shape, it is not easy to identify the overlapped area. Therefore, the overlapped area can be identified more easily if we can transform the coordinate system of cells to get rectangular regions.

In the second stage, we would like to build a combination table, which defines all possible combinations of flip-flops in order to get a new multi-bit flip-flop provided by the library. The flip-flops can be merged with the help of the table. After the legal placement regions of flip-flops are found and the combination table is built, we can use them to merge flip-flops. To speed up our program, we will divide a chip into several bins and merge flip-flops in a local bin. However, the flip-flops in different bins may be mergeable. Thus, we have to combine several bins into a larger bin and repeat this step until no flip-flop can be merged anymore.

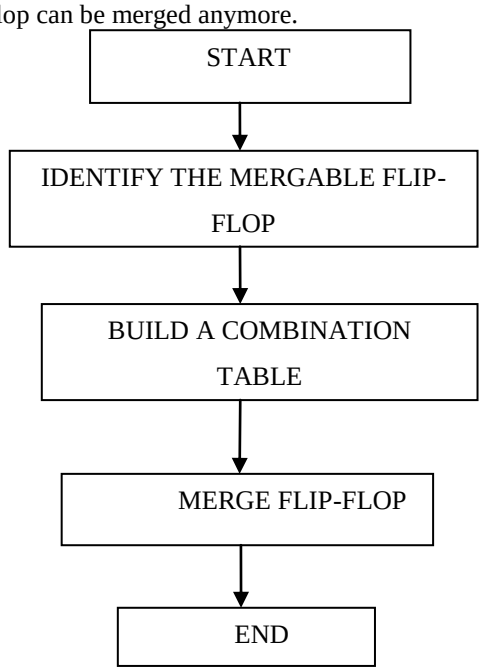

Fig5. Flow chart

D. *Performance Comparison*

The following table shows the power consumption using single and multi bit flip-flop. From the table we come to know that the use of multi bit flip-flop may reduces the overall power consumption. The timing complexity also reduced by means of Manhattan distance. The use of coordinate

transformation can reduces the difficulty of calculating the location of flip-flop.

Flip-flop	Power consumption using single bit flip-flop	Power consumption using multi bit flip-flop
1 bit flip-flop	0.52	0.52
2 bit flip-flop	1.04	0.52
4 bit flip-flop	2.08	0.52
8 bit flip-flop	4.16	0.52

Table 2.1 performance comparison

The following graph shows graphical representation of performance comparison

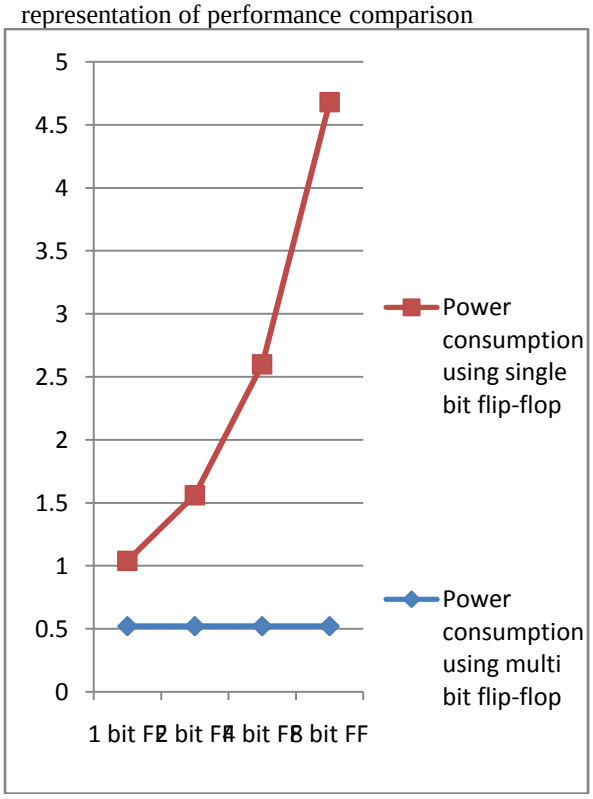

Fig6.graphical representation of performance comparison

III. APPLICATION OF MULTI BIT FLIP-FLOP

This paper presents the application of multi bit flip-flop in an 8 bit adder. Here the 1 bit and 2 bit flops are combined to form a 3bit flip-flop, 1 bit and 4bit flops are combined to form a 5 bit flip-flop. 2 bit and 4 bit flops are combined to form a 3bit flip-flop. 1, 2,4 bit flip-flops are combined to form a 7bit flip-flop. Now by using this 8 bit adder we can able to add up to eight bit without any memory loss.

IV. EXPERIMENTAL RESULT

The following fig shows the stimulated wave form of multi bit flip-flop. Here 1,2,4,8 bit flip-flops are designed and by using this flip-flop 3, 5, 7 bit flip-flop are created by means of merging. The application of 8 bit adder is included and the addition results are stored on specified location. Here the wastage of memory is avoided. The results checked by using Xilinx ISE simulator

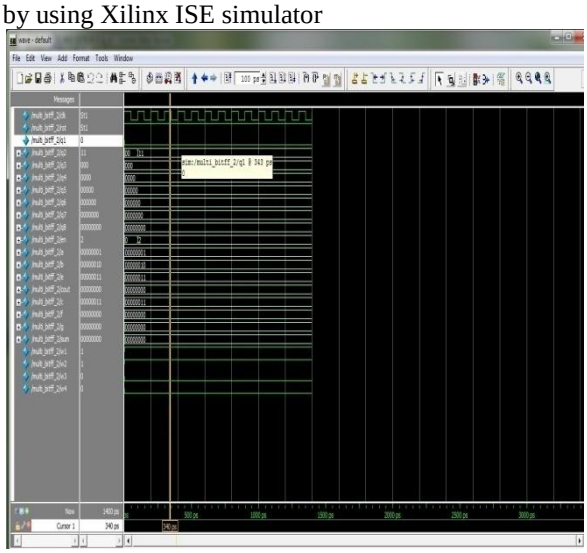

Fig7. Stimulated wave form

V. CONCLUSION

This paper reduces the total power consumption by using multi bit flip-flop. Also include the application of multi bit flip-flop in an 8 bit adder. The total wire length also reduced with the help of Manhattan distance the experimental result shows that the use of multi bit flip-flops can achieve power reduction. Power reduction in turn reduces the chip area the total power consumption of multi bit flip-flop is less when compared to the set of single bit flip-flop.

REFERENCES

[1] shyu Y-T,Lin M-J,Huang C-P,Lin C-W "Effective and Efficient Approach for Power Reduction by Using Multi-Bit Flip-Flops "Vol. 21 no 4 IEEE transactions on VLSI ,April 2013

[2] P. Gronowski, W. J. Bowhill, R. P. Preston, M. K. Gowan, and R. L.Allmon, "High-performance microprocessor design," IEEE J. Solid-State Circuits, vol. 33, no. 5, pp. 676–686, May 1998.

[3] W. Hou, D. Liu, and P.-H. Ho, "Automatic register banking for lowpower clock trees,"

in Proc. Quality Electron. Design, San Jose, CA, Mar. 2009, pp. 647–652.

[4] D. Duarte, V. Narayanan, and M. J. Irwin, "Impact of technology scaling in the clock power," in Proc. IEEE VLSI Comput. Soc. Annu. Symp., Pittsburgh, PA, Apr. 2002, pp. 52–57.

[5] H. Kawagachi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% clock power reduction," in VLSI Circuits Dig. Tech. Papers Symp., Jun. 1997, pp. 97–98.

[6] Y. Cheon, P.-H. Ho, A. B. Kahng, S. Reda, and Q. Wang, "Power-aware placement," in Proc. Design Autom. Conf., Jun. 2005, pp. 795–800.

[7] Y.-T. Chang, C.-C. Hsu, P.-H. Lin, Y.-W. Tsai, and S.-F. Chen, "Post-placement power optimization with multi-bit flip-flops," in Proc.IEEE/ACM Comput.-Aided Design Int. Conf., San Jose, CA, Nov. 2010, pp. 218–223.

[8] Faraday Technology Corporation[Online]. Available:http://www.faraday-tech.com/index.html

[9] C. Bron and J. Kerbosch, "Algorithm 457: Finding all cliques of an undirected graph," ACM Commun., vol. 16, no. 9, pp. 575–577, 1973.

[10] CAD Contest of Taiwan [Online].Available: http://cad_contest.cs. nctu.edu.tw/cad11

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Pursuing M.E (Master of Engineering) in applied electronics from Loyola institute of technology and science. Received her B.E in Electronics and Communication Engineering from Marthandam College of engineering and technology, Anna University. Her areas of interests include low power VLSI design and testing of VLSI circuits.