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High Speed, Low Power, Area Efficient Mux-Add and Bec Based Implementation of Carry Select Adder.

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Abstract
Adder being the basic hardware block of any arithmetic operation, the major constraint in the field of signal processors, data processors to perform any operations are highly dependent on the adder performance of the circuit. The gate level implementation of the carry select adder (CSLA) and modified carry select adder has significantly reduced the area and power consumption which replaced the ripple carry adder (RCA) used in modified CSLA with MUX-ADD block has further reduced the power consumption by efficiently utilizing the area with faster performance.

I. Introduction

Switching speed with low power consumption is the major area needed to be concentrated in modern trends of signal processing, data processing and VLSI applications. To perform any kind of signal and data processing operation, fast arithmetic functions are to be calculated with higher speed but non-degrading functionality. With the advancements in the technology the factors to be taken care during the hardware designs are frequency or speed of operation, power consumption, area utilization, circuit complexity, portability, robustness etc. Thus while designing a modern high performance processing element the optimization or best utilization of the above mention factors are to be considered.

In any modern processing element the digital adder block is a basic block which ensures the high-speed performance to a large extend. The drawback of a simple ripple carry adder (RCA) is associated with its propagation of carry bit which is highly overcome by the implementation of high-speed, area efficient carry select adder (CSLA)[1]. The traditional CSLA independently generates multiple carry and then with the selected carry generates the sum which reduces the carry propagation delay of the RCA. The CSLA has been modified further by reducing the area and power consumption [2] to [4]. The implementation of square-root CSLA (SQRT CSLA) [5] & [6] is modified with the usage of binary to excess-1 converter (BEC) instead of RCA [7] which claims an improved performance.

In this paper the usage of an element ripple carry adder is eliminated and instead a MUX-ADD based arithmetic adder block is used which proves to be logically stronger with a reduced propagation delay in comparison to the other existing logic styles for full-adders such as standard CMOS, complementary pass transistor logic (CPL), double pass transistor logic (DPL), swing restored CPL (SR-CPL) [8]. The brief structure of MUX-ADD block is discussed in section.2 . The BEC block structure is also explained in section.3 . The delay and area is evaluated for the used elemental blocks, modified CSLA & MUX-ADD & BEC based CSLA in section. 4. The proposed designed is elaborated in section. 5. The detailed simulation results in terms of delay, power consumption and area along with the used simulation and synthesis environment is discussed in section. 6 .Finally the work concludes in section.7.

II. MUX –ADD Block

The main idea of this paper is to replace RCA from modified CSLA by a MUX-ADD unit for improved performance. The MUX being a faster hardware than direct adder block mainly improvises the performance in terms of delay, area and power consumption.The truth table of full adder is studied and shown in table.1 with respect to carry input (Cin).

Cin	A	B	Sum		Carry	
0	0	0	**0**	**X**	**0**	**A**
0	0	1	**1**	**O**	**0**	**N**
0	1	0	**1**	**R**	**0**	**D**
0	1	1	**0**		**1**	
1	0	0	**1**	**X**	**0**	**O**
1	0	1	**0**	**N**	**1**	**R**
1	1	0	**0**	**O**	**1**	
1	1	1	**1**	**R**	**1**	

Table.1: Truth table of FA with respect to Cin

The MUX-ADD concept follows the following algorithm:

begin
If Cin=='0'
Then
Sum=A xor B;
Carry=A and B;
Else if Cin=='1'
Then
Sum= A xnor B;
Carry=A or B;

End if;
End;

The above algorithm is implemented by basic gates i.e. AND, OR, INVERTER (AOI) implementation for area and delay calculations. The MUX-ADD (1-bit) implementation is shown in figure.1.

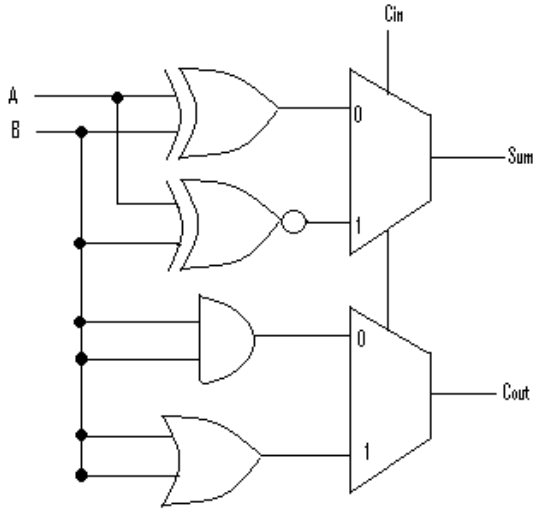

Figure.1: 1-bit MUX-ADD Implementation

III. BEC & BEC based CSLA

Binary to excess-1 converter is used to perform the addition task faster whenever the carry input is '1'. The CSLA for Cin='1' is obtained by the implementation of BEC. For a 4-bit BEC it takes the four bits as input and the output is four bits excess to one as shown in figure.2.

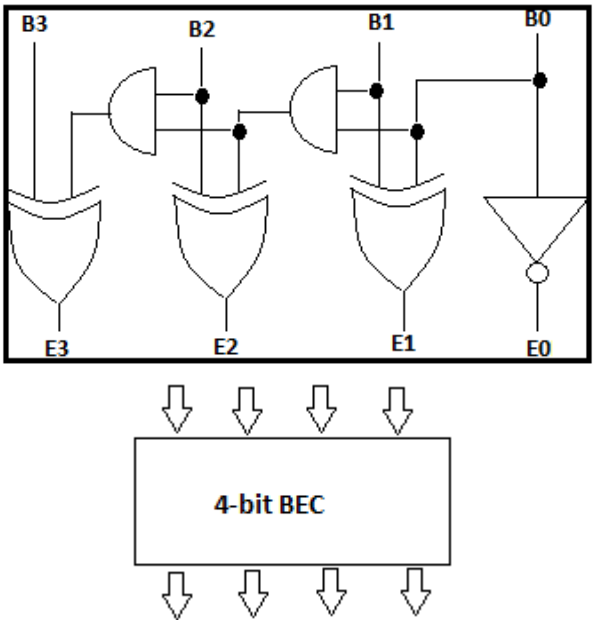

Figure.2 : 4-bit BEC

Both the inputs of BEC and outputs of BEC are fed to four 2:1 MUX and the carry input selects the outputs of the MUXs. The BEC based carry select addition happens by following the algorithm below:

begin
Set MUX I0=SUM with '0'carry;
Set MUX I1= BEC output;
If Cin=='0'
Then
The MUX output is I0;
Else if Cin=='1'
The MUX output is I1;
End if;
End;

IV. Delay & Area evaluation for FA (RCA), MUX-ADD & BEC

The implementation of the basic modules used in the design is AOI i.e. AND, OR & INVERTER. The area is calculated by the presence of total number of basic gates whereas the delay is to be calculated by finding the largest path of the logic block. Each gate 1 unit area having a delay of 1 unit. The delay & area evaluation is shown in table.2. The 1-bit MUX-ADD design implementation is shown in Figure. 1 with the delay area evaluation described in table.3.The 4-bit modified CSLA and 4-bit MUX-ADD & BEC based csla delay & area is also calculated in table.3.

Module	Block	Delay	Area
FA/RCA 1-bit	Half adder	3	6
	Full adder	6	13
4-BEC	XOR	3	5
	2:1 MUX	3	4
MUX-ADD 1-bit	XOR/XNOR	3	5
	AND/OR	1	1
	2:1 MUX	3	4

Table.2: Delay & area evaluation of FA,BEC & MUX-ADD

V. Proposed Design

The proposed design replaces the regular RCA for calculating the higher bit summation by MUX-ADD. This MUX –ADD being faster and low power consumable block improves the overall performance of the circuit. In the proposed design, as shown in figure.3 ,the first bit is calculated using a direct one bit MUX-ADD block to calculate SUM0.The next higher order bits are calculated in two parts i.e. for Cin='0' where it's a simple carry addition using MUX-ADD blocks & the other one for Cin='1' using BEC. Both the output sets from MUX-ADD blocks and BEC is given as the input to 8:4MUX and the final output of sum and carry is taken from the MUX output. Figure .3 depicts the 4-bit implementation of MUX-ADD & BEC based CSLA which can be extended for higher bits

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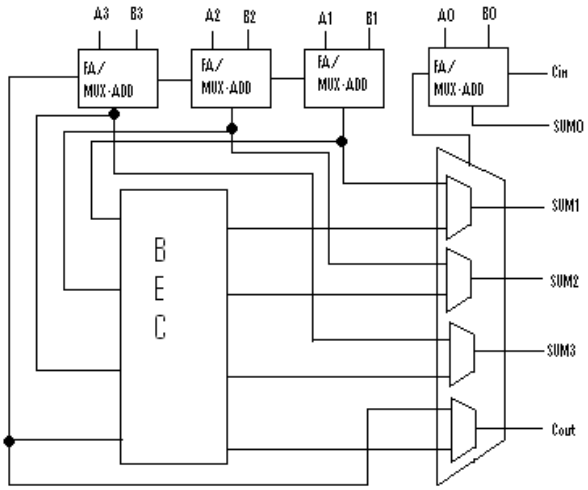

Figure.3: 4-bit RCA/MUX-ADD & BEC based CSLA

VI. Simulation Results

The design proposed in this paper has been developed using Verilog-HDL and synthesized using Cadence RTL. Simulation is done using Cadence Simvision . In order to have a fair comparison the basic measures of gate or transistor levels are kept same for both RCA-BEC based modified CSLA and MUX-ADD & BEC based CSLA.

Table.3 shows the simulation results for the different modules used in this paper regarding delay, power consumption, area, Power -Delay Product (PDP) & Area-Delay Product (ADP). The total power is the sum of leakage power & switching power where as the area indicates the total cell area of the design.

VII. Conclusion

With reference from table.4 the usage of MUX-ADD & BEC based CSLA has 48.3% of improvement in PDP and 33.04 % of improvement in ADP in comparison to modified CSLA(4-bit, can be extended for higher bit size) and delay reduces by 34.63%. Thus with maintaining optimization & proper functionality MUX-ADD & BEC based CSLA claims to be highly efficient. The similar work can be extended for higher order bits i.e. for higher word size and implemented to use in modern processors.

MODULES	DELAY(ns)	AREA(μm^2)	POWER(nW)			Power-Delay product(nW-ns)	Area-Delay product(μm^2-ns)
			Leakage power	Switching power	Total power		
1-bit RCA/FA	2.164	30	16.919	676.008	692.927	1499.49	64.92
1-bit MUX-ADD	1.154	42	20.472	716.274	736.746	850.204	48.468
4-bit BEC	2.145	39	23.192	814.597	837.789	1797.057	83.655
4-bit RCA with BEC	1.588	123	71.783	3077.694	3149.477	5001.369	195.324
4-bit MUX-ADD with BEC (proposed model)	1.038	126	61.417	2428.017	2489.434	2584.032	130.788

Table.3: Delay, area, power, PDP & ADP calculations of different modules.

MODULES	DELAY	AREA	POWER	PDP	ADP
1-bit RCA/FA	46.67% ↓	40% ↑	6.3% ↑	43.3% ↓	25.34% ↓
1-bit MUX-ADD					
4-bit RCA with BEC	34.63% ↓	2.4% ↑	20.95% ↑	48.3% ↓	33.04% ↓
4-bit MUX-ADD with BEC(proposed model)					

Table.4.:Percentage wise comparison of the modules

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