RESEARCH ARTICLE OPEN ACCESS

A Noval method to improve the Logic Test by using Single Cycle Access Structure

[*]Sri Lakshmi. Chandana, [**]B. Vamsi Krishna

[*] M.Tech, Embedded systems, Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru, A.P. India

** Assistant Professor, Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru, A.P. India

Abstract

This paper describes a new single cycle access test structure for logic testing in digital circuits. It avoids the peak power consumption problem of conventional shift based scan chains and reduces the activity during shift and capture cycles of the logic used. This leads to more realistic circuit behaviour during stuck-at and at-speed tests. It provides access to the complete test to run at much higher frequencies which is equal or close to the one in functional mode. The test cycles per net are based on a simple test pattern generator algorithm without using test pattern compression is below 1 for larger designs, and are independent of the design size. The structure allows an additional on-chip debugging signal visibility for each register in the scan chain. This method is backward compatible to full scan designs, existing test pattern generators and simulators can be used with a minor enhancement. It is shown, that how to combine the proposed solution with built-in self-test (BIST) and massive parallel scan chains.

I. Introduction

This paper presents a novel scan cell register for logic tests combined with a novel scan cell routing architecture. The structure allows a single cycle access (SCA) to individual register sets. This access scheme is fundamentally different to SS. It can be compared to a memory with single cycle synchronous write and asynchronous read functionality, whereas the remaining memory content (registers) does not change. The proposed structure is applicable for pattern driven tests and for BIST.

The paper provides reasonable data but is not limited to a frozen solution. It also describes about various trade-offs of different alternatives used in this BIST. The logic testing is a wide field and different users have different preferences on the applied and preferred logic. A reference example based on 992 registers is used.

The proposed FLS gating technique minimizes power in the combinational block. It removes redundant switching activity in the combinational block and also provides leakage minimization through application of the best input vector during scan shifting. The proposed scan partitioning technique reduces average and peak power in the scan chain by minimizing rippling of scan values deterministically.

II. Single Cycle Access Structure For Logic Test

SSR is a compression solution that does not require any information about don't care bits. Yet, it achieves 10 xs to 40x reduction in test data volume, test time, and test channel requirements. With the same minimal hardware used in as SAS, SSR achieves this major cost reduction through modifying

the ATPG process instead of utilizing the don't care bits.

This scheme where the scan enables control information for the launch and capture cycle is already embedded itself in the test data. A new scan register, called the last transition generator (LTG), generates the local fast scan enable signals. The LTG cell has the flexibility to be inserted anywhere in the scan chain and the hardware area overhead is comparable to the pipeline scan enable approach. The proposed method poses no additional constraints for the place and route tool and provides more flexibility to re-order the scan cells to meet the timing closure of the local scan enable signals.

Our goal is to reduce all the VPT parts simultaneously. This is achieved by reducing test data Volume with variable-to-fixed run-1ength coding and reducing scan-in power dissipation as test application time with RAS structure. A heuristic algorithm is proposed to arrange the scan ce11s in RAS to obtain a high compression ratio.

The peak power consumption problem of conventional shift-based scan chains and reduces the activity during shift and capture cycles. This raises to more realistic circuit behaviour during stuck at faults and at-speed logic tests. It enables to complete test run at very higher frequencies equal or close to the one in functional mode. It will be shows, that a lesser number of test cycles can be achieved as compared to other solutions. The test cycle per scan chain based on a simple test pattern generator algorithm without

test pattern compression is below 1 for larger designs and is independent of the scan chain size. The structure provides an additional on-chip debugging signal visibility for each register in scan chain. This method is backward compatible to full scan designs and existing test pattern generators and simulators can be used with a minor enhancement. It shows how to combine the proposed solution with built-in self test (BIST) and massive parallel scan chains.

2.1 SCAh-FF based on an S-FF:

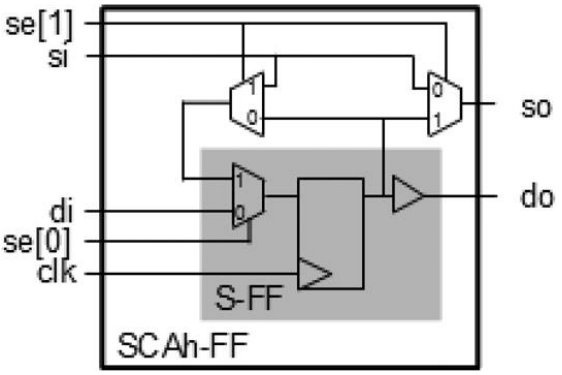


Fig. 1. SCAh-FF based on an S-FF

- The key element of the single cycle access structure with hold mode is the signal cycle access register with hold mode (SCAh-FF).
- It is based on a standard scan register (S-FF) and uses two more 2-to-1 multiplexers. The new SCAh-FF register can be seen in Fig.
-

2.2 SCAH-FF Connectivity:

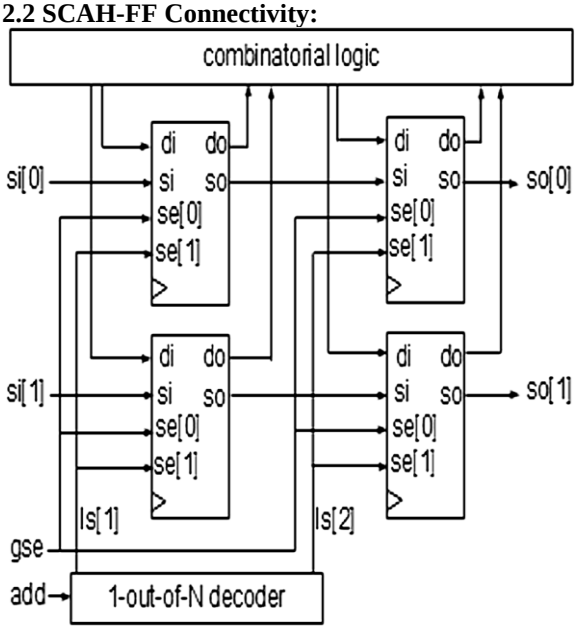


Fig. 2 SCAhS connectivity.

Fig. 2 shows the SCAh-FF and its connectivity. The two major differences are, that the scan-in {si } is now connected to a dedicated scan-out {so } of the preceding register in the scan chain and the register { se[1]} inputs on the same scan depth are connected to the same line-select {ls } signal, which is driven by a "1 to *N* " decoder. Single cycle accesses withhold mode (SCAh-ff) register connected to the line-select signal and it is considered as one line. If {add} is 0, no line is selected. {se[0]} of each SCAh-FF is connected to the global scan enable signal { gse} (comparable to the global scan enable signal of shift-scan structures). The output of the address decoder is connected to the {se[1] } pin of the registers on same line select signal on a particular line. All registers on the same scan depth, enabled by the same line-select signal can be read or written with a single cycle access.

2.3 SCA-Structure without Hold mode:

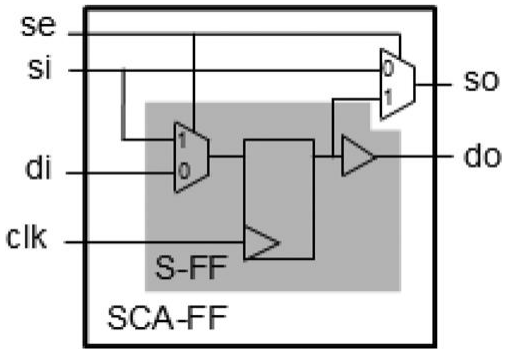


Fig – 3: SCA-Structure without Hold mode

In order to reduce the area overhead of a single cycle access with hold mode, a simpler Single Cycle Access (SCA-FF) is discussed. It adds only one 2x1 Multiplexer to the standard S-FF. It only has one {se} input, which is connected to the individual line-select signal (ls), which is connected to the global enable signal in the Single Cycle Access with hold mode register is removed, therefore the entire global {se} tree is incomplete. The SCA-structure (SCAS) connectivity and page organization equals the one of the SCAhS without the global scan enable {gse}.

2.4 Gated SCA-Structure:

The hold function of the SCAh-FF is missing in the Single cycle access register; it is instead built into the gated clock tree of the gSCAS. Fig shows the connectivity of the gSCA. The scan path reaches from the scan-in AND-selector over the SCA-FF chain (by connecting the scan-out pins of each SCA-FF with the scan-in pins of the succeeding SCA-FF) and is connected with the input of the XOR-tree. The individual line-select signals {ls} are connected with the {se} input of the SCA-FF in the same line. All Single Cycle Access registers on a line are clocked by a gated clock element (gcl). The gcl is driven by the clock and the line-select signal. The gcl can be enhanced, if a clock enable signal {ce} generated by combinatorial logic exists. The gscan enable signal is connected with each {gcl}, which is already the case in SS if gated clock elements are used to propagate the clock during shift.

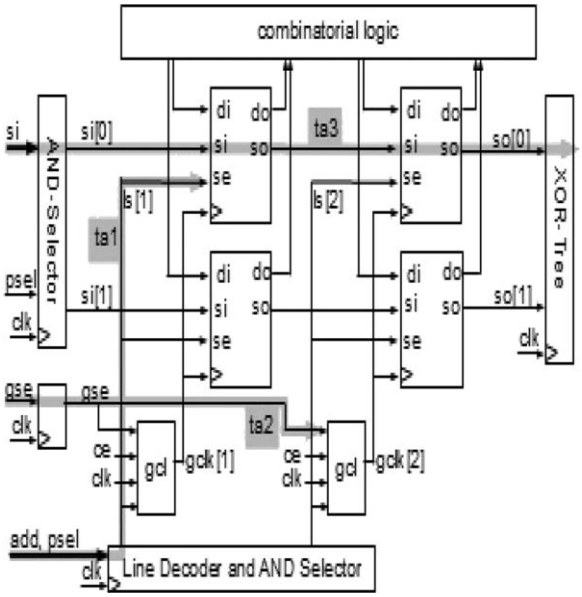


Fig – 4: Gated SCA-Structure

2.5 SCAH-FF Page:

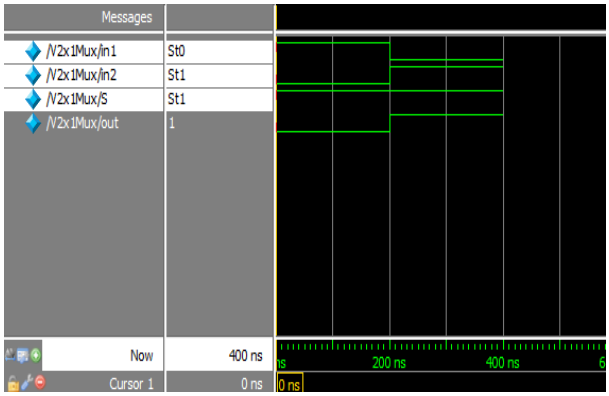
The SCAhS enables single cycle read/write accesses to the each register line. The test structure is organized as pages, to achieve a read/write access at design speed or at a reasonable test speed.

The page depth equals the scan chain depth (SD = number of SCAh-FF connected to one chain on one page). Assuming it is 31. Multiplied with the scan width (SW = number of scan chains on one page, for example 32), then number of SCAh-FF is SD*SW=992 per page.

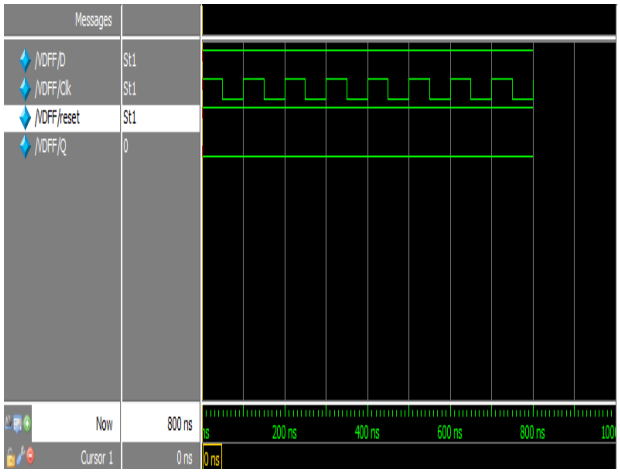
III. Implementation of the modules:

All the sub modules were implemented and simulated with Xilinx 13.2 version based on Spartan 3 Basic kit hardware specifications. Initially all modules implemented separately and then synthesized in our proposed design implementation as given below.

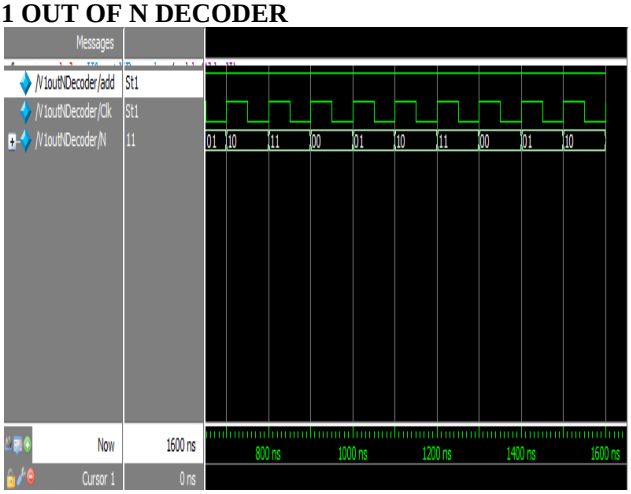
Various implementations with and without hold mode as well as gated and partial implementation methods are presented. The aspects feasibility, peak power consumption, switching activity during test, area, test cycles, at-speed testing and debugging features are compared. The best solution (gSCAS) is compared to RAS implementations and is superior to all known RAS solutions



D FLIP FLOP

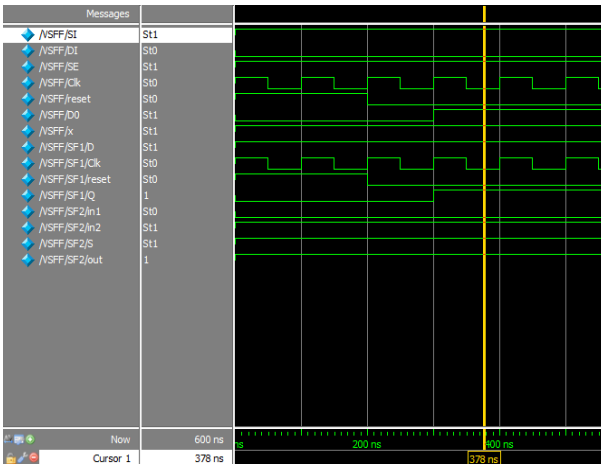


1 OUT OF N DECODER

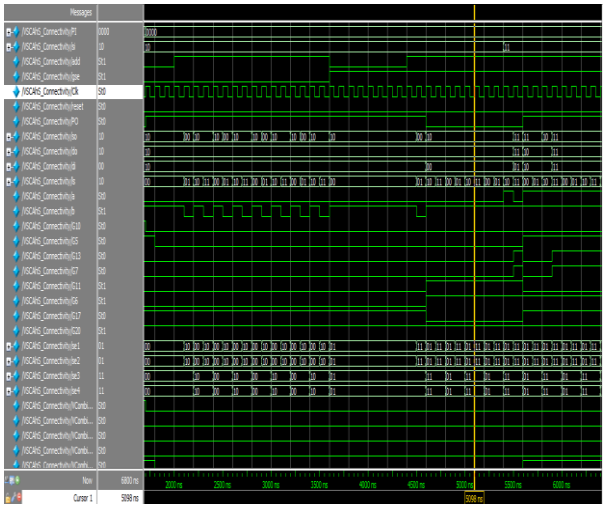


2*1 MUX:

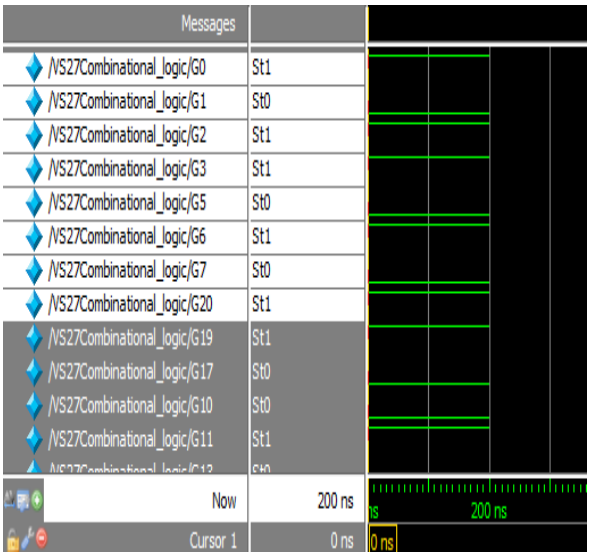
SCAN FLIPFLOP



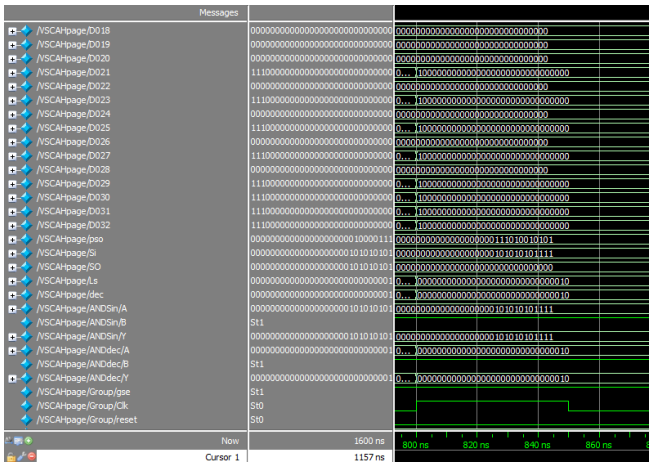
SCAHS CONNECTIVITY

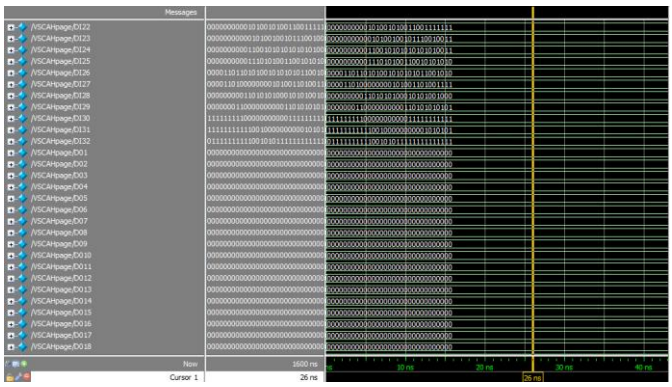


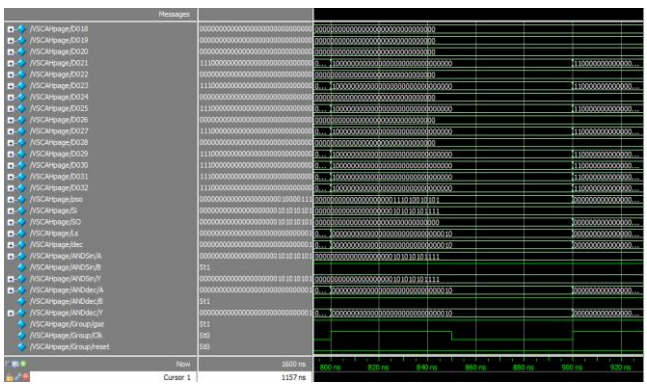
BENCHMARK :



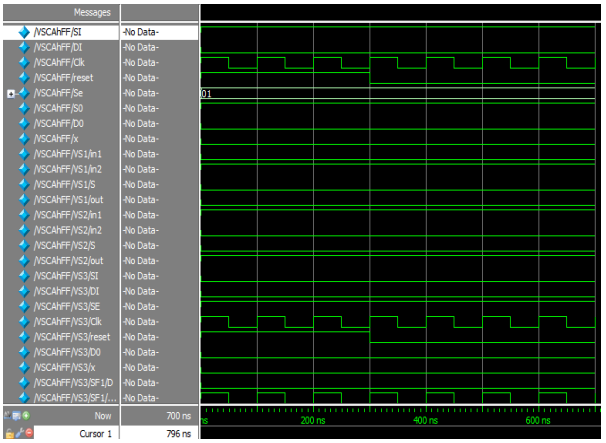
SCAH-FF PAGE



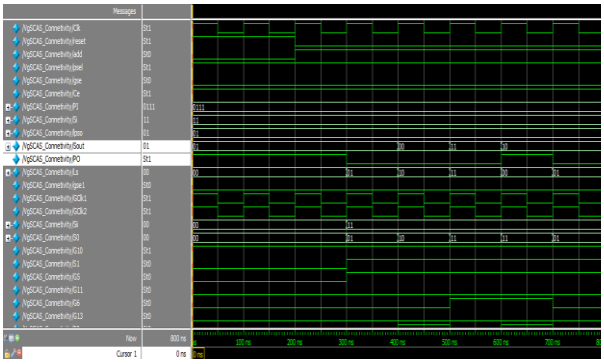




SCAH FLIPFLOP



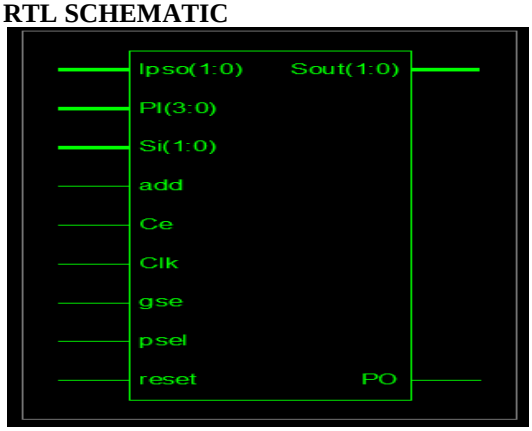
TOP MODULE:



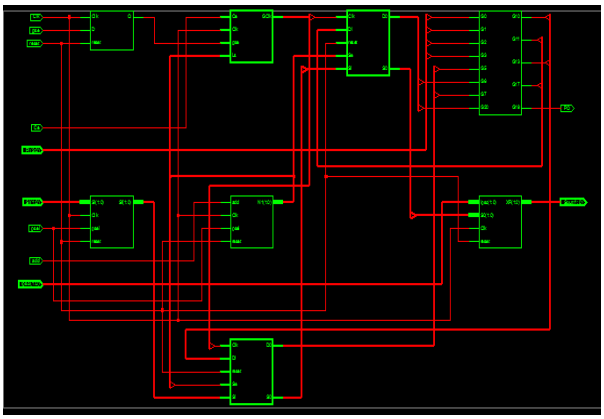
DEVICE UTILIZATION SUMMARY

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s**
Number of Slice Flip Flops	8	7,168	1%	
Number of 4 input LUTs	27	7,168	1%	
Logic Distribution				
Number of occupied Slices	16	3,584	1%	
Number of Slices containing only related logic	16	16	100%	
Number of Slices containing unrelated logic	0	16	0%	
Total Number of 4 input LUTs	28	7,168	1%	
Number used as logic	27			
Number used as a route-thru	1			
Number of bonded IOBs	17	141	12%	
IOB Flip Flops	2			
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	257			
Additional JTAG gate count for IOBs	816			

RTL SCHEMATIC



TECHNOLOGY SCHEMATIC



IV. CONCLUSION

A single cycle access structure is explained. Various blocks implementations with and without hold mode as well as gated and partial implementation methods are presented. The aspects feasibility, peak power consumption, switching activity during test, area, test cycles, at-speed testing and debugging are compared. A guide is given how to choose the best implementation. The best solution (gSCAS) is compared to RAS implementations and is superior to all known RAS solutions. If BIST is preferable due to limited chip IOs or partial scan implementation, an address controlled BIST is discussed. The ATPG algorithms can be enhanced with the same methods SS implementations are optimized. Future work is related to algorithms for reducing the test cycles per net itself, register reordering, and pattern optimization for activity reduction and de-compression methods for BIST using the gSCAS.

References

[1] M. Kassab, and N. Mukherjee, "Embedded testing," IEEE Computer Aided Design, May 2004, pp.776–792.

[2] M. L. Bushnell and V. D. Agarwal, Essentials of Electronic Testing of Memory, and Mixed Signal VLSI Circuits, Kulwer Academic Publishers, 2000.

[3] N. Ahmed, M. Tehran poor, and V. Jay ram. Supply Voltage Noise Aware ATPG for Transition Delay Faults. In Proceedings IEEE VLSI Test Symposium (VTS), pages 179–186, 2007.

[4] S. Almukhaizim and O. Sinanoglu. Power optimization Through Dynamic Partitioning of Scan Chains. In Proceedings IEEE International Test Conference, paper 9[2], 2008.

[5] B. Koenemann and T. Onodera. Extending OPMISR Beyond 10x Scan Testing Efficiency. IEEE Design & Test of Computers,19(5):65–73, 2002.

[6] A. Chandra and K. Chakrabarty. Reduction of SOC on Test Data Volume, Scan Power and Test Time Using Alternative Run-Length Codes. ACM/IEEE Design Automation Conference (DAC), pages 673–678, 2002.

[7] S. Ravi. Power-Aware Test: Challenges and Solutions. IEEE International Test Conference, Lecture 2[2], 2007.

[8] I. Pomeranz, and J. Raj ski. A Scalable Method to optimize Capture Power that Based on Scan Designs. IEEE International Test Conference, paper 32[2], 2006.

[9] P. M. Rosinger, B. M. Al-Hashimi, and N. Nicolici. Low Power Mixed Mode BIST Based on Mask Pattern Generation Using

Dual LFSR Reseeding. International Conference on Computer Design, Sept 2002.

[10] J. Saxena, K. M. Butler, V. B. Jay ram, and S. Kundu. A Case Study of IR-Drop in Structured At-Speed Testing. IEEE International Test Conference, pages 1098–1104, Oct. 2003.

[11] N. A. Touba. Survey of Test Vector Compression methods. IEEE Design & Test of Computers, 294–303, April 2006.

[12] J. Wang, D. M. H. Walker, A. Majhi, B. Kruseman, G. Gronthoud, L. E. Villagra, Wiel, and S. Eichenberger. Power Supply Noise in Delay Testing. In Proceedings IEEE International Test Conference, page 17.3, 2006.

[13] K. K. Saluja, and K. Kinoshita. Low Capture Power Test Generation for Scan-Based At-Speed Testing. In Proceedings IEEE International Test Conference, pages 1019–1028, November 2005.

[14] D. J. Campbell, J. Berech, "Scan-Based on Transition Fault Testing – Implementation and Low Cost Test Challenges," International Test Conference, pp. 1120 - 1129, Oct. 2002.

[15] S. Wang "A BIST TPG for low power dissipation and high fault coverage" IEEE Transaction on Very Large Scale Integrated (VLSI) System, vol. 15, pp. 777–789, Jul 2007.

[17] S. Almukhaizim and O. Sinanoglu "Dynamic scan chain partitioning for optimizing peak shift power during test" IEEE Transaction on Computer Aided Design Integrated Circuits System, vol. 28,pp. 298–302, Feb 2009.

[18] M. Grinch, and A. Gunda "Scan test cost and power reduction through systematic scan reconfiguration" IEEE Transaction on Computer Aided Design Integrated Circuits System, vol. 26, pp. 907–917, May 2007.