RESEARCH ARTICLE OPEN ACCESS

UPQC for Power Quality Improvement of Induction Motor Drive with Reduced DC Link Voltage

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Abstract
The main aim of this project is ,this topology enables UPQC to have a reduced dc-link voltage without compromising its compensation capability. Three-phase, four-wire unified Power Quality (UPQC) to improve power quality. The UPQC is realized by the integration of series and shunt active power filters (APF) sharing a common dc bus capacitor. The realization of shunt APF is carried out using a three-phase, four-leg Voltage Source Inverter (VSI), The performance of the applied control algorithm is evaluated in terms of power-factor correction, source neutral current mitigation, load balancing, and mitigation of voltage and current harmonics in a three-phase, four-wire distribution system for different combinations of linear and non-linear loads. This circuit consists of capacitor in series with the interfacing inductor of the shunt active filter. The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously compensating the reactive power required by the load, so as to maintain unity power factor, without compromising its performance. This allows us to match the dc-link voltage requirements of the series and shunt active filters with a common dc-link capacitor. AC induction motor has a fixed in the output side to run the ac machine with required speed. The proposed topology enables UPQC to compensate voltage sags, voltage swells and current harmonics with a reduced DC-link voltage without compromising its compensation capability by implementing the circuit in MATLAB/SIMULINK software.
Index Terms: Power quality, UPQC, Load balancing, voltage sags, voltage swells, AC Induction motor, APF

I. INTRODUCTION

This proposed topology also helps to match the dc-link voltage requirement of the shunt and series active filters of the UPQC. The topology uses a capacitor in series with the interfacing inductor of the shunt active filter, and the system neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter. The average switching frequency of the switches in the VSI also reduces; consequently the switching losses in the inverters reduce. The main aim of this project this topology enables UPQC to have a reduced dc-link voltage without compromising its compensation capability. The three phase three wires UPQC system is used for compensation of power quality issues. In this method the UPQC which requires more rating of series and shunt active filters. Additionally to maintain the Low harmonics level by adding passive filters.

The different topologies reported in literature of three-phase four-wire UPQC use active compensation for the mitigation of source neutral current along with other PQ problems. For the mitigation of source neutral current, the uses of passive elements are advantageous over the active compensation due to ruggedness and less complexity. There are many techniques proposed for the compensation of neutral current using star-delta transformer in a three-phase four-wire distribution system and some of these have been patented. The application of star-delta transformer along with an APF is also used for harmonic current reduction in the neutral conductor. A filter employing three single-phase transformers with a capacitor has been used for removing harmonic current from the neutral conductor and has been patented. Another scheme by providing a six-phase system, with the help of two transformers connected in anti-phase has been reported for canceling third harmonic current in neutral conductor. The star-delta transformer along with a diode rectifier and a half-bridge PWM inverter is also reported for the compensation of neutral current. For the mitigation of source neutral current along with other current based distortions, the integration of readily available three-leg VSI with star-delta transformer has been reported in literature for 3P-4W DSTATCOM [6]. Unfortunately, for the mitigation of neutral current the performance of the star-delta transformers is affected to an extent under distorted or unbalanced source voltages, which is very common in practice. The UPQC is one of the key CPDs, which takes care of both voltage and current based distortions simultaneously. Hence, for neutral current mitigation the integration of star-delta transformer with UPQC is

more justified. In this paper, a simple star-delta configuration is utilized for the mitigation of source neutral current, while other options such as zig-zag transformer or T-connected transformer require specially designed transformers.

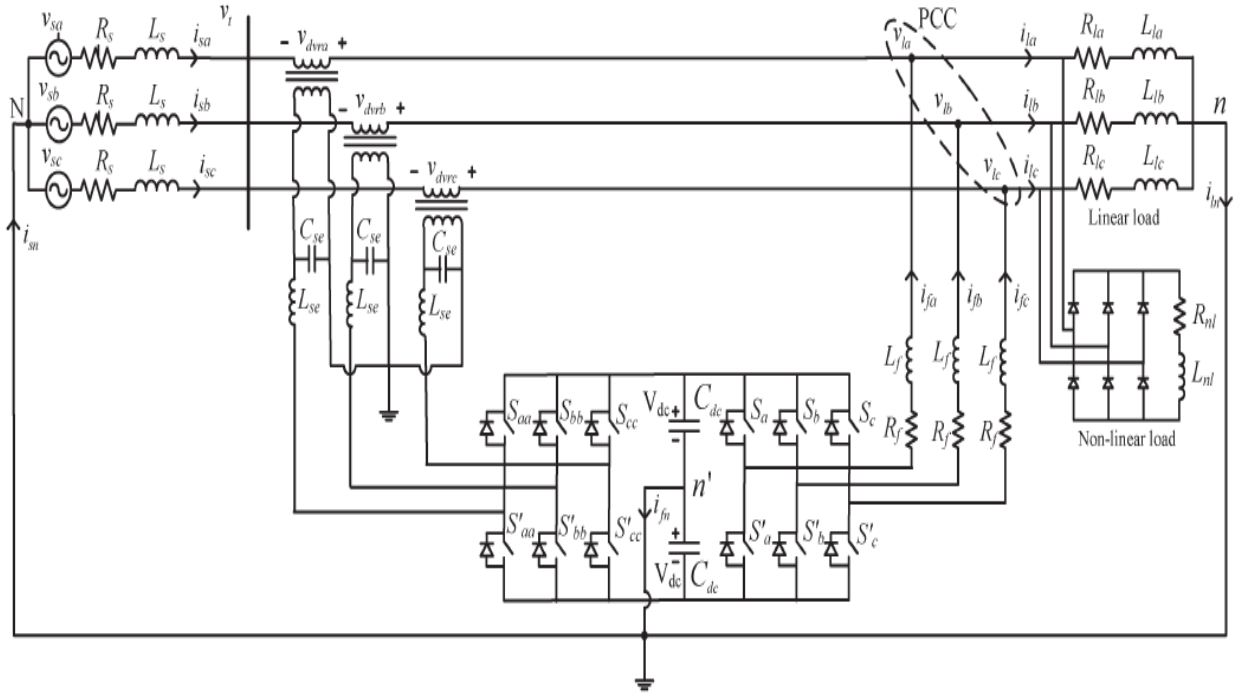


Fig.1. Equivalent circuit of neutral-clamped VSI topology-based UPQC

The conventional and proposed topology of the UPQC are discussed in detail. Fig. 1 shows the power circuit of the neutral-clamped VSI topology-based UPQC which is considered as the conventional topology in this study. Even though this topology requires two dc storage devices, each leg of the VSI can be controlled independently, and tracking is smooth with less number of switches when compared to other VSI topologies. In this figure, *vsa*, *vsb*, and *vsc* are source voltages of phases *a*, *b*, and *c*, respectively. Similarly, *vta*, *vtb*, and *vtc* are terminal voltages. The voltages *v*dvr*a*, *v*dvr*b*, and *v*dvr*c* are injected by the series active filter. The threephase source currents are represented by *isa*, *isb*, and *isc*, load currents are represented by *ila*, *ilb*, and *ilc*. The shunt active filter currents are denoted by *ifa*, *ifb*, *ifc*, and *iln* represents the current in the neutral leg. *Ls* and *Rs* represent the feeder inductance and resistance, respectively. The interfacing inductance and resistance of the shunt active filter are represented by *Lf* and *Rf* , respectively, and the interfacing inductance and filter capacitor of the series active filter are represented by *L*se and *C*se, respectively. The load constituted of both linear and nonlinear loads as shown in this figure. The dc-link capacitors and voltages across them are represented by *C*dc1 = *C*dc2 = *C*dc and *V*dc1 = *V*dc2 = *V*dc, respectively, and the total dc-link voltage is represented by *Vd*bus(*V*dc1 + *V*dc2 = 2*V*dc).

The system under consideration for three-phase, four wire distribution system is shown in Fig. 2.The UPQC is connected before the load to make the source and the load voltage free from any distortions. At the same time, the reactive current drawn from the source should be such that the currents at source side would be in phase with utility voltages. Provision is made to realize voltage harmonics in the source voltage by switching on/off the three-phase diode bridge rectifier. The UPQC, carried out by using two VSIs, is shown in Fig.3: one VSI acts as the shunt APF and the other as the series APF. The shunt APF is realized using a three-phase, four-leg VSI, and the series APF is carried out using a three-phase, three-leg VSI. Both APFs share a common dc link between them. The four-leg, VSI based shunt active filter is capable of suppressing the harmonics in the source currents, negative sequence of the source current, load balancing, and power-factor correction. The implemented control algorithm consists mainly of the computation of the three-phase reference voltages of load $(v^*_{la}, v^*_{lb}, \text{and } v^*_{lc})$ and the reference currents for the source current $(i^*_{sa}, i^*_{sb}, \text{and } i^*_{sc})$

II. SYSTEM CONFIGURATION

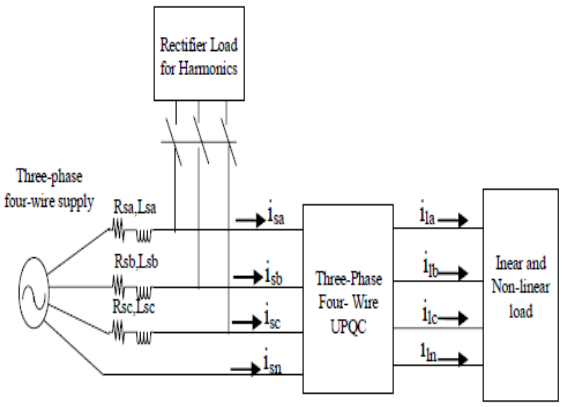


Fig.2 Three-phase, four wire distribution system

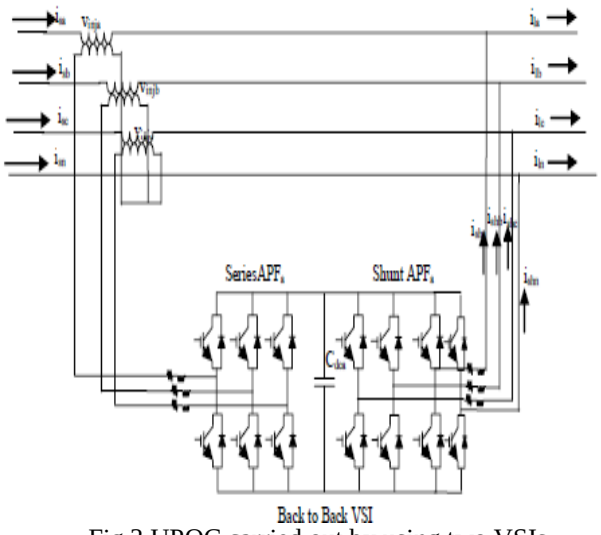


Fig.3 UPQC carried out by using two VSIs

The voltage at the source side before UPQC, load voltage at the load, voltage injected by the series APF, and dc link voltage between two inverters are represented by v_s, v_L, v_{inj}, and V_{dc}, respectively. The current on the source side, current drawn by the loads, neutral current on the source side, load neutral current, and current injected by the shunt APF are represented by i_s, i_l, i_{sn}, i_{ln}, and i_{sh}, respectively.

III. THREE PHASE FOUR WIRE UPQC

Fig. 4 shows a 3P-4W UPQC topology, which is feeding a combination of linear and non-linear unbalanced load. The series and shunt APFs are realized using two readily available three-leg VSIs. The dc links of both APFs are connected to a common dc link capacitor. The series APF is connected between the supply and load terminals using three single phase transformers with turn's ratio of 5:1. The primary winding of these transformer are star connected and the secondary windings are connected in series with the three-phase supply. In addition to provide the required injecting voltages, these transformers are used to filter the switching ripple content in the series APF. A small capacity rated R-C filter is connected in parallel with the secondary of each series transformer to eliminate the high switching ripple content in the series APF injected voltage. The voltage source inverters for both the APFs are implemented with Insulated gate Bipolar Transistors (IGBTs). In Fig.4 (isa, isb , isc), (ila, ilb , ilc) and (ifa, ifb , ifc,) represent the source currents, load currents and shunt APF currents in phase a, b and c respectively.

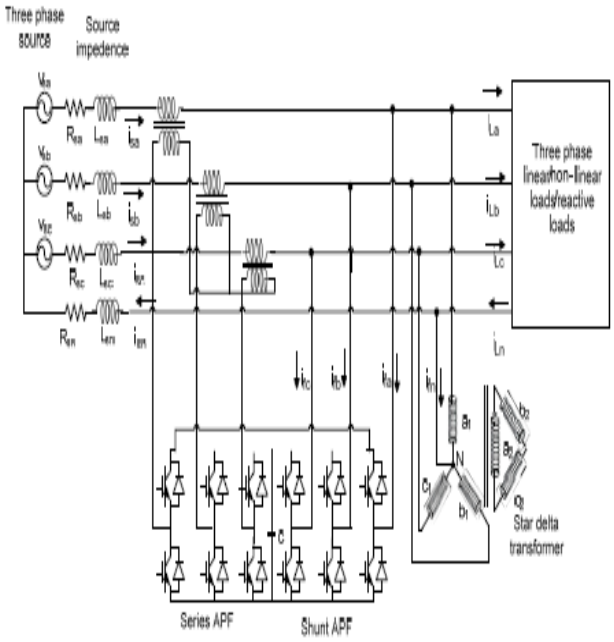


Fig.4. Detailed configuration of proposed 3P-4W UPQC

The source neutral current, load neutral current and neutral current of the additional connected transformers are represented by isn, iln and iTn, respectively. The injected voltages by the series APF in phase a, b and c is represented by vinja, vinjb and vinjc, respectively. In this topology, a star-delta transformer is connected in shunt near the load for the mitigation of the source neutral current. The delta connected secondary provides a circulating path to the zero sequence current (io) in case of unbalanced load and hence the supply neutral current is reduced to zero. The load under consideration is a combination of linear and non-linear load. Two single-phase R-L loads are taken as unbalanced linear load, where as a induction motor is taken as non-linear load.

ADVANTAGES

- The reactive power is injected along with the sinusoidal current,
- The voltage and current regulation is done effectively,
- The PF is maintained even if the load is varied.

APPLICATIONS

- Distribution Generation
- Grid Control Systems
- Transmission Lines

Series Active Filter

Dynamic Voltage Restorer is one of custom power device specially used to maintain the load voltage constant in the distribution system. DVR has two operating modes. In normal operation mode it is in standby mode in which voltage injection by DVR is zero. Most of the time DVR will be in standby mode and hence reduces the losses.

As soon as control circuit detects the any voltage disturbance, reference voltage is generated for required magnitude, duration and phase and is injected through injection transformer. This mode of DVR is known as injecting mode. This injection should satisfy the equation

$$V_L=V_S+V_{INJ}$$

Where V_S is the source voltage, V_{INJ} is the injected voltage by DVR and V_L is the load voltage.

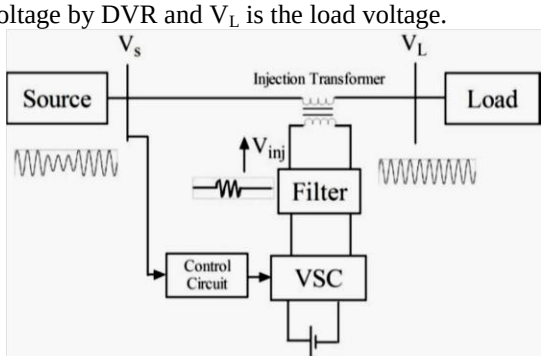


Fig 5 : Structure of DVR

Fig 5 shows the basic configuration and operation of DVR which consist of an injection transformer, Voltage Source Converter (VSC), harmonic filter, storage device and control system

Shunt Active Filter

Nonlinear loads require harmonics current I_{LH} from the main supply beside fundamental current I_{LF}. This causes the main supply to operate at frequencies above the nominal 50Hz or 60Hz and in doing so, also creates a negative phase-sequence component which is undesirable.

The shunt active filter is considered a current source because it injects non-sinusoidal current I_{LH} through the parallel branch of the network in order to compensate for the current harmonic demand of the nonlinear load. The role of the active filter controller is to sense and monitor the load current and to appropriately determine the correct reference harmonic current for the inverter. Once the correct reference harmonic content is determined; this reference current is fed through a suitable current controller which then is sent to the inverter for injection into the network. Fig 6 .shows the basic concept and principle of shunt active filter

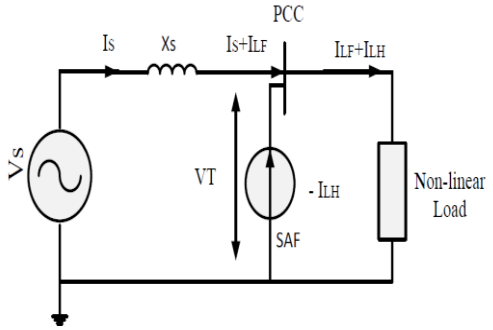


Fig6: Principle of shunt active filter

IV. MATLAB MODELING AND SIMULATION RESULTS

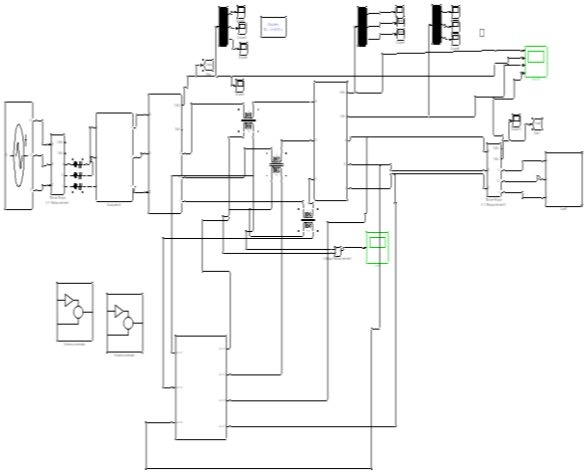


Fig 7.Outer View of the system with Proposed UPQC

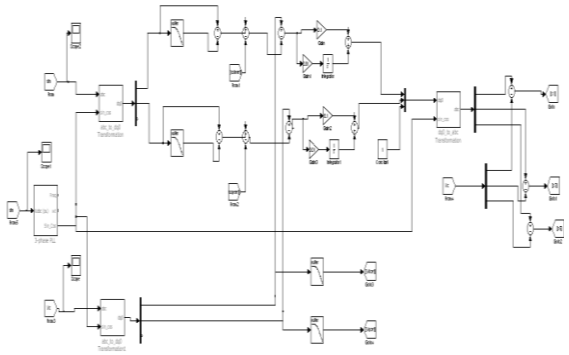


Fig 8.Series Compensator

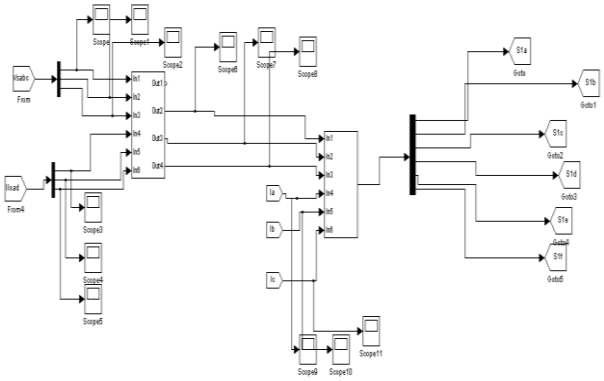


Fig 9.Shunt Compensator

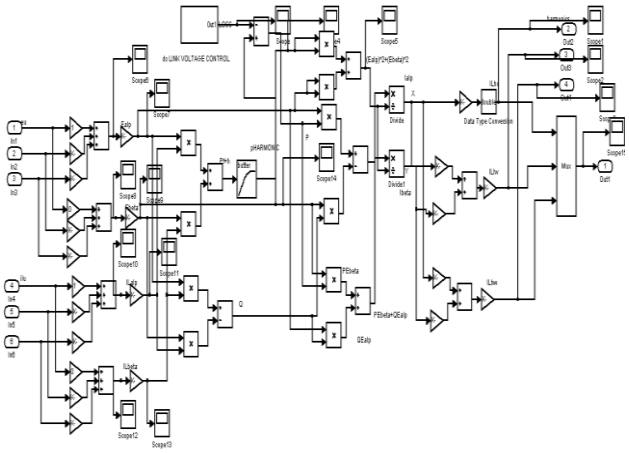


Fig 10.Shunt Reference Generator

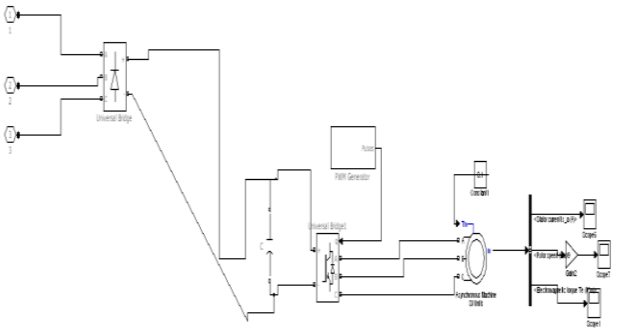


Fig 11.Induction Motor Load

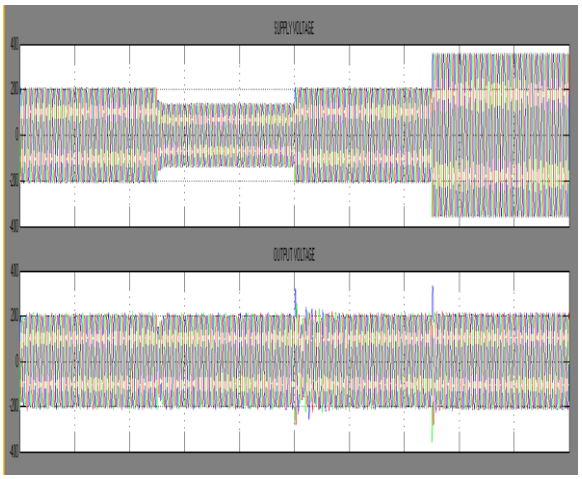


Fig.12. Voltages Before And After Compensation

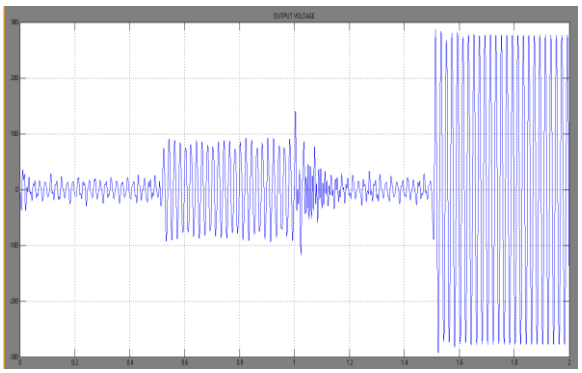


Fig.13.Injected Voltages

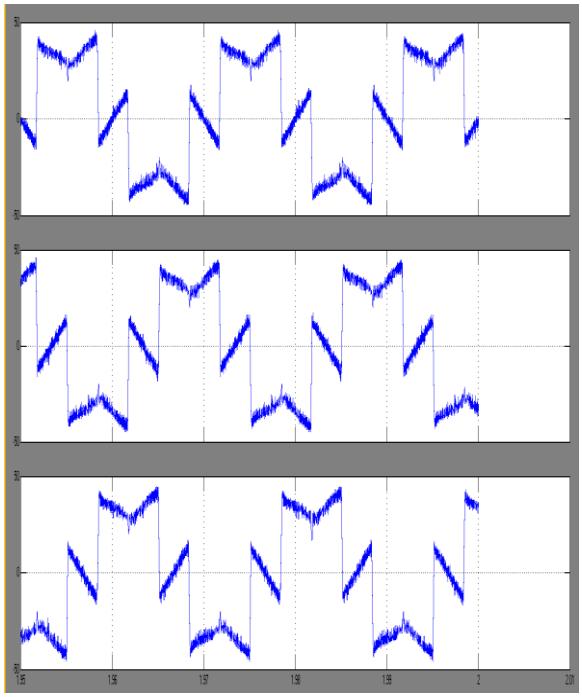


Fig 14.Shunt Filter Currents

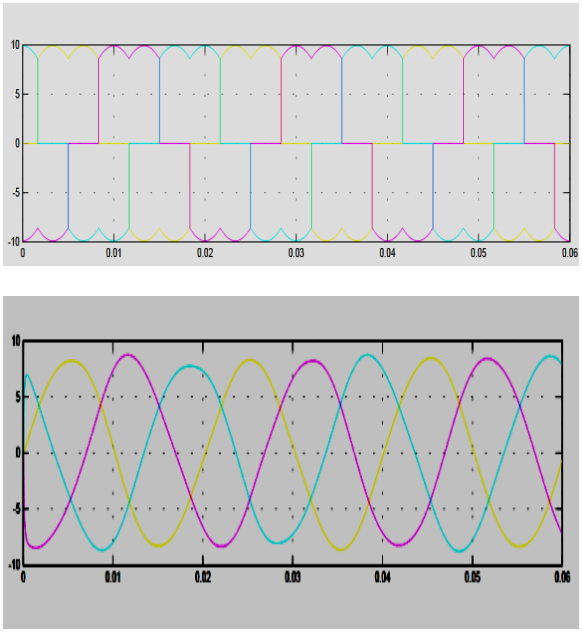
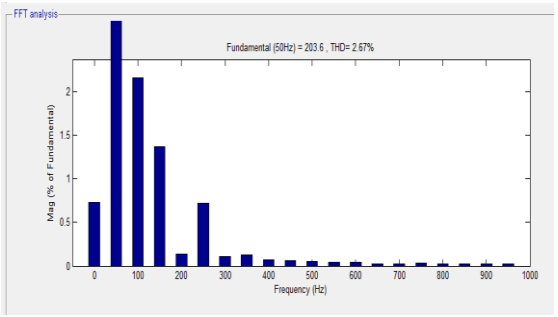


Fig 15.Currents Before And After Compensation



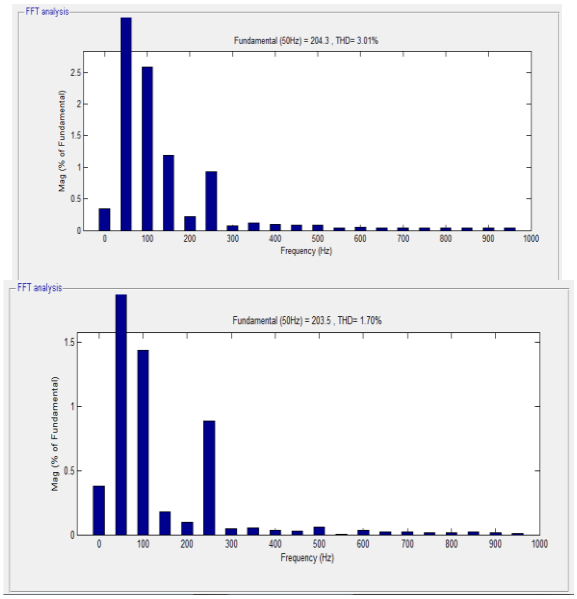


Fig 16.THD of Load Voltages After Compensation

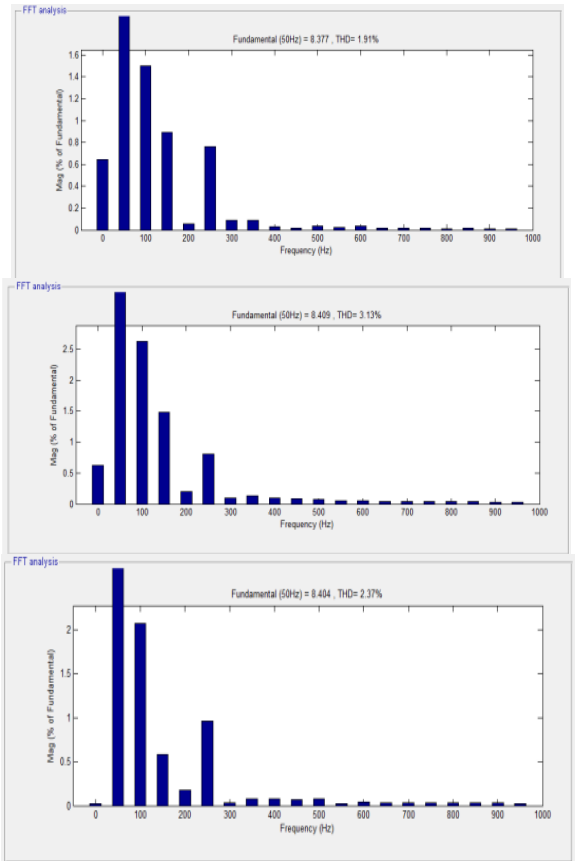


Fig 17.THD of Source Currents After Compensation

V. CONCLUSION

UPQC topology has been proposed in this paper which has the capability to compensate voltage sags, voltage swells and current harmonics at the load at a lower DC-link voltage by using different control strategies for series and shunt APF's. The proposed method is validated through MATLAB simulation. The topology gives the advantages of both the neutral clamped topology and the four leg topology. THD's are less than 5% in the source currents and load voltages.

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