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Design and Implementation of 2mbps Data and Voice Frame Structure

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Abstract
Most digital data are not stored in the most compact form. Rather, they are stored in whatever way makes them easiest to use, such as: ASCII text from word processors, binary code that can be executed on a computer, individual samples from a data acquisition system. The soft core allows the manipulation of E1(2Mbps) 2048KHz 32-channel carrier information. It inserts/removes data into/from E1 frame and multiframe structures. The main use of the developed soft core in the implementation of data communication equipment is to allow multiple users to share a common 2Mbps carrier with a flexible scheme for bandwidth allocation. The hardware module that increases performance of the data communications.
KEYWORDS –2Mbps carrier frame, Drop_insert

I. INTRODUCTION

Data compression is the general term for the various algorithms and programs developed to address this problem. A *compression program* is used to convert data from an easy-to-use format to one optimized for compactness. Likewise, an *uncompression program* returns the information to its original form.

A series of digital multiplexes graded according to capability so that multiplexing at one level combines a defined number of digital signals, each having the digit rate prescribed for the next lower order, into a digital signal having a prescribed digit rate which is then available for further combination with other digital signals of the same rate in a digital multiplex of the next higher order.

The design implements the 2Mbps carrier frame for adding and dropping for the scope of individual enterprise users research & development. The IP core is a complex, pre-designed and pre-verified hardware module that can be used in the composition of large circuits, typically custom VLSI integrated circuits or large programmable devices, such as multimillion-gate FPGAs. The developed software code in the form of hardware description language file will support some applications & may not support some functions due to synchronization at the final implementation.

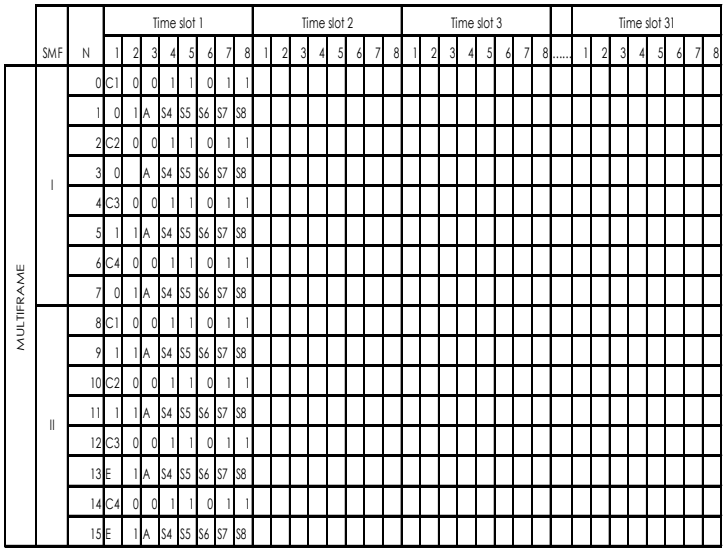
The developed design used for a telecom applications in the form of E1 carrier transmission protocol. The design operates dropping and adding information from/to an E1 carrier frame, or simply E1 frame. This hardware design respects the ITU-T Standards G.703.

G.704 AND G.706 [1][2][3].The developed module posed challenges in the synchronization of data and control information. A dedicated IC to mount an E1 frame and perform multiframe alignment detection, Cyclic Redundancy Check (CRC) computation and time slot detection. To execute the add-drop function the usual solution is to add a micro-controller. The hardware module used to cascade several add-drop modules in a single equipment. The next section describes the 2Mbps frame structure . section 3 gives the hardware implementation of the design for 2Mbps frame structure. Section 4 gives the output waveforms of each module. Section 5 presents a set of conclusions.

II. Design and implementation of E1 Carrier Frame Structure

2.1 E1 multi Frame Structure

E1 is the lowest level of the Plesiochronous Digital Hierarchy (PDH). It is among the most common ways of transmitting voice and data over telephone and data networks. The signal transported in an E1 carrier allows the transmission of up to 31 voice or data channels plus 1channel dedicated to carry low level control information



C1, C2,C3,C4 : SMF CRC code ,computed during transmission and inserted in the SMF that follows it
E: CRC – 4 error ,indicates if the computed CRC is equal or not to the received CRC in each SMF
A: remote alarm indication , bit 3 of all odd frames indicates the event of a remote alarm
S4, S5,S6,S7,S8 : service channel or synchronization status messages

Fig 1 Basic E1 MF Structure ,highlighting the control information structure in time slot 0

Each channel in a frame has 8 bits and is called a *time slot*. Thus, a frame contains a total of 256 bits. Time slots in a frame are numbered from 0 to 31. Each time slot corresponds to a 64Kbps channel carrying 8 bits of either data or an 8KHz digitized voice sample. Bits in a time slot are numbered from 1 to 8. Time slots are combined using Timing Division Multiplexing (TDM) at 2,048MHz. Thus, a frame is transmitted each 125μs . Multiple frames are grouped to transport alignment, error detection and service information. Eight consecutive frames constitute an E1 *submultiframe* (SMF) structure. Two consecutive E1 submultiframes form an E1 *multiframe* (MF). E1 carrier equipment transmits and/or receives an MF each 2ms. Frames in an MF are numbered from 0 to 15. The basic E1 frame and multiframe structure is depicted in Figure1.

The first time slot of each frame, named time slot 0 contains MF basic control information. Two kinds of alignment are employed, frame and MF alignment. Frame alignment provides frame synchronism information, where every even frame contains a "0011011" pattern from bit 2 to bit 8, and all odd frames have a '1' in bit 2. MF alignment provides MF synchronism, where every odd frame from 1 to 11 has in bit 1 a value that generates a "001011" pattern along an MF. The other time slots (1 to 31) are responsible for carrying voice and/or data. As the frame repetition rate is 8KHz, the basic frequency of the frame is 2048KHz. Time slot 16 can be used by higher level protocols to carry control information such as signaling start and end of a phone call.

III. DROP_INSERT DESIGN

The Drop_Insert circuit main function is threefold. It receives E1 frames coded either in HDB3 or AMI formats and a binary data stream to insert in the incoming frame, of ASCII text from word processor of the external source. Then, it replaces a contiguous set of time slots in the incoming E1 frame with the data in the binary stream. Finally, the new E1 frame and the dropped set of time slots are sent to the external world. These functions are executed continuously, in real-time.

Figure 3.2 shows the block diagram for the Drop_Insert IP soft core. The communication with the external world can be roughly divided into four interfaces:

(*i*) E1(2Mbps) input-output; (*ii*) binary data stream;
(*iii*) service channel; (*iv*) control

The E1 input/output interface comprises two pairs of differential signals, (*DI+* , *DI-*) and (*DO+* and *DO* -), being the signal *code* responsible for selecting between HDB3 or AMI formats. The signal *f2m* is the synchronizing clock for reception and transmission of E1 frames.

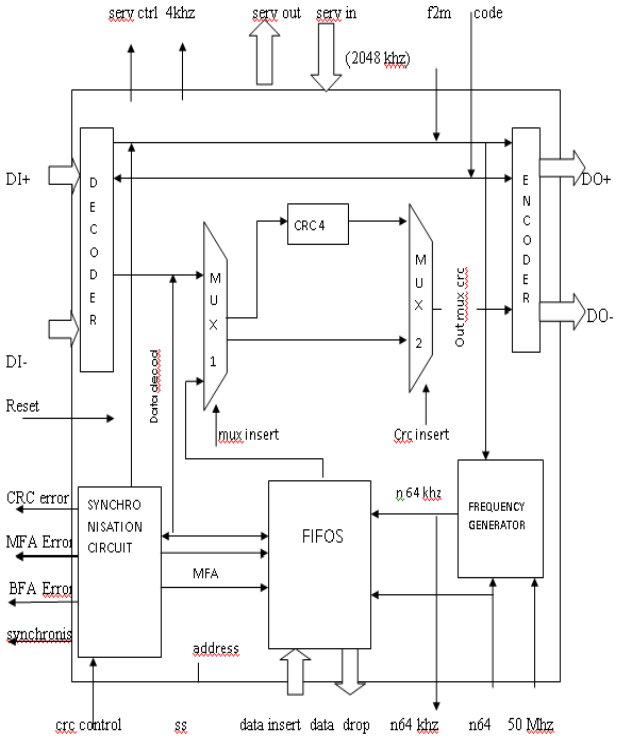


Fig 3.1 – Block diagram of drop _ Insert

The binary data of add signal & its associated control signal depends on the 5bit control input. The first timeslot is replaced & determined by the only after verification of the 5-bit control input otherwise error condition occurs.

This signal is internally generated from the *50MHz* input reference clock signal. The jitter tolerance specified in the ITU standard is 50 ppm. The *synchronized* signal informs when the system is synchronized.CRC operation is implemented by the *CRC Control* input signal, which controls the enabling of the CRC computation and by *CRC Error* output signals, which notify the presence of CRC errors.The ***Decoder*** converts an electrical signal in one of two formats, HDB3 or AMI, into a logical signal, the bits of the E1 frame (*data Decod* internal signal). The ***Encoder*** has functionality opposite to that of the Decoder. The ***CRC4*** module computes and inserts the CRC into the SMF following the current SMF. The ***Frequency Generator*** is based on the 50MHz external clock, generating the *n64KHz* frequency, being *n64KHz* a 64KHz multiple frequency, in the range from 1 to 31, as defined by the *n64* input. The ***Synchronization Circuit*** is responsible for frame and MF synchronization, and for operation with or without CRC. This module controls multiplexers *mux1* and *mux2*, using the signals *mux insert* and *CRC insert*.

The ***FIFOS*** module is a structure that allows inserting and dropping information to and from an E1 frame. This FIFOS module is needed to adapt the distinct bit rates found in the E1 carrier line and the *data Insert*/*data Drop* lines. It receives bits from the *data Insert* input at rates smaller than 2048Kbps,controlled by the *n64KHz* input, and sends bits through the *data Drop* output at the rate specified in the *n64KHz* input.

IV. RESULTING OUTPUT WAVE FORMS

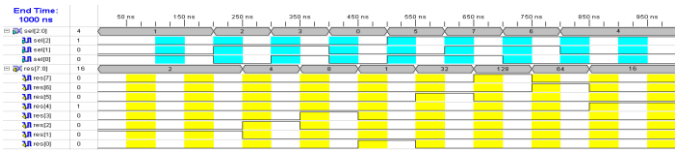


Fig 4.1 output waveform for 3-to-8 DECODER

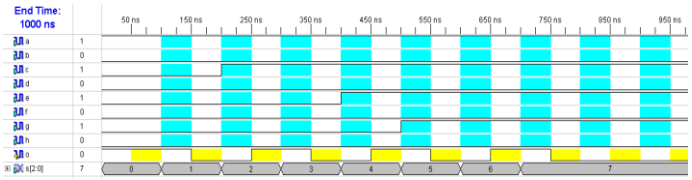


Fig 4.2 output waveforms for 8 to 1 Multiplexer

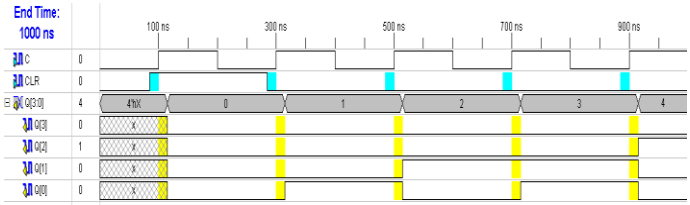


Fig 4 .3 output waveforms for 4-bit unsigned up counter with asynchronous clear

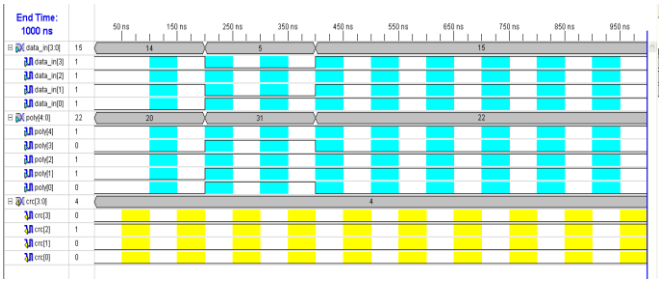


Fig 4.4 output waveforms for crc 4

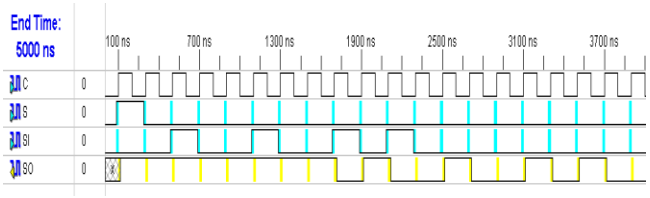


Fig 4.5 output waveform for Shift-Left Register

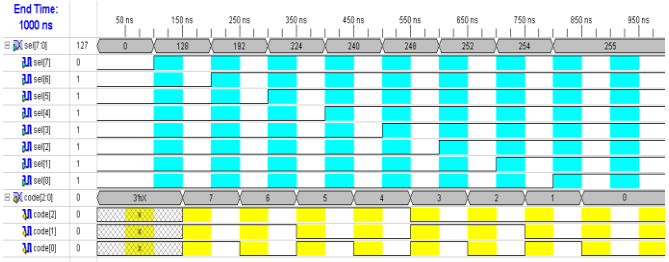


Fig 4.6 output waveform for1-of-9 Priority Encoder

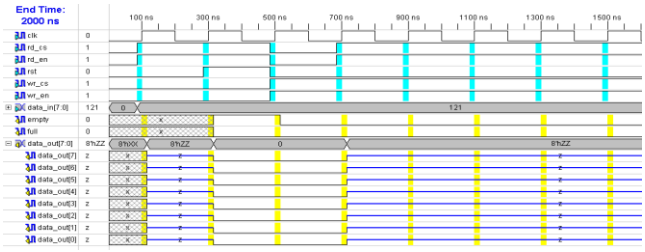


Fig 4.7 output waveform for Synchronization circuit

V. CONCLUSION

The hardware module designed for the add-drop functions of 2Mbps carriers. For better solution than in the current availability in the VLSI design. The timing constraints in the implementation were not critical in the design. The only timing restriction that posed some problem to be fulfilled was the n64 frequencies generation with the jitter tolerance specified in the ITU standard, namely 50 ppm.

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