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Implementation of Two Level DWT VLSI Architecture

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ABSTRACT
The digital data can be transformed using Discrete Wavelet Transform (DWT). The images need to be transformed without loosing of information. The Discrete Wavelet Transform (DWT) was based on time-scale representation, which provides efficient multi-resolution. The lifting based DWT are lower computational complexity and reduced memory requirements. The discrete wavelet transform (DWT) is being increasingly used for image coding. This is due to the fact that DWT supports features like progressive image transmission (by quality, by resolution), ease of transformed image manipulation, region of interest coding, etc. DWT has traditionally been implemented by convolution. DWT has traditionally been implemented by convolution Such an implementation demands both a large number of computations and a large storage features that are not desirable for either high-speed or low-power applications. In this work, the design of Lossless 2-D DWT (Discrete Wavelet Transform) using Lifting Scheme Architecture will be modeled using the Verilog HDL and its functionality were verified using the Modelsim tool and can be synthesized using the Xilinx tool.

I. INTRODUCTION

The aim of this brief paper is to construct an efficient single input/single output(SISO) VLSI architecture based on lifting scheme, which meets the high processing speed requirement with controlled increase of hardware cost and simple control signals.
High processing speed can be achieved when multiple row data samples are processed simultaneously. And time multiplexing technique is adopted to control the increase of the hardware cost.

Furthermore, the control signals are simple, since the regular architecture is a combination of simple single-input/single-output (SISO) modules and two-input/two-output (TITO) modules. It provides a variety of hardware implementations to meet different processing speed requirements the rapid progress of VLSI design technologies, many processors based on audio and image signal processing have been developed recently. The two-dimensional discrete wavelet transform (2-D DWT) plays a major role in the JPEG-2000 images compression standard. Presently, research on the DWT is attracting a great deal of attention. In addition to audio and image compression the DWT has important applications in many areas, such as computer graphics, numerical analysis, radar target distinguishing and so forth. The architecture of the 2-D DWT is mainly composed of the multi rate filters. Because extensive computation is involved in the practical applications, e.g., digital cameras, high efficiency and low-cost hardware is indispensable. At present, many VLSI architectures for the 2-D DWT have been proposed to meet the requirements of real-time processing.

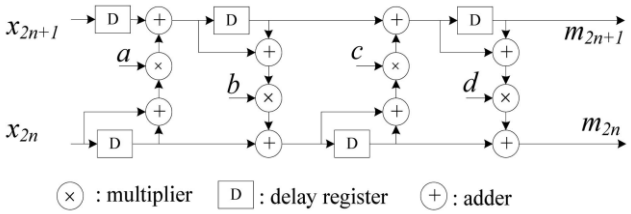


Fig. 1. Two-input/two-output lifting architecture of the CDF97.

However, because the filtering operations are required in both the horizontal and vertical directions, designing a highly efficient architecture at a low cost is difficult. Lewis and Knowles used the four-tap Daubechies filter to design a 2-DDWT architecture. Parhi and Nishitani proposed two architectures that combine the word-parallel and digital-serial methodologies. Chakrabarti and Vishwanath presented the non-separable architecture and the SIMD array architecture. Vishwanath *et al.* employed two systolic array filters and two parallel filters to implement the 2-D DWT. The modified version uses four parallel filters as reported in [15] and [16]. Chuang and Chen [17]proposed a parallel pipelined VLSI array architecture for the 2-D DWT. Chen and Bayoumi [18] presented a scalable systolic array architecture. Other 2-D DWT architectures have been reported Among the various architectures, the best-known design for the 2-D DWT is the parallel filter architecture. Therefore, in this paper, we propose a new VLSI architecture for the separable 2-D DWT. The advantages of the proposed architecture are the

100% hardware utilization, fast computing time, regular data flow, and low control complexity. Additionally, because of the regular structure, the proposed architecture can easily be scaled with the filter length and the 2-D DWT level.

This paper is organized as follows. Section II introduces the 2-D DWT algorithm. Section III discusses the previous design techniques. In Section IV, an efficient architecture for the 2-D DWT is proposed. Section V compares the performance of various 2-D DWT architectures.

II. LINE-BASED 2-D WAVELET TRANSFORM

Image data is usually acquired in a serial manner. For example, a very common way to acquire image data is to scan an image one line at a time. Throughout this paper, we will assume our system operates with this line-by-line acquisition. Given this, our objective in this section will be to design a 2-D WT that requires *storing a minimum total number of lines*. The assumption is that images are stored in memory only while they are used to generate output coefficients, and they are released from memory when no longer needed. Obviously, performing a 1-D WT on a single line can be done without significant memory. However, in order to implement the separable 2-D transform the next step is to perform column filtering and here memory utilization can become a concern. For example, a completely separable implementation would require thus memory sizes of the order of the image size will be required.

III. LIFTING SCHEME OF DWT

Lifting scheme is a relatively new method to construct wavelet bases, which was first introduced by Sweldens in 1990s [4]. This scheme is called the second-generation wavelet, which leads to a fast in-place implementation of the DWT. According to [4], any DWT of perfect reconstruction can be decomposed into a finite sequence of lifting steps. This decomposition corresponds to a factorization for the poly-phase matrix of the target wavelet filter into a sequence of alternating upper and lower triangular matrices and a constant diagonal matrix, which can be expressed as follows

$$h(z) = h_e(z^2) + z^{-1}h_o(z^2)$$
$$g(z) = g_e(z^2) + z^{-1}g_o(z^2)$$
$$P(z) = \begin{bmatrix} h_e(z) & g_e(z) \\ h_o(z) & g_o(z) \end{bmatrix} = \prod_{i=1}^{m} \begin{bmatrix} 1 & s_i(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ t_i(z) & 1 \end{bmatrix} \begin{bmatrix} K_0 & 0 \\ 0 & K_1 \end{bmatrix}$$

Where h(z) and g(z) are the low-pass and high-pass analysis filters, respectively. Equation (1) is the poly-phase decomposition and P(z) is the poly-phase matrix. For example, the (9, 7) filter (CDF97) adopted in JPEG2000 can be decomposed into four lifting stages as follows

$$P(z) = \begin{bmatrix} 1 & a(1+z^{-1}) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ b(1+z) & 1 \end{bmatrix} \begin{bmatrix} 1 & c(1+z^{-1}) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ d(1+z) & 1 \end{bmatrix} \begin{bmatrix} K_0 & 0 \\ 0 & K_1 \end{bmatrix},$$

Where a, b, c, and d are the lifting coefficients, and K_0, K_1 are the scale normalization coefficients. The scale normalization coefficients can be implemented together with the quantization, if image compression is performed [7]. Thus, we focus on the implementation of the lifting stages in this brief paper. The odd (even) indexed data samples are represented by x_{2n+1} (x_{2n}). The intermediate values computed during lifting steps are denoted as m^k_{2n+1} and m^k_{2n} (k = 0, 1, 2, 3), and the high- and low-frequency coefficients are expressed as the sequence m_{2n+1} and m_{2n}, respectively. With these mathematical notations, the implementation of the CDF97 can be rewritten as follows:

$$\begin{aligned}
{m^0}_{2n+1} &= x_{2n+1} \\
{m^0}_{2n} &= x_{2n} \\
{m^1}_{2n+1} &= {m^0}_{2n+1} + a({m^0}_{2n} + {m^0}_{2n+2}) \\
{m^1}_{2n} &= {m^0}_{2n} \\
{m^2}_{2n+1} &= {m^1}_{2n+1} \\
{m^2}_{2n} &= {m^1}_{2n} + b({m^1}_{2n-1} + {m^1}_{2n+1}) \\
{m^3}_{2n+1} &= {m^2}_{2n+1} + c({m^2}_{2n} + {m^2}_{2n+2}) \\
{m^3}_{2n} &= {m^2}_{2n} \\
m_{2n+1} &= {m^3}_{2n+1} \\
m_{2n} &= {m^3}_{2n} + d({m^3}_{2n-1} + {m^3}_{2n+1})
\end{aligned}$$

Based on (3), the two-input/two-output lifting architecture of the CDF97 is shown in Fig. 1.

Architecture for the Horizontal Filtering along the Rows (M = 8)

First, CDF97 is applied to the row dimension, which is a 2D DWT. The architecture for the horizontal filtering along the rows consists of eight SISO modules, as shown in Fig. 2. The input data flow is shown in Fig. 3.The elements from each row are processed by one SISO module. We can accordingly get output data flow of the architecture for the horizontal filtering, as shown in Fig. 4, where $m_{i,j}$ denotes the computation results after we apply CDF97 to the row dimension.

Many SISO architectures for the 2D DWT are proposed. An efficient SISO architecture is proposed in by employing the fold technique. Therefore, we adopt it in our SISO modules, which consists of two multipliers, four adders, and ten registers

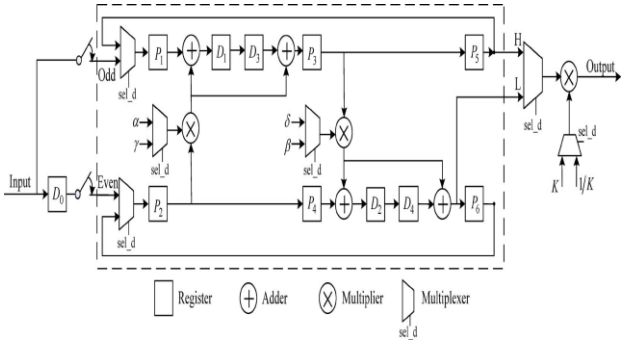


Fig. 2.Proposed Folded Architecture.

Architecture for the Vertical Filtering along the Columns (M = 8)

Second, CDF97 is applied to the column dimension. Eight elements (for example, $m_{0,0}$, $m_{1,0}$ . . .$m_{7,0}$) from each column arrive simultaneously. One solution is to design an eight-input/eight-output architecture by directly mapping, which can process eight elements per clock cycle. However, it will lead to a complex architecture, which has complicated control signals and cannot be easily extended for its irregularity. For example, a four-input/four output can process four elements from each column per clock cycle. The eight-input/eight-output architecture will be more complicated.

Each TITO module is designed to receive two elements simultaneously. The LD is composed of some delay registers, which are used to temporarily store the elements. Port A (Port B, Port C ....Port H) is used as a symbol to demonstrate how the mux works. The elements, which have been delayed by the LD, will be selected by the mux and sent to TITO modules at a proper time.

The number of delay registers in LD (LD1, LD2, LD3) is determined by the rule: The time interval arriving at the same TITO module for every two elements from one column is constant. The time interval is measured by the number of clock cycles (ccs).We assume that the length of the image is N pixels, the throughput rate of proposed architecture is M pixels/ccs, and the computation time interval between the first pair and the second pair of the elements from one column is ccs. Therefore architecture by directly mapping (3) is shown in Fig. 3,

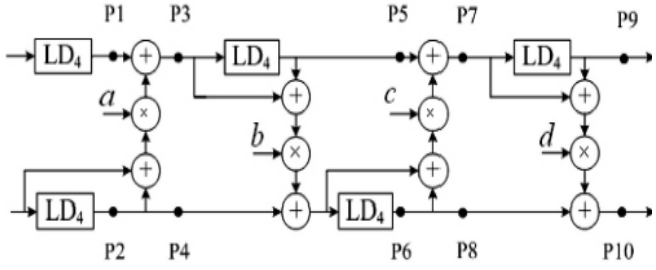


Fig. 3. Architecture of the TITO module.

the number of the input in the architecture for the vertical filtering is M, then the computing time interval between the first pair and the (M=2 þ 1)th pair(such as m0;0, m1;0 and m8;0, m9;0) is M=2 _ _ ccs. On the other hand, from Figs. 4 and 6, the time interval between the first pair and the (M=2 þ 1)th pair arriving at the same TITO module is equal to

$$\frac{N \text{ pixels} \times M}{M \text{ pixels/ccs}} = N\text{ccs}.$$

Therefore, the following formula should be satisfied:

$$\frac{M}{2} \times \Delta = N.$$

By solving (5), we have that

$$\Delta = 2N/M.$$

The selected time interval for the mux from one input port to another is equal to ccs. Because every two elements from one column will arrive at the same TITO module with a fixed time interval, the architecture of the TITO module can be constructed by replacing the delay registers used in Fig. 1 with corresponding LD4. The architecture of the TITO module is shown in Fig. 3. The LD4 is used to synchronize the intermediate results of the vertical filtering, in which the number of delay registers is equal to ccs. An example is given to show the data flow in a TITO module (PORT E). P1 (P2, . . . P10), as shown in Fig. 3, is the intermediate node of the architecture of TITO module, which is used to show how the vertical filtering is processed. The data flow is shown in Table 1, where mm_{ij} denote the computation results after CDF97 is applied to the column dimension. The subscript i and j represent the coordinates of the results. And mm_{ij}^{k} (k =0, 1, 2, 3) denote the intermediate results of the vertical filtering, which are calculated as in (3). For example, $mm_{1,0}^{1}$, can be calculated from $mm_{0,0}^{0}$, $mm_{1,0}^{0}$ and $mm_{2,0}^{0}$of the same column. Based on (3), Figs. 8 and 9, and Table 1, it can clearly show how the computation results are calculated.

IV. ANALYSIS AND COMPARISON

To evaluate the performance of the proposed architecture, different 2D DWT architectures are compared in terms of hardware cost, on-chip memory, computing time, etc.

The hardware cost is measured by the number of multipliers and adders used in the architecture. The on-chip memory refers to the number of registers consumed (the width of the register is equal to the word length for the internal data). The computing time is normalized as clock cycles. Compared with the similar architectures, computing time of siso is reduced with less increase of hardware cost. For example, M is equal to two. SISO

two-output architecture, the computing time of which is N2=2.

Compared with the architectures of the proposed MIMOA has the least consumption of hardware cost and on-chip memory. However, the best advantage of the proposed architecture is that it provides a variety of hardware implementations to meet different processing speed requirements by selecting different throughput rates. The architecture proposed by Cheng is also designed to achieve high processing speed. However, compared with the proposed architecture (M = 4), it needs more hardware cost in the same computing time (N2=4) for its FIR structures. Then a conclusion can be made that the SISO has a good performance in terms of the reduction of computing time and hardware cost, which will be an efficient alternative for future high-speed applications.

The Verilog HDL descriptions of the architectures are generated and synthesized on an Altera stratix EP1S25B672C7. The test image size is 1024*1024 pixels. The pipeline technology is used to increase the maximum operating frequency(Fmax).

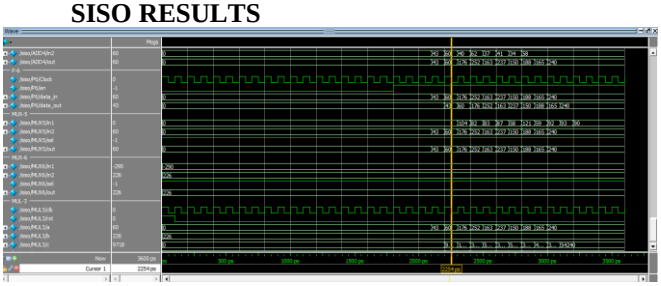
TABLE 1
Experimental Results among Different 2D DWT Architectures for the CDF97

Architecture	Logic	Register	Memory (Bits)	F_{max}(MHz)	Computing Time(us)
Barua[11]	3984	2727	114688	65.37	8.020
Cheng[12]	12330	8070	491520	58.73	4.464
MIMOA(*M*=2)	3180	2378	81920	65.38	8.019
MIMOA(*M*=4)	7017	5182	98304	64.25	4.080
MIMOA(*M*=8)	15409	11302	131072	63.52	2.063

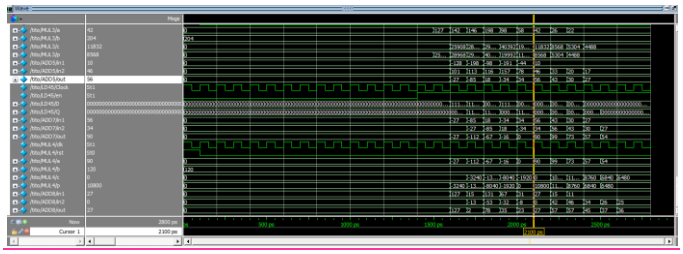
Under close computing time, the number of the logics, registers, and memories in the proposed architecture (M ¼ 2) is reduced by 20.2 percent, 12.8 percent, and 28.6 percent, compared with the architecture . The number of the logics, registers, and memories in the proposed architecture (M ¼ 4) is reduced by 43.1 percent, 35.8 percent, and 80 percent, compared with the architecture . Meanwhile, the best advantage of the proposed architecture is that it provides a variety of hardware implementations to meet high processing speed requirement. For example, the computing time of the proposed architecture can be reduced to 2:063 _s, if M is equal to eight. Therefore, the above conclusion has been confirmed.

V. RESULTS

SISO RESULTS



TITO RESULTS



VI. CONCLUSION

In this brief, we have proposed a novel EFA for the lifting based DWT. We have given a new formula for the conventional lifting algorithm**.** Then, by employing the of SISO techniques, the conventional data flow of the lifting-based DWT is converted to a parallel one, resulting in the OA with repeatable property. Based on this property, the proposed EFA is derived from the OA by further employing the fold technique.

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