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Design and Implementation of Glitch-Free Phase Switching Plls to Suppress Quantization Noise

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Abstract
A programmable frequency divider for quantization noise suppression in fractional- phase-locked loops is presented in this paper. The proposed phase switching Multi-modulus frequency divider (PS-MMFD) utilizes a novel glitch-free phase switching (PS) divide-by-0.5/1/1.5/2 cell to reduce the frequency division step to 0.5 and its QN induced by modulation is thus suppressed by additional 6 dB. Compared with other frequency dividers used for QN suppression, the proposed glitch-free PS-MMFD is more robust, can operate at higher input frequency and consumes less power.
Key Words—Glitch-free, phase switching (PS), phase switching multi-modulus frequency divider (PS-MMFD), phase-locked loops (PLLs), quantization noise (QN) suppression

I. INTRODUCTION

In wireless communication systems the Δ Σ fractional n-phase locked loop(pll) is widely used allowing tradeoffs among PLL design constrains for phase noise, settling time, Frequency resolution .The ΔΣ modulator generates a pseudo-random bit sequence to dither the instantaneous division ratio and its time-average value equals to the required fractional division ratio. However, since the internal step of the frequency divider still remains discrete, the quantization error, i.e., the deviation from the desired fractional division ratio, introduces the quantization noise (QN) and deteriorates the overall phase noise performance especially for wideband PLLs. Several researchers used digital-to-analog converter (DAC) controlled current branches to compensate for the QN The performance is mainly limited by the mismatch from DAC digital value to its analog counterpart .Many recent publications have been progressively improving the mismatch .Many adaptive algorithms like 2.GHZ ΔΣ fractional NPLL with mb/sec in loop modulation is 700KHZ Band width ΣΔ fractional synthesizer with suprs compensation and linearization techniques for CDMA applications are used the most straight forward way to suppress the QN is to decrease the quantization step I.e. the internal division step in ΔΣ fractional –NPLL's the QN is suppressed by 6DB if reducing division step by half. The key principle is to trigger the frequency divider on either rising or falling edges of the input signal to perform the double edge triggering the robustness of the frequency dividers cannot be guarantee at high input frequency because though operating frequency is actually twice of the input signal frequency in this paper In this paper, a novel circuit technique, glitch-free phase switching multi-modulus frequency divider (PS-MMFD) to suppress the QN in a ΔΣ fractional- PLL, is proposed. The division step of the PS-MMFD is 0.5, and its QN induced by ΔΣ modulation is thus suppressed by additional 6 dB. In addition, the PS-MMFD could operate at a higher frequency since its internal operating frequency is not doubled.

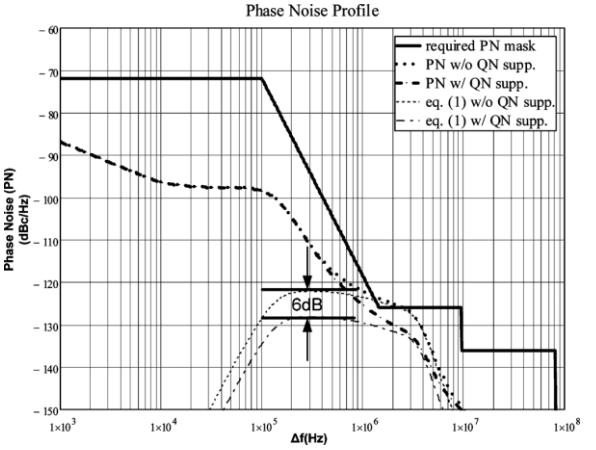

Fig 1. Phase noise profile with and without QN suppression

II. The pulse-swallow frequency divider and the truly modular frequency divider are widely used in PLLs for wireless communication systems.

1) Pulse-Swallow Frequency Divider for QN Suppression:

It is different from the traditional architectures the pulse-swallow frequency divider with QN suppression adopts dual-modulus prescalar with step size of 0.5 instead of 1 as shown in Fig. 2. The dual-modulus prescalar divides the input frequency Fin either by N or N+0.5 according to the modulus control signal mod. When *mod* is high, the DTFF is enabled, and generates a signal which lags half input cycle of selected DFF output. The signal feedbacks to DFFs input and a half input cycle is swallowed due to

its delay. Two issues limit the use of this divider in PLLs for wideband wireless communication systems. First, the minimum continuous division ratio $2\times N^2$ is twice as that of divide-by –N/N+1 the extra circuits are operating at the highest frequency f_{in} with double-edge-triggered operation and the total power consumption is almost doubled.

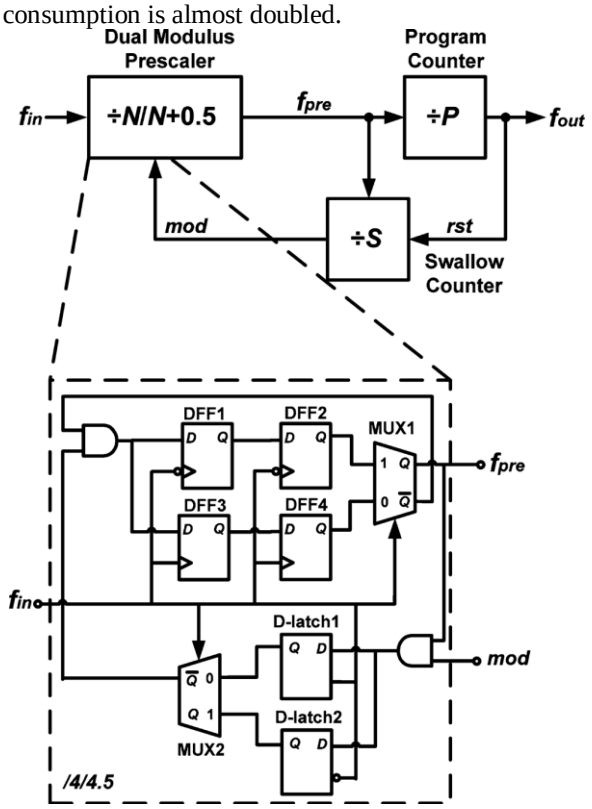

Fig 2. pulse swallow frequency divider

2) Truly Modular Frequency Divider for QN Suppression:

Truly modular frequency divider with QN suppression composed of a divide-by-1/1.5 (/1/1.5) divider cell , a traditional divide-by-2/3 (/2/3) chain, and a few logic gates to extend the division ratio The topology of the /1/1.5 divider cell added in front of the /2/3 chain is shown in Fig. 4 . It is used to achieve QN suppression by reducing the division step to 0.5. The /1/1.5 divider cell consists of two parts, i.e., the prescalar logic and the end-of-cycle logic. When both *mod* and are high, it is in divide- by-1.5 mode, the prescalar logic swallows half input cycle due to the delay of end-of-cycle part; otherwise, the /1/1.5 divider cell tracks the input by the DFF composed of D-latch1 and D-latch2. The end-of-cycle part is based on a DTFF which inherently doubled the operating frequency of the divider. Potential timing racing problem exists due to the relationship of the input-to-DFF delay (or input-to-latch delay) and input-to-MUX delay in divide-by-1.5 mode. Furthermore, employing the /1/1.5 divider cell suppresses the QN induced phase noise but increases power consumption by about 20% and decreases the maximum operating frequency.

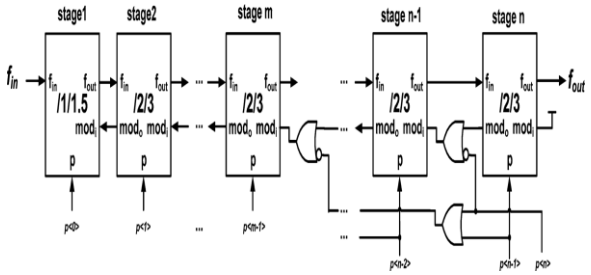

Fig 3.truly modular frequency divider with QN suppression

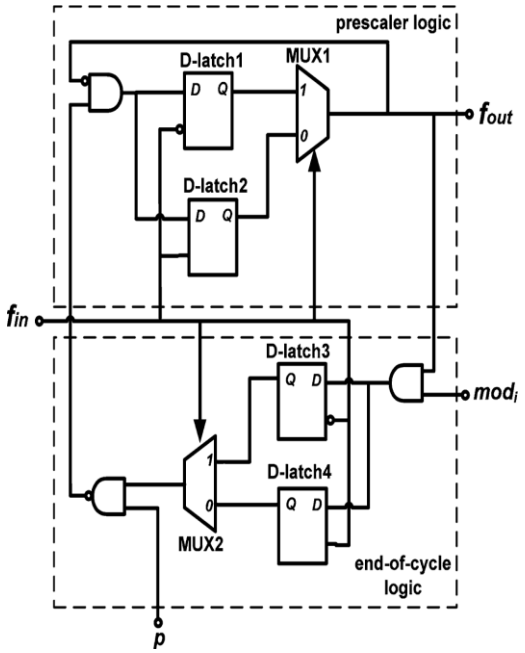

Fig 4. /1/1.5 divider cell

3) Summary*:* Both aforementioned programmable frequency dividers for the QN suppression are based on double-edge-triggering. Though it achieves a 0.5 division step, double-edge-triggering limits the highest input frequency of the frequency divider and demands larger power consumption because the frequency divider essentially operates at twice of the input frequency.

III. PHASE SWITCHING MULTI-MODULUS FREQUENCY DIVIDER

A novel multi-modulus frequency divider based on a divide- by-0.5/1/1.5/2 (/0.5/1/1.5/2) cell utilizing glitch-free phase switching (PS) technique is proposed to improve the performance for the QN suppression. Compared with the techniques discussed in Section II, the proposed PS-MMFD is robust without any timing racing or glitch problems and achieves the desired 6 dB QN suppression while consuming less power and Operating at higher input frequencies.

A. Unconditional Glitch-Free Phase Switching

The basic idea of phase switching is first proposed in [17] as shown in Fig. 5(a). The high-frequency input f_{in} directly feeds into a divide-by-2 quadrature phase generator and the four 90^0 phase

apart outputs, are Grey-Coded as states (00) (0^0), (01) (90^0),(11) (180^0), and (10) (270^0).When a PS is required, the output switches to the next state [e.g., from (11) (180^0) to (270^0) as shown in Fig. 5(a)]. Compared with the waveform of no PS occurrence, the rising edges are moved backward by half of the input f_{in} cycle as the solid arrows indicate in Fig. 5a When the PS occurs at time , it operates properly. However, if the PS occurs a little earlier at , an unwanted narrow pulse is generated. Although the rising edges of the output are moved backward as normal, an additional rising edge would be counted because of the unwanted pulse (glitch). The phase information will be corrupted and the function of the overall frequency divider would be failed. Glitches can be avoided by using long rising time control signals for output selecting multiplexer which is not a robust solution A retimer circuit can also be inserted between the quadrature phase generator and the multiplexer to synchronize the four outputs and the corresponding control signals before they feed into the multiplexer to eliminate the glitches However, this solution increases the circuit complexity. The simplest solution for the undesirable glitch problem is Shown in Fig. 5(b) . In this case, the rising edges are moved forward by half of the input cycle f_{in} as the solid arrows indicate. Different from the backward movement, whether the PS occurs at t_1 or t_2, the only difference is the duty cycle of Current period, and such duty cycle variation will not influence the function of the frequency divider.

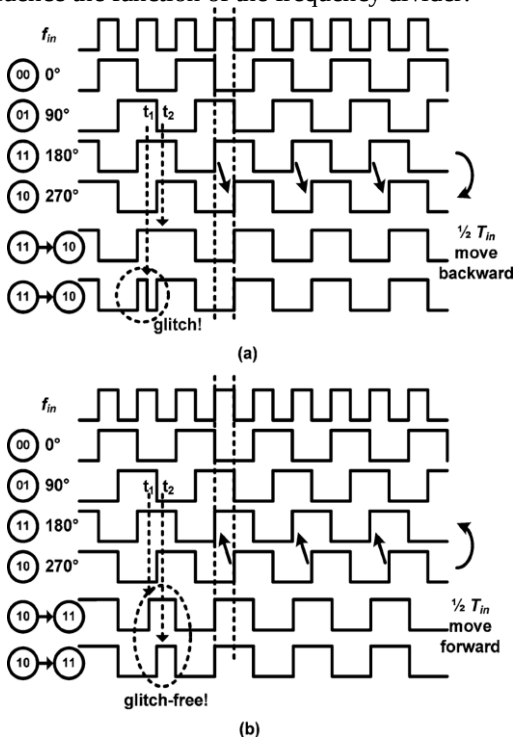

Fig.5. Phase switching. (a) Glitch-occurred. (b) Glitch-free

In summary, for unconditionally glitch-free PS between the current phase state and the next phase state, the next phase state has to be in its logic high when the rising edges of the current phase state occur. For example, the PS from (10)(270^0) to (11) (180^0) (as shown in Fig. 5) is glitch-free while it is not the case for the PS from (10) (270^0) to (01)(90^0). This is because the rising edges of (10)(270^0) see the logic high in (11)(180^0) but the transition moments in (01) (90^0). The PS from the current phase state to its corresponding lead-90 phase state, i.e., the nearest-reversed-state PS, is guaranteed to be glitch-free as shown in Fig. 5(b).

B. Proposed Glitch-Free PS-MMFD

The overall architecture of the proposed Phase Switching multi-modulus frequency divide (PS-MMFD) is shown in Fig. 6. It is mainly composed of a divide-by-0.5/1/1.5/2 (/0.5/1/1.5/2) cell, several divide-by-2/3 (/2/3) cells and the
division range extension logic circuit. The frequency division ratio, , is controlled by the 10 bit division ratio control input, p<9:0> . With the division range extension logic

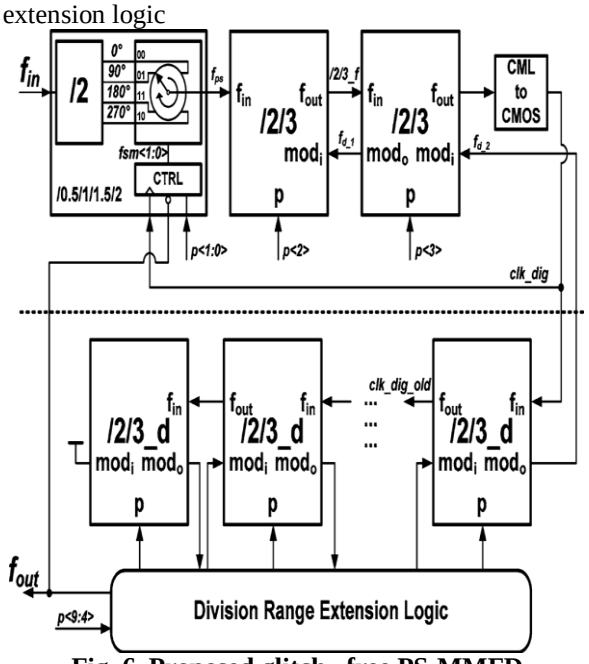

Fig. 6. Proposed glitch –free PS-MMFD architecture

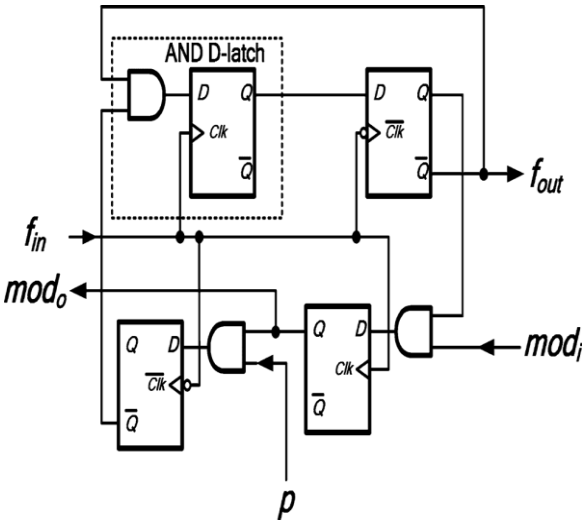

Fig.7. Divide-by-2/3 cell.

C. Divide-by-0.5/1/1.5/2 Cell

The operating principle of the divide-by-0.5/1/1.5/2 (/0.5/1/1.5/2) cell extends the basic glitch-free phase switching technique. It is composed of a divide- by-2 quadrature phase generator, a phase selector and a digital controller CTRL, as shown in Fig. 6. The divide-by-2 in /0.5/1/1.5/2 cell works at full speed (f_{in}), and generates four Grey-coded outputs whose rising edges (or phases) are separated by 90^0 . At any instance, only one of the divide-by-2 outputs is connected to the subsequent /2/3 chain through a 2-bit MUX. The MUX is controlled by the 2-bit word Fsm ‹1:0›, given by the control circuit block (CTRL).

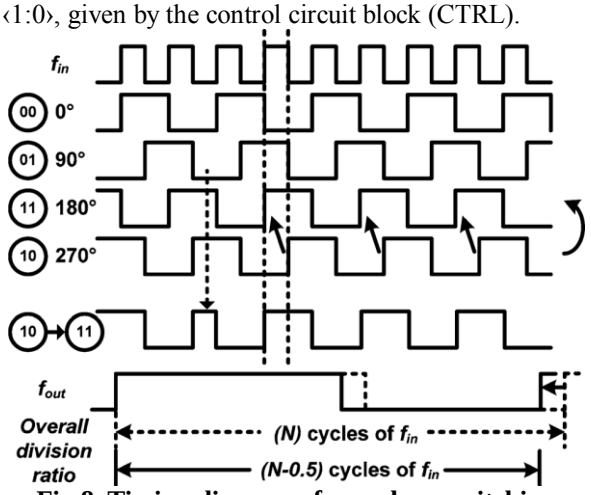

Fig.8. Timing diagram of one phase switching

In order to achieve e the required four division ratios (/0.5/1/1.5/2), the CTRL logic for glitch-free PS has to be carefully designed. To guarantee the operation of unconditionally glitch-free phase switching in /0.5/1/1.5/2 cell, the CTRL logic has to ensure that only nearest-reversed-state PS can be performed through the MUX. When one nearest-reversed-state PS is finished, the following rising edges of the /0.5/1/1.5/2 cell output phase state seem to be moved forward by one half input (fin) compared to the original output phase state, effectively reducing the period of final divider output by half input cycle, i.e., divide-by- (N-0.5)becomes divide-by- as depicted in Fig. 7. In order to obtain the continuous division ratio stepped by 0.5, the phase switching module should be able to conduct 0-3 times of nearest-reversed-state PS in an output f_{out} cycle to realize the divide-by-/0.5/1/1.5/2. For the sake of convenience, assume that the output of the MUX initially selects (10)(270^0) and the same analysis can be applied to other initial conditions. The operating procedure of the /0.5/1/1.5/2 cell depends on the number of nearest-reversed state PS occurred in one output f_{out} cycle, which is determined by the instantaneous division ratio. Different situations are analyzed as follows.

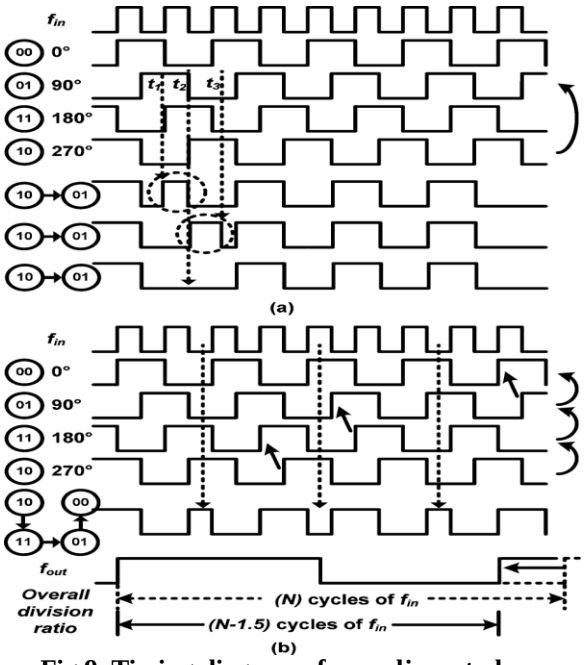

Fig.9. Timing diagram of nonadjacent phase switching.(a) direct phase switching.(b) Multiple phase switching's.

1)No PS Occurred:

The control signal, fsm ‹1:0› does not change, and the MUX would stay at (10)(270^0). The /0.5/1/1.5/2 cell operates as a simple divide-by-2 cell, and the output of the /0.5/1/1.5/2 cell, fps is the same as initial state (10)(270^0).

2) Only One Nearest-Reversed-State PS:

As an example shown in Fig. 8, the state change from (10)(270^0) to (11)(180^0) Requires only one nearest-reversed-state PS. The dotted arrow shown in Fig. 8 indicates the moment of PS occurrence. No matter when the PS occurs, there is no difference except the duty cycle of one period at the moment of PS. As we discussed before, nearest-reversed-state PS (10)-> (11) or (11)-> (01) or (01)->(00) or (00)-> (10) in each output cycle guarantees the MUX output to be glitch-free. Compared with case 1), the rising edges of f_{ps} are brought forward by a half input f_{in} cycle after the PS occurrence, as the solid arrows indicate (shown in Fig. 8), effectively reducing the period of final divider output by half input cycle, i.e., the /0.5/1/1.5/2 cell operates as a simple Divide-by-1.5 cell.

3) Multiple Nearest-Reversed-State PSes*:* Direct PS with more than one half-input-cycle phase change (nonadjacent phase switching), e.g., two-half-input-cycle PS from (10)(270^0) To(01) (90^0) or three-half-input-cycle PS from (10)(270^0) to (00)(0^0), is not guaranteed to be glitch-free. Whether or not a glitch occurs depends on when the PS happens [e.g t1,t2 or T3 shown in Fig. 9(a)]. For example, the direct PS from (10)(270^0) To (01) (90^0) would generate an unwanted glitch which corrupts the frequency divider function, if the PS occurs earlier or later as shown in Fig. 9(a). In order to achieve a glitch-free operation, multiple nearest reversed- state PSes should be used in

series combination to accomplish the nonadjacent phase state switching. For example, two-half-input-cycle PS from (10) (270^0) to (01)(90^0) is guaranteed to be glitch-free if done in two nearest-reversed-state PS steps, (10)(270^0) to(11) (180^0) to (01)(90^0); and three-half-input-cycle PS from (10)(270^0) to(00) (0^0) is guaranteed to be glitch-free if done in three nearest-reversed-state PS steps, (10)(270^0) to (11)(180^0) to(01) (90^0) to(00) (0^0), as shown in Fig. 9(b). Two-half-input-cycle PS from (270^0) to (90^0) is guaranteed to be glitch-free if done in two nearest-reversed-state PS steps, (270^0) to (180^0) to (90^0); and three-half-input-cycle PS from (270^0) to (0^0) is guaranteed to be glitch-free if done in three nearest reversed-state PS steps, (270^0) to (180^0) to (90^0) to (0^0), as shown in Fig. 9(b).

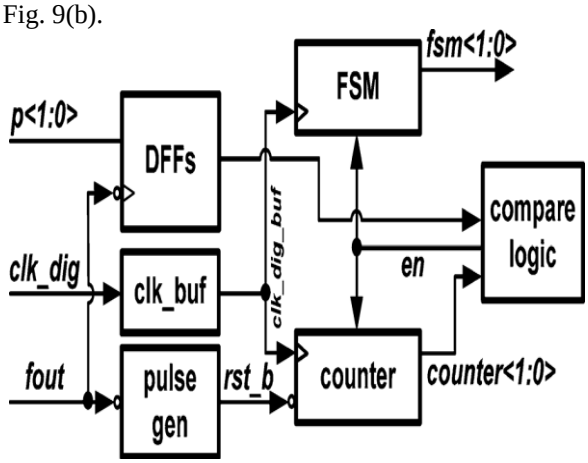

Fig.10. CTRL circuit block

Fig. 10 shows the detailed implementation of the CTRL circuit block. The CTRL is mainly composed of a pulse generator, a grey-coded finite state machine (FSM), a 2-bit counter and some logic control circuits (compare logic). The topology of the pulse generator is shown in Fig. 11(a) . The data input of the positive latch is always connected to logic high. For each falling edge of the clock signal, the output follows the input to transfer to logic high if *rst* signal is disabled. However, the output is also served as the *rst* signal through a delay cell which will set the output to logic low. The transient waveforms of the pulse generator are shown in Fig. 11(b). As can be seen from Fig. 11(b), a short pulse *rst_b* is generated to reset the 2-bit counter to state (00) at each falling edge of the PS-MMFD output f_{out} . The digital clock, *clk_dig*, passing through a buffer, synchronizes the FSM and the 2-bit counter by its falling edges. The state transition graphs of the FSM and the 2-bit counter are shown in Fig. 12(a) and (b), respectively. The input p‹1:0›which gives the total number of required glitch-free nearest-reversed- state PS steps in current output f_{out} cycle is synchronized by the falling edges of the PS-MMFD output f_{out} before it is compared with the number of finished glitch-free nearest-reversed- state PS steps in the compare logic (CL) circuit block.

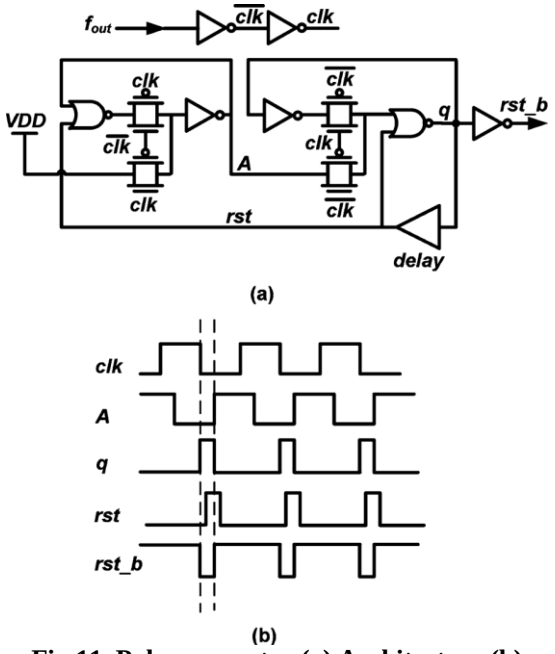

Fig.11. Pulse generator (a) Architecture (b) Transient Waveforms

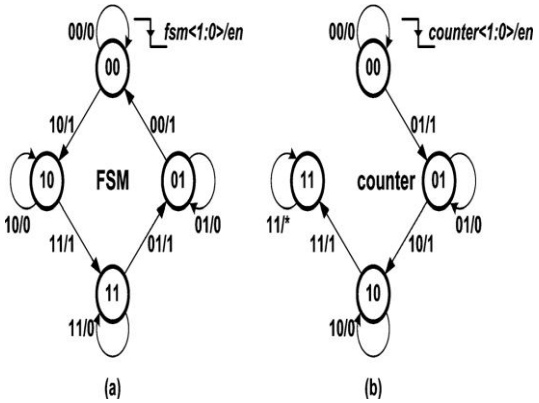

Fig.12. State transition graphs (a) FSM (b) 2 bit controller

The CL output, *en*, which controls the operating state of the FSM and the 2-bit counter, will remain valid before all required glitch-free nearest-reversed-state PS steps finished. The output of the CTRL, i.e., the output of the FSM, gives the 2-bit MUX control word Fsm <1:0> to control the switching among the four phase states

IV. Conclusion

In this paper, a novel multi-modulus frequency divider architecture utilizing glitch-free phase switching is proposed to achieve half-stepped division ratios and thus QN suppression in fractional-PLLs. The proposed PS-MMFD is unconditionally glitch-free and achieves 6-dB QN suppression thanks to its half-step division. The proposed PS-MMFD is able to operate at higher input frequency and consume less current, compared with other state-of-the-art frequency dividers (usually based on double-edge-triggering technique) used for QN suppression.

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