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Design and Implementation of Digital CMOS VLSI Circuits Using Dual Sub-Threshold Supply Voltages

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ABSTRACT
Power dissipation in high performance systems requires more expensive packaging. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field. As the density and operating speed of CMOS VLSI chip increases, power dissipation becomes more significant due to the leakage current when transistor is OFF. This can be observed in both combinational and sequential circuits. Static power reduction techniques are achieved by means of operating the transistor either in Cut-off or in Saturation region completely and by avoiding the clock in unnecessary circuits. In this work, "Dual sub-threshold voltage supply" technique is used to operate the transistor under either OFF or ON state by applying some voltage at the gate of the MOS transistor. The designed circuits are simulated by using Mentor Graphics Backend Tool. With this technique, nearly 10-75% of the power dissipation is reduced for designed circuits. Thereby, the performance of circuit can be increased.

Keywords- Digital circuits, Dual sub-threshold leakage current, Power dissipation, Performance.

I. Introduction

Low power design is the upcoming design technology due to its high performance battery-portable digital systems. Presently there are many portable devices that run on batteries like laptop, tablet PC, mobile phone, ipod, etc. The power dissipation in these devices is high. This is due to the supply of high voltage to the low power components in the device. If the supply power is low then the circuits operating with that power should be capable of holding the loads. For example, if an amplifier circuit is working with low input power then the output should be capable of driving a loud speaker. The complexity for the high speed devices is more. Thermal problems arise due to more hardware in a dense packing. For this there is a need for the cooling process. So, there is a need for heat sinks and cooling fans for heat exhaust. The dual sub-threshold supply voltage technique would help to operate where complex devices need to consume less power. Thereby, the complex circuits will dissipate less amount of power [1].

In this work, the circuits are designed and simulated in mentor graphics back-end tool through Linux operating system. This provides the better way to design the circuits from physical design and the circuits can be simulated easily as in the real time. The remaining sections of the paper as follows: section 1 is about different low power design techniques, design principles, power dissipation are given in section 2 and 3, implementation of the circuits are given in section 4 and finally results and conclusion are discussed.

1. Different low power design techniques

There are certain low power techniques that provide low power dissipation by using the low power design techniques. The different techniques used in low power design include [1] [2]:

i) Clock gating technique
ii) Multi-threshold CMOS (MTCMOS)
iii) Stacked Transistors
iv) Dynamic Threshold MOS (DTMOS)
v) Dynamic/voltage/frequency scaling
vi) Near sub-threshold supply
vii) Dual sub-threshold supply

In this work, among these techniques the dual sub-threshold supply voltage is used to minimize power dissipation. Therefore, by using multi threshold supply voltages that are provided with near sub-threshold voltage and the voltage can also be varied around below or near sub-threshold voltages. The dynamic power consumed by the transistors depends on the switching frequency of the signal that is applied at the gate of the transistor, full supply voltage and the load capacitance used.

Supply voltage scaling was developed for switching power reduction. It is an efficient method for reducing switching power. It also helps to reduce leakage power because the sub-threshold leakage is due to Gate Induced Drain Leakage (GIDL) and Drain Induced Barrier Leakage (DIBL) these are also reduced as well as the gate leakage component when the supply voltage is scaled down. Static supply voltage scaling is a multiple supply voltage where as different supply voltages are provided.

In order to satisfy the speed performance the critical and non-critical paths are made to operate with same speed without disturbing the system performance.

II. Design Principles

Transistors are designed in such a way that the width of the gate should be more when compared with the length of the channel this is made such that the for applied gate voltage the channel must be formed for logic high in NMOS and logic low in PMOS transistors. If the insulator used at the gate of the MOS transistor is of very less width than the channel length, hence if the transistor is OFF even though certain current flows due to charge induced due to capacitance effect. To reduce the leakage current the length and width of MOS transistor is made suitably for low voltage applications that to near sub-threshold voltages.

III. Power dissipation

Power dissipation is reduced by reducing the length of the channel and width of the gate of transistors [3]. This is the easy way to reduce the power consumption of a transistor without disturbing its operation. The low voltage operation is that the conduction of transistor due to diffusion of charge carriers. Transistors connected to low threshold supply voltage conduct as the channel will be formed for very low voltage. So that, even for a high threshold supply voltage the power dissipation by the transistors is less. The near sub-threshold supply voltage is sufficient for the transistors to conduct. Static power essentially consists of the power used when the transistor is not in the process of switching.

$$P_{static} = I_{static} * V_{dd} \quad (1)$$

The near threshold supply voltage is also provided in order to make the transistors to conduct if there are equal paths that there are no critical and non-critical paths. Thereby, the static power dissipation is reduced. Dynamic power is the sum of transient power consumption ($P_{transient}$) and capacitive load power consumption (P_{cap}). $P_{transient}$ represents the amount of power consumed when the device changes logic states. Capacitive load power consumption is the power used to charge the load capacitance.

$$P_{dynamic} = P_{cap} + P_{transient} = (C_L + C) * V_{dd}^2 * f * N^3 \quad (2)$$

Where 'N' is the number of logic values that are switching, 'f' is the switching frequency. The short circuit power depends upon the frequency of the transition. Hence the total power dissipated is the sum of all the power dissipations in the circuit.

$$P_{total} = P_{ststic} + P_{sc} + P_{dynamic} \quad (3)$$

The total power dissipated is the sum of static power dissipated, short circuit power and the dynamic power consumed by the circuit. A way to reduce leakage power consumption is to raise the V_{th} of some gates. A higher V_{th} reduces the sub-threshold leakage [4]. Hence, the transistors are designed in order to reduce the power dissipation to maximum level. The use of two power supplies makes some devices to allow the leakage current hence by providing a third power supply that is greater than the threshold supply voltage. This technique can be applied to any circuit either combinational or sequential circuit.

IV. Implementation

Any CMOS circuits can be designed by implementing the dual sub-threshold supply voltages along with Vdd [5-7]. The designed combinational circuits are decoder, 4x1 multiplexer and sequential circuits are Moore and ring counter. The logic gates are designed with CMOS transistors, the gates are designed as shown below. The inverter with V_{DD} as supply voltage is given in fig. 1.

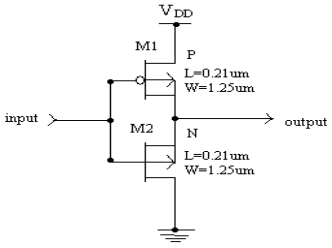

Fig. 1: Inverter with V_{DD} as supply voltage

In this circuit the input is applied to both transistors depending on the applied input logic the transistors conduct and the output is obtained. The inverter circuit uses very less number of transistors connected through the supply voltage to the ground. Hence very low voltage is sufficient to operate the inverter with very less power dissipation.

The NAND gate with V_{DD} as supply voltage is given in fig. 2. The circuit inputs are i1 and i2, depending on the input voltage applied transistors conduct and the output at O is obtained. The designed NAND gate uses supply voltage VDD, either Low or High V_{th}. Depending upon the voltage applied the NAND gate is operated with low leakage current and very low power dissipation.

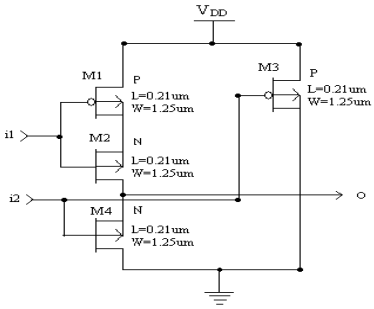

Fig. 2: NAND gate with V_{DD} as supply voltage

Fig. 3 gives the functionality of 4-input OR gate with V_{DD} as supply voltage. In this circuit, the inputs are i1, i2, i3, i4 and the output is O. The input is applied to the transistors as the input voltage is very low the transistors conduct. Depending upon the number of transistors used in the circuit the supply voltage is also varied, if there are a number of transistors connected in series the supply voltage is to

be increased in order to obtain the required output for the given input.

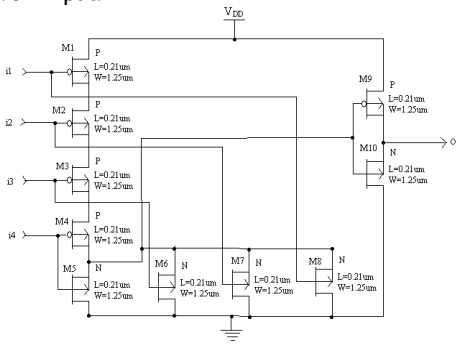

Fig. 3: 4-input OR gate with V_{DD} as supply voltage

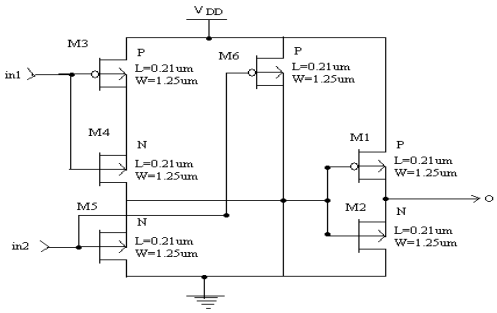

Fig. 4: 2-input AND gate with V_{DD} as supply voltage.

The 2-input AND gate with V_{DD} as supply voltage is given in fig. 4. In this circuit the inputs are in1 and in2. The output is O. Depending upon the applied logic the transistors conduct and the output is obtained. The AND gate designed with an inverter and the NAND gate, hence inverter requires very low power supply, NAND gate uses some high voltage than the inverter. Hence High Vth supply voltage is sufficient to drive the AND gate.

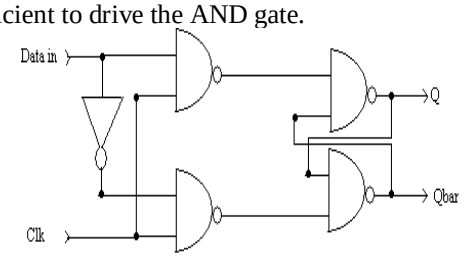

Fig. 5: D-Flip Flop

The D-Flip flop is given in fig. 5. In this circuit, the inputs are Data in and Clk. The outputs are Q and Qbar. The D-Flip flop requires high threshold supply voltage, in order to dissipate low power. Further, the designed circuits are discussed below.

The gate level diagram of 4x1 Multiplexer with dual sub-threshold supply voltage is given in fig. 6. The simulation waveform of 4x1 Multiplexer with dual sub-threshold supply voltage is given in fig. 7. In this simulation waveform, the inputs are i1, i2, i3, i4, s0 and s1 and output is out. In this s0, s1 are selection lines. The NOT gate can also be provided with low threshold supply voltage as the voltage drop in the NOT gate is very low, the AND gat uses more number of transistors so high Vth supply voltage can be provided and the OR gate that drives all the outputs from the AND gates require V_{DD} as power supply and also there are more number of transistors required for 4-input OR gate.

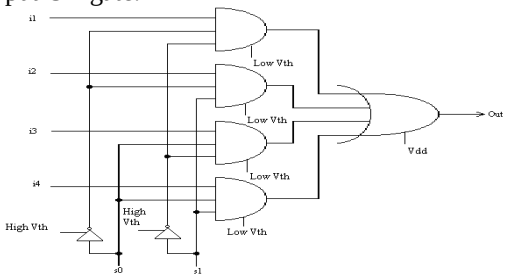

Fig. 6: 4x1 Multiplexer with dual sub-threshold supply voltage

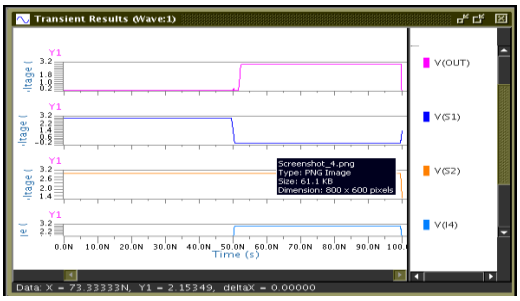

Fig. 7: Simulation waveform of 4x1 Multiplexer with dual sub-threshold supply voltage

The Differential cascode voltage switched (DCVS) level converter for NOT gate is shown in fig. 8 and its simulation waveform is given in fig. 9. In this circuit, the input is IN, output is OUT The DCVS circuit designed with NOT gates and few transistors so low threshold supply voltage is provided to the inner NOT gate and high threshold supply voltage is provided to the overall circuit and the output driven NOT gate.

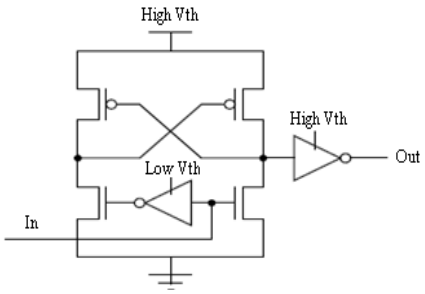

Fig. 8: Differential cascode voltage switched (DCVS) level converter for NOT gate

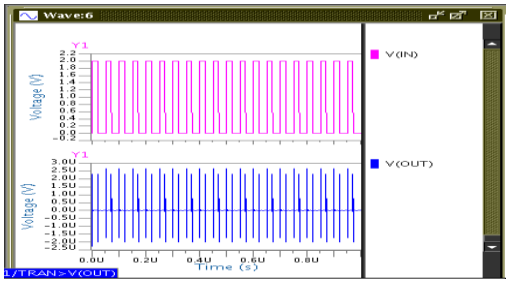

Fig. 9: Simulation waveform of DCVS level converter for NOT gate

The 2 × 4 Decoder with dual sub-threshold supply voltage and its simulation waveforms are given in figures 10 and 11 respectively.

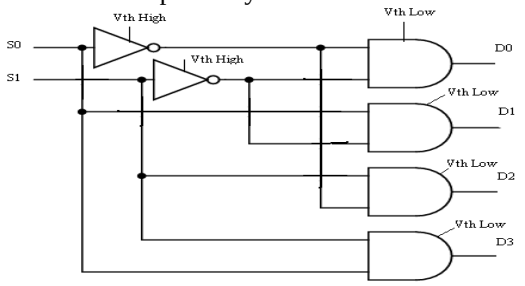

Fig. 10: 2×4 Decoder with dual sub-threshold supply voltage

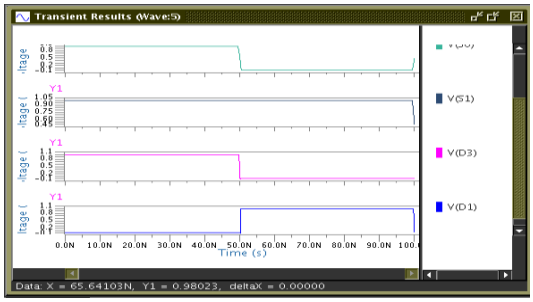

Fig. 11: Simulation waveform of 2×4 Decoder with dual sub-threshold supply voltage

The Moore Machine with dual sub-threshold supply voltage and its simulation waveform is given in figures 12 and 13 respectively.

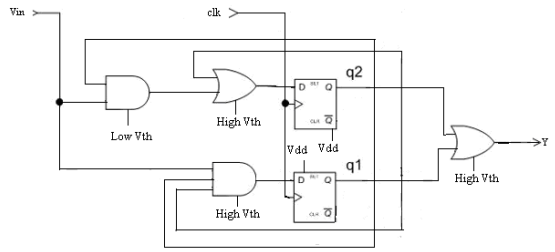

Fig. 12: Moore Machine with dual sub-threshold supply voltage

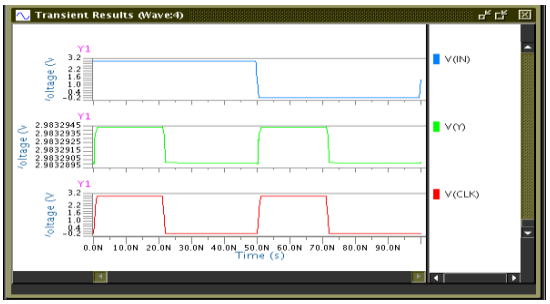

Fig. 13: Moore Machine with dual sub-threshold supply voltage

In the Moore machine the use of D flip flop is to provide some delay for the given input from the OR gate and AND gates the high V_{th} and V_{DD} can be altered (inter changed). The logic diagram of ring counter and its functionality with dual sub-threshold supply voltage is given in figures 14 and 15 respectively. The ring counter is a sequential circuit in which D flip flops are used as the memory elements. The inputs are clk and reset are provided to the D flip flop directly with supply voltage of low V_{th}, 4-input OR gate is supplied with high V_{th}.

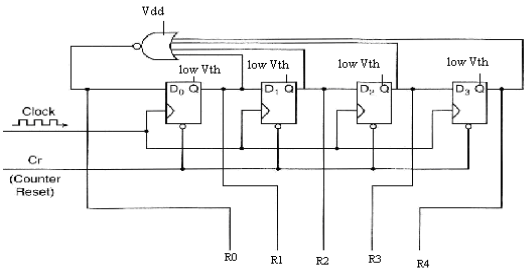

Fig. 14: Ring counter with dual sub-threshold supply voltage

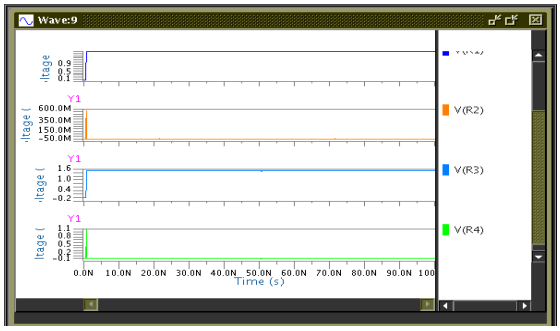

Fig. 15: Simulation waveform of Ring Counter with dual sub-threshold supply voltage

Power consumption varies from one circuit to another circuit, as it depends upon the supply voltage, load applied, type of components, the technique and technology used to design the circuit. The 1.25µm technology is used to implement these designed circuits. The power dissipation of circuits with sub-threshold supply voltages along with V_{DD} is given in Table 1. The results of power dissipation of circuits with dual sub-threshold supply voltages with out V_{DD} are given in Table 2.

Table 1. Power dissipation of circuits with dual sub-threshold supply voltages along with V_{DD}

Designed circuit	**Supply voltages (volts)**			**Power dissipation**
	V_{DD}	**V_{DD} high**	**V_{DD} low**	(watts)
DCVS for NOT gate	0.7	0.35	0.15	2.279µ
Nand	-----	-------	0.15	39.9354n
Inverter	-----	-------	0.15	25.9438f
2 to 4 Decoder	0.7	0.35	0.15	1.7851µ
4x1 Multiplexer	1.0	0.7	0.35	24.3857 µ
Moore	0.7	0.25	0.15	18.6552µ
Ring counter	1.5	-----	0.15	690.1097n

Table 2. Power dissipation of circuits with dual sub-threshold supply voltages with out V_{DD}

Designed circuit	**Supply voltages (volts)**		**Power dissipation**
	V_{th} low	**V_{th} high**	(watts)
DCVS for NOT gate	0.15	0.24	6.385 µ
Nand	0.15	0.24	244.0433n
Inverter	0.15	0.24	34.680n
2 to 4Decoder	0.15	0.24	5.417 µ
4x1 Multiplexer	0.15	0.24	40.1425 µ
Moore	0.15	0.24	20.9725 µ
Ring counter	0.15	0.24	800.6924n

V. Power Dissipation Comparison

The power dissipation by using the dual sub-threshold supply voltage is more this is because of the more leakage power and the output results are not accurate, when compared with the power dissipation using the dual sub-threshold supply voltage along with V_{DD} and the output is accurate. The Table 3 describes the percentage of power dissipation between dual sub-threshold supply voltage along with V_{DD} and dual sub-threshold supply voltage.

Table 3. Percentage reduction of power dissipation for dual sub-threshold supply voltage with and without supply voltage

Designed circuits	**Power dissipation (watts)**		**Power reduction (%)**
	without V_{DD}	**With V_{DD}**	
DCVS - NOT	6.385 µ	2.279µ	73.69
Nand	244.0433n	39.9354n	85.93
Inverter	34.680n	25.9438f	99.99
2 to 4 Decoder	5.417 µ	1.7851µ	75.21
4x1 Multiplexer	40.1425 µ	24.3857 µ	39.25
Moore	20.9725 µ	18.6552µ	12.15
Ring counter	800.6924n	690.1097n	13.81

VI. Conclusion

The power dissipation of designed digital circuits using dual sub-threshold supply voltage along with V_{DD} is less when compared to the dual sub-threshold supply voltage without V_{DD}. The power dissipation increases while increasing the V_{DD} supply voltage. Hence this technique provides a better solution for the low power devices. Therefore high supply voltages are restricted for these circuits. The power saving is nearly 10-70% better for dual sub-threshold supply voltage along with V_{DD} as supply voltages.

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