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Enhancement of Power Quality in Distribution System with Reduced DSTATCOM Voltage Rating

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ABSTRACT
In power distribution network, distribution static compensator (DSTATCOM) is used for enhancing power quality. This paper investigates the application of DSTATCOM with non-stiff source connected to distribution network to enhance power quality. The model discussed in this paper is designed to have reduced DC-link voltage rating without compromising compensation capability when non-linear loads are connected to distribution network. This model uses a series capacitor along with interfacing inductor and a shunt filter capacitor. Having this reduced DC-link voltage, the average switching frequency of insulated gate bipolar transistor (IGBT) switches of DSTATCOM reduces and thus reducing switching losses in inverter. Simulation studies are carried out using matlab/simulink and the results shown proves the performance of the system when non-linear loads are connected.
Keywords – DSTATCOM, DC-link voltage, non-linear loads, non-stiff source, power quality.

I. INTRODUCTION

The evolution of power electronic devices, nonlinear loads, and unbalanced loads has degraded the power quality in the power distribution network [1]. The distribution static compensator (DSTATCOM) is a shunt active filter, which injects currents into the point of common coupling (PCC) (the common point where load, source, and DSTATCOM are connected) such that the harmonic filtering, power factor correction, and load balancing can be achieved. In practice, the presence of feeder impedance and non-linear loads distorts the terminal voltage (PCC) and source currents. The load compensation using state feedback control of DSTATCOM with shunt filter capacitor gives better results [2]. The switching frequency components in the terminal voltages and source currents are eliminated by using state feedback control of shunt filter capacitor.

The voltage rating of dc-link capacitor decides the compensation performance of any active filter [3]. In general, the dc-link voltage has much higher value than the peak value of the line-to-neutral voltages. This is done in order to ensure a proper compensation at the peak of the source voltage. In [4], the authors discuss the limit of current distortion and loss of control limit, which states that the dc-link voltage should be greater than or equal to 6 times the phase voltage of the system for distortion-free compensation. When the dc-link voltage is less than this limit, there is insufficient resultant voltage to drive the currents through the inductances so as to track the reference currents. Reference value of the dc-bus capacitor voltage mainly depends upon the \ requirement of reactive power compensation of the active power filter [5]. The primary condition for reactive power compensation is that the magnitude of reference dc-bus capacitor voltage should be higher than the peak of source voltage at the PCC. Due to these criteria, many researchers have used a higher value of dc capacitor voltage based on their applications.

Having high value of dc-link capacitor, the voltage source inverter (VSI) becomes bulky and the switches used in the VSI also need to be rated for higher value of voltage and current which in turn, increases the entire cost and size of the VSI. Here in this paper, the detailed model with reduced dc-link voltage rating having non-linear loads (one with only three phase bridge diode rectifier and the other is increased non-linear load, i.e. three phase bridge diode rectifier driving BLDC) connected to distribution network.

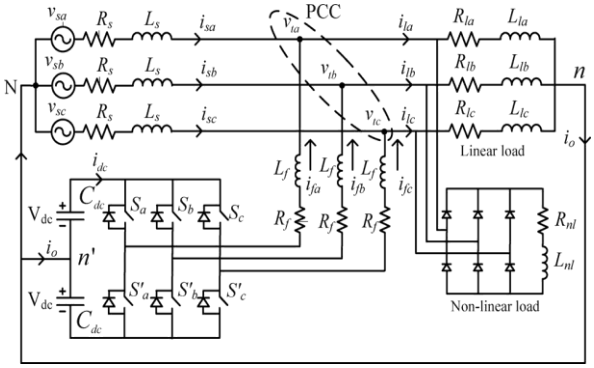


Fig.1: circuit of DSTATCOM having normal dc-link voltage

In this paper, DSTATCOM topology with reduced dc-link voltage is developed. The topology consists of two capacitors: one in series with the interfacing inductor of the active filter and the other is in shunt with the active filter. The series capacitor is used to reduce the dc-link voltage while simultaneously compensating the reactive power required by the load [6], so as to maintain unity power factor without compromising the performance of the DSTATCOM. The shunt capacitor, along with the state feedback control, maintains the terminal voltage to the desired value in the presence of feeder impedance and non-linear loads. The simulation studies are carried out using studies are carried out using matlab/simulink, and detailed results are presented in this paper.

II. CONVENTIONAL AND PROPOSED TOPOLOGIES OF DSTATCOM

In this section, the conventional and proposed topologies of the DSTATCOM are discussed in detail. Fig. 1 shows the power circuit of the neutral clamped VSI topology-based DSTATCOM which is considered the conventional topology in this study. In this figure, Vsa, Vsb, Vsc are source voltages of phases a, b, and c, respectively. Similarly, Vta, Vtb, Vtc are the terminal voltages at the PCC. The source currents in three phases are represented by i_{sa}, i_{sb} ,i_{sc} and load currents are represented by i_{la}, i_{lb}, i_{lc}. The shunt active filter currents are denoted by i_{fa}, i_{fb}, i_{fc} and i_o represents the current in the neutral leg. Ls and Rs represent the feeder inductance and resistance respectively. The interfacing inductance and resistance are represented by L_f and R_f respectively. The load constitutes both linear and nonlinear loads as shown in the figure. The dc-link capacitors and voltages across them are represented by $C_{dc1}=C_{dc2}=C_{dc}$ and $V_{dc1}=V_{dc2}=V_{dc}$ respectively.

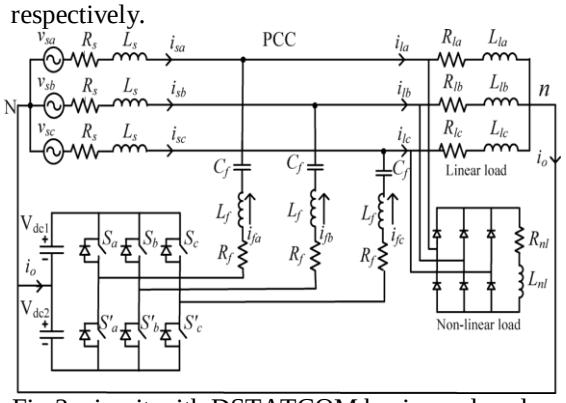


Fig.2: circuit with DSTATCOM having reduced dc-link voltage (hybrid filter)

Fig. 2 shows the circuit of the developed neutral clamped VSI topology-based DSTATCOM. It consists of conventional DSTATCOM model with a capacitor C_f in series with the interfacing shunt branch of the active filter and a capacitor C_{sh} in shunt with the active filter. This topology is referred to as hybrid topology in this study. The capacitor C_f has the ability to supply a part of the reactive power required by the load, and the active filter will compensate harmonics and the balance reactive power at the load. The addition of capacitor in series with the interfacing inductor in conventional topology will reduces the need of high dc-link voltage and results in reduced average switching frequency of the switches. The shunt capacitor C_{sh} eliminates the switching frequency components of the VSI in the terminal voltages and source currents using state feedback control. The series capacitor C_f and the shunt capacitor Csh design will have influence on the performance of the compensator (which is discussed later).

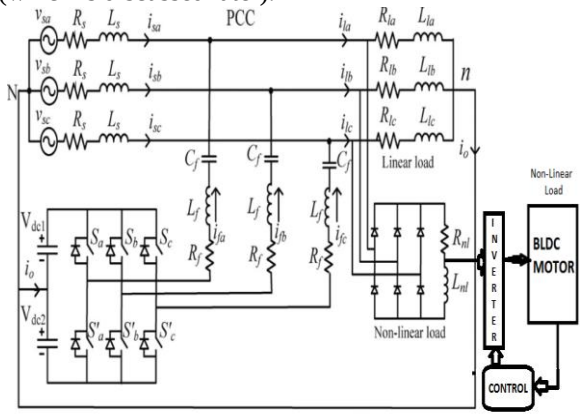


Fig.3 : circuit with DSTATCOM having reduced dc-link voltage and increased non-linear load

Also in this paper a new model was developed and simulated using the same parameters as in hybrid topology but by further increasing the non-linear load of the network by connecting a brushless DC motor (BLDC) which is shown in Fig.3. The model results prove that even when the reduced dc-link voltage is applied to DSTATCOM by further increasing the non-linear type of load connected to the distribution network, the performance of the network is appreciable.

III. DESIGN OF PARAMETERS

3.1 Design of VSI Parameters

Designing the parameters in VSI needs to be carefully for better performance of the system. The most important parameters that need to be taken into consideration while designing conventional VSI are dc-link voltage V_{dc}, dc storage capacitor C_{dc}, interfacing inductance L_f, and switching frequency f_{sw}. A detailed design procedure of VSI parameters is given based on the following equations, the parameters of the conventional VSI topology are chosen. The dc-link capacitor value is given by

$$C_{\mathrm{dc}} = \frac{(2X - X/2)nT}{(1.8V_m)^2 - (1.4V_m)^2} \qquad (1)$$

Where V_m is the peak value of the source voltage, X is the kVA rating of the system, n is the number of cycles, and T is the time period of each cycle. The interfacing inductance is given by

$$L_f = \frac{1.6V_m}{4hf_{\text{swmax}}} \quad (2)$$

where

$$h = \sqrt{\frac{k_1}{k_2}\frac{(2m^2-1)}{4m^2}f_{\text{swmax}}} \quad (3)$$

where k_1 and k_2 are proportionality constants, $f_{sw\ max}$ is maximum switching frequency of the switch, $f_{sw\ min}$ is the minimum switching frequency of the switch and *m* is given by

$$m = \frac{1}{\sqrt{1 - f_{\text{swmin}}/f_{\text{swmax}}}}. \quad (4)$$

Consider a three-phase system with 230-V line-to-neutral voltage. The hysteresis band is taken as 0.5 A. Using(1), C_{dc} is calculated as 3300 μF.

TABLE - 1 : System Parameters

System Quantities	Values
System Voltage	230V (line to neutral), 50Hz
Feeder Impedance	Z_s = 34+j3.141 Ω
Linear Load	Z_{la} = 34+j47.5 Ω, Z_{lb} = 81+j39.6 Ω, Z_{lc} = 31.5+j70.9 Ω
Non-Linear Load	Three-phase full bridge rectifier load feeding R-L load (of 150 Ω-300mH) driving BLDC Motor
VSI Parameters	C_{dc}=3300μF, V_{dcref}=1.6V_m=520V, L_f = 26mH, R_f = 0.1Ω
PI - Controller Gains	K_P = 2, K_i = 0.5
Hysteresis Band (h)	±0.5 A

From (2), the interfacing inductance L_f is computed to be 26 mH and the base KVA rating of the system is taken as 15 KVA. The system parameters are given in Table I for the conventional VSI topology.

3.2 Design of Shunt Capacitor C_{sh} for hybrid VSI

In the presence nonstiff source in the system, the terminal voltages are distorted due to unbalance and nonlinear load currents. These distorted voltages cannot be used to generate the reference quantities. In order to improve the performance of system, positive-sequence voltages at the terminal are transformed using the power-invariant instantaneous symmetrical transformation and are used for generating the reference currents. Still, the terminal voltages contains inverter switching frequency components. By providing a low impedance path using a filter capacitor C_{sh}, connected in shunt at the PCC in each phase as shown in Fig. 5, these switching frequency components might be nullified. If the filter capacitor resonates with the feeder reactance at frequency ω_r, then we get

$$C_{\text{shr}} = \frac{1}{\omega_r^2 L_s}. \quad (5)$$

3.3 Design of Series Capacitor C_f for hybrid VSI

The design of the C_f depends upon the value to which the dc-link voltage is reduced. In general, loads with only nonlinear components of currents are very rare, and most of the electrical loads are combination of the linear inductive and nonlinear loads. Under these conditions, the proposed hybrid topology will work efficiently. The design of the value of C_f is carried out at the maximum load current, i.e., with the minimum load impedance. If S_{max} is the maximum kva rating of a system and V_{base} is the base voltage of the system, then the minimum impedance in system is given as

$$Z_{\text{min}} = \frac{V_{\text{base}}^2}{S_{\text{max}}} = |R_l + jX_l| \ \text{(say)}. \quad (6)$$

In order to achieve the unity power factor, the shunt filter current needs to supply the sufficient load reactive current, i.e., the imaginary part of the filter current should be equal to the imaginary part of the load current. The filter current and load current in a particular phase are given as follows:

$$\boldsymbol{I}_{\text{filter}} = \frac{V_{\text{inv1}} - V_{t1}}{R_f + j(X_{lf} - X_{cf})} \quad (7)$$

$$\boldsymbol{I}_{\text{load}} = \frac{V_{t1}}{R_l + jX_l} \quad (8)$$

where $X_{lf} = 2\pi f L_f$, $X_l = 1/2\pi f C_f$ and f is supply frequency of fundamental voltage.

Neglecting the interfacing resistance and equating the imaginary parts of the above equations gives

$$\frac{V_{t1}X_l}{R_l^2 + X_l^2} = \frac{V_{\text{inv1}} - V_{t1}}{(X_{lf} - X_{cf})^2}(X_{lf} - X_{cf}) \quad (9)$$

where V_{inv1} and V_{t1} are the line-to-neutral rms voltage of the inverter and the PCC voltage at the fundamental frequency, respectively. The fundamental component of inverter voltage in terms of dc-link voltage is

$$V_{\text{inv1}} = \frac{0.612V_{\text{dc}}}{\sqrt{3}}. \quad (10)$$

Equations (11) and (12) give the Kirchhoff's voltage law along the filter branch for conventional topology and the proposed hybrid topology, respectively.

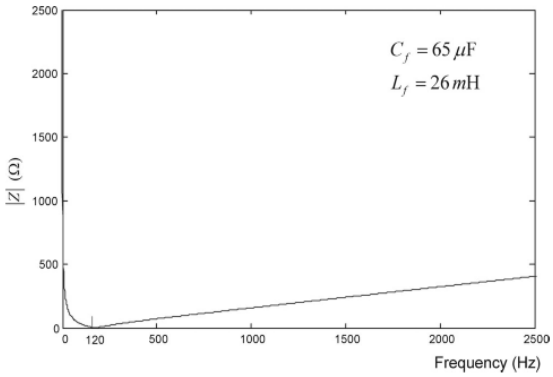


Fig.4 Frequency response of passive filter components of DSTATCOM

$$uV_{\rm dc} - v_t = L_f \frac{di_f}{dt} + R_f i_f \qquad (11)$$

$$\left(uV_{\rm dc} - \frac{1}{C_f}\int i_f dt\right) - v_t = L_f \frac{di_f}{dt} + R_f i_f$$

$$(uV_{\rm dc} - v_{cf}) - v_t = L_f \frac{di_f}{dt} + R_f i_f \qquad (12)$$

where u attains values of 1 or −1 depending on the switching of the inverter.

In (12), the fundamental voltage across the capacitor (V_{cf1}) adds to the inverter terminal voltage (uV_{dc}) when the load is inductive in nature. This is because, when the load is inductive in nature, the fundamental of the filter current lags the voltage at the PCC by 90^0 for reactive power compensation, and thus, the fundamental voltage across the capacitor again lags the fundamental filter current by 90^0. Finally, the fundamental voltage across the capacitor will be in phase opposition to the voltage at the PCC. Thus, the fundamental voltage across the capacitor adds to the inverter terminal voltage. This allows us to rate the dc-link voltage at lower value than conventional design. The designer may choose the value of dc-link voltage to be reduced, such that the LC filter in the active filter leg of each phase offers minimum impedance to the fundamental frequency component and higher impedance for switching frequency components.

From the system parameters mentioned in Table I, phase-a load impedance is chosen as Zmin and the dc-link voltage is chosen to be 300 V. Using (9), the value of the capacitor C_f is obtained to be 65 μF.

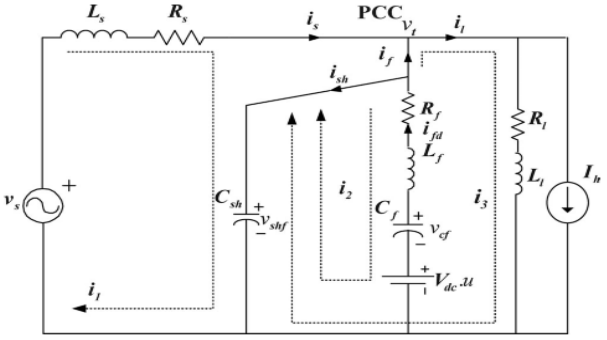


Fig.5 Single-line diagram of proposed DSTATCOM

dc-link voltage is chosen to be 300 V, such that the resultant capacitance along with the inductor forms an LC filter in the active filter branch, which provides minimum impedance at the lower order frequencies as shown in Fig. 4.

IV. STATE FEEDBACK CONTROL

The single-line diagram of the proposed DSTATCOM is shown in Fig. 5. To derive the state-space model of the system in Fig.5, we choose five local variables (i.e., three loop currents and two capacitor voltages). Now, the state vector is defined as follows:

$$x = [i_1 \quad i_2 \quad i_3 \quad v_t \quad v_{cf}]^t. \qquad (13)$$

The circuit shown in Fig.5 contains three forcing functions: the source voltage V_s, nonlinear load current I_h, and switching variable u. The u is replaced by the continuous time variables u_c and the control vector is defined as

$u = [u_c]$ (14)

The state-space equation of the circuit can be written as

$$\dot{x} = Ax + B_1 v_s + B_2 u + B_3 I_h \qquad (15)$$

where

$$A = \begin{bmatrix} -R_s/L_s & 0 & 0 & -1/L_s & 0 \\ 0 & -R_f/L_f & 0 & 1/L_f & -1/L_f \\ 0 & 0 & -R_l/L_l & 1/L_f & 0 \\ 1/C_{\rm sh} & -1/C_{\rm sh} & -1/C_{\rm sh} & 0 & 0 \\ 0 & 1/C_f & 0 & 0 & 0 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 1/L_s \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ -V_{\rm dc}/L_f \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad B_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ -1/C_f \\ 0 \end{bmatrix}$$

The state variables can be written as network parameters as follows

$$i_s = i_1; \quad i_{sh} = i_1 - i_2 - i_3; \quad i_l = i_3;$$

$$i_f = i_3 - i_1; \quad v_{cf} = v_{cf}; \quad v_{shf} = v_t. \qquad (16)$$

A transformed state vector z, which relates the state vector x with the network parameters using (16), can be written as

$$z = \begin{bmatrix} i_f \\ i_{sh} \\ i_l \\ v_t \\ v_{cf} \end{bmatrix} = \begin{bmatrix} -1 & 0 & 1 & 0 & 0 \\ 1 & -1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} x = Px. \qquad (17)$$

The state-space representation of the system given in (15) is transformed by using (17) as

$$\dot{z} = PAP^{-1}z + PB_1 v_s + PB_2 u + PB_3 I_h$$

$$= \Lambda z + \Gamma_1 v_s + \Gamma_2 u + \Gamma_3 I_h. \qquad (18)$$

Assuming that we have full control over u, the control law is defined as

$$u_c = -K(z - z_{\rm ref}) \qquad (19)$$

where Z_{ref} is the desired state vector. An optimization function can be developed to find the optimal feedback gains to maximize the left shift and increase the damping ratio of the eigenvalues of the state matrix given in (18). The optimization function is given as

$$\min f = \sum_{i=1}^{N} [\mathrm{Re}[\lambda_i(\Lambda_i - \Gamma_{1i}K)] - \xi_i(\Lambda_i - \Gamma_{1i}K)] \qquad (20)$$

subject to

$$K_{\min 1} < K_1 < K_{\max 1}, \quad K_{\min 2} < K_2 < K_{\max 2}.$$

Here K = [K_1 K_2 0 0 0] and N is the number of possible operating conditions. K is the feedback controller gain vector having two nonzero elements. It is not possible to find the reference of the load current, so partial feedback is considered. Similarly, the feedback for the terminal voltage v_t and series capacitor voltage V_{cf} are considered to be zero, as they are dependent on the other network parameters (i_f and i_{sh}).

V. INDUCTION OF COMPENSATOR CURRENTS UNDER DISTORTED AND UNBALANCED VOLTAGES

In this paper, the reference currents are generated by instantaneous symmetrical component theory [7] and are given as

$$i_{fa}^* = i_{la} - i_{sa}^* = i_{la} - \frac{v_{ta} + \gamma(v_{tb} - v_{tc})}{\Delta}(P_{\text{lavg}} + P_{\text{loss}})$$
$$i_{fb}^* = i_{lb} - i_{sb}^* = i_{lb} - \frac{v_{tb} + \gamma(v_{tc} - v_{ta})}{\Delta}(P_{\text{lavg}} + P_{\text{loss}})$$
$$i_{fc}^* = i_{lc} - i_{sc}^* = i_{la} - \frac{v_{tc} + \gamma(v_{ta} - v_{tb})}{\Delta}(P_{\text{lavg}} + P_{\text{loss}}) \quad (21)$$

where

$$\Delta = \sum_{j=a,b,c} v_{tj}^2, \gamma = \tan\varphi/\sqrt{3}.$$

The distorted and unbalanced load currents flow through the feeder impedance and make the voltage at PCC unbalanced and distorted. If the voltages are unbalanced and distorted, it is not possible to get balanced and sinusoidal currents after compensation using (21).

$$i_{fa}^* = i_{la} - i_{sa}^* = i_{la} - \frac{v_{ta1}^+ + \gamma(v_{tb1}^+ - v_{tc1}^+)}{\Delta_1^+}(P_{\text{lavg}} + P_{\text{loss}})$$
$$i_{fb}^* = i_{lb} - i_{sb}^* = i_{lb} - \frac{v_{tb1}^+ + \gamma(v_{tc1}^+ - v_{ta1}^+)}{\Delta_1^+}(P_{\text{lavg}} + P_{\text{loss}})$$
$$i_{fc}^* = i_{lc} - i_{sc}^* = i_{la} - \frac{v_{tc1}^+ + \gamma(v_{ta1}^+ - v_{tb1}^+)}{\Delta_1^+}(P_{\text{lavg}} + P_{\text{loss}}) \quad (22)$$

The switching commands are issued when limit (lim) exceeds tolerance band "±h". Unlike the predictive controllers, the hysteresis controller has the advantage of peak-current limiting capacity apart from in addition to other merits such as extremely good dynamic performance, simplicity in implementation, and independence from load variations. The disadvantage with this hysteresis method is that the converter switching frequency is highly dependent on the ac voltage and varies with voltage. The switching signals generated for the VSI are given by

$$u_c = -K(z - z_{\text{ref}})$$
$$u = \text{hys}(-K(z - z_{\text{ref}})). \quad (24)$$

If $h \geq lim$ then *hys(h)* = -1, *bottom switch is turned ON, whereas top switch is turned OFF* ($S_a = 0, S_a' = 1$).
If $h \leq lim$ then *hys(h)* = 1, *top switch is turned ON, whereas bottom switch is turned OFF* ($S_a = 1, S_a' = 0$).

The control circuit is simple for all topologies because only three switching commands are to be generated. These three signals along with the complementary signals will control all the switches of the inverter.

VI. SIMULATION RESULTS

In order to confirm the proposed topology, simulation is carried out using matlab/simulink. The same system parameters that are given in Table-I are used. The simulation results for the topologies are discussed and presented in this section.

The load currents and terminal (PCC) voltages before compensation are shown in Fig. 6. The load currents and terminal voltages are unbalanced and distorted. Fig.7 gives the simulation results of the DSTATCOM using the conventional VSI topology (having V_{dc}= 520V). The source currents after compensation are balanced and sinusoidal as shown in Fig. 7(a) but here currents still contain the switching frequency components. The three-phase compensating currents are shown in Fig. 7(b). The dc-link voltages across the top and bottom dc-link capacitors are shown in Fig. 7(c); using PI controller, the voltage across both capacitors are maintained constant to the reference value of 520 V as shown in the figure. The voltage across the interfacing inductor in phase-a is shown in Fig. 7(d). The peak-to-peak voltage across the inductor is 820 V. The terminal voltages contain the switching frequency components of the inverter and are shown in Fig. 7(e).

Fig. 8 and Fig. 9 gives the simulation results with the proposed hybrid topology with three phase full bridge rectifier as load and the same three phase full bridge rectifier driving brushless DC motor (BLDC) respectively. The value of the capacitor C_f in the active filter branch is chosen to be 65 µF and the reference dc-link voltage is 300 V for each capacitor. The shunt capacitor C_{sh} is taken as 50 µF. The voltage across the capacitor in phase-a (V_{cfa})) is shown in Fig. 10.

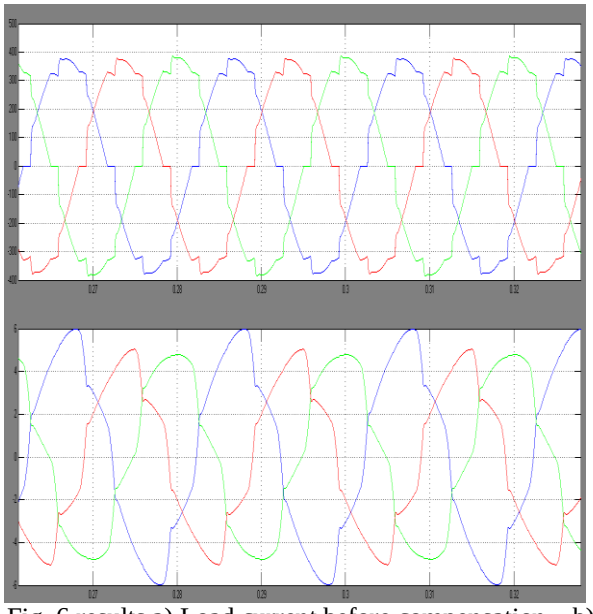


Fig. 6 results a) Load current before compensation, b) Terminal voltages before compensation.

Fig.10 also shows the phase-a terminal voltage V_{ta} and the voltage across top dc storage capacitor V_{dc1}.From the figure, it is clear that the voltage across the capacitor is in phase opposition to the terminal voltage. According to (12), the voltage across the capacitor eventually adds to the dc-link voltage and injects the required compensation currents into the PCC. The reason beyond showing phase-a capacitor voltage is that the design of the reference dc-link voltage is based on phase-a filter current, which has the maximum filter current among the three phases. The source currents after compensation using proposed topology with only converter as load and both converter and BLDC as non-linear loads are shown in Fig. 8(a) and Fig. 9(a) respectively. The compensator currents are displayed in Fig. 8(b) and Fig. 9(b) which are identical to the currents using the conventional topology. The dc-link voltages across the top and bottom dc-link capacitors are shown in Fig. 8(c) and 9(c). The voltage across the inductor is shown in Fig. 8(d) and 9(d). Here the peak-to-peak voltage is 630 V, which is far lower than the voltage across the inductor using the conventional topology.

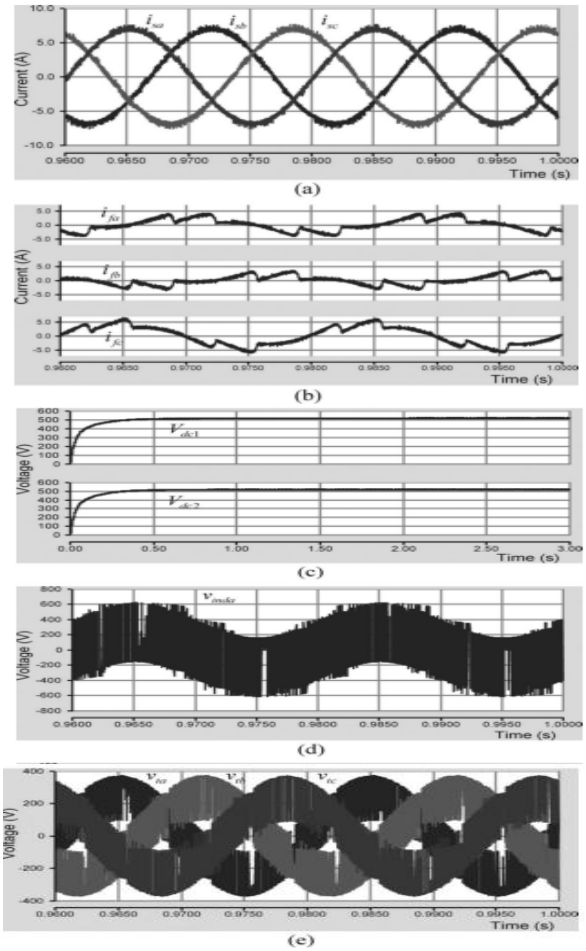


Fig. 7. Simulation results using conventional topology (having V_{dc} = 520V). (a) Source currents after compensation. (b) Filter currents. (c) DC capacitor voltages (top and bottom). (d) Voltage across the interfacing inductor in phase-a. (e) Terminal voltages after compensation.

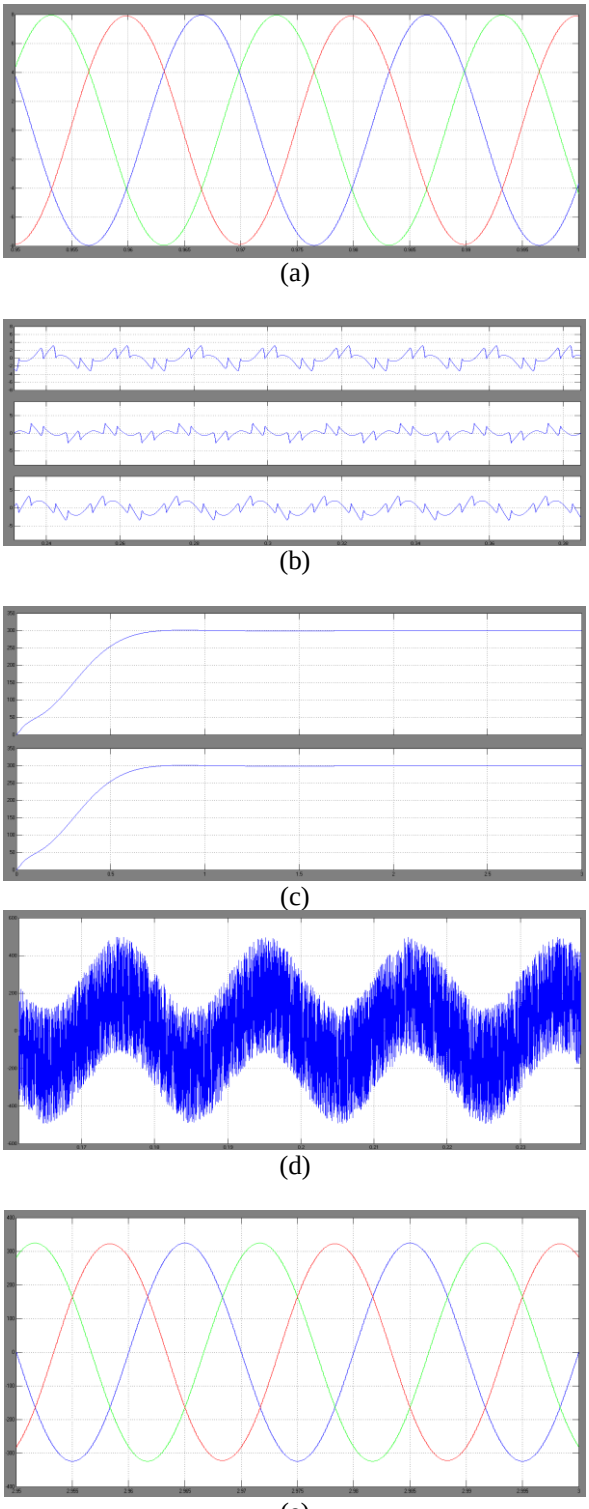
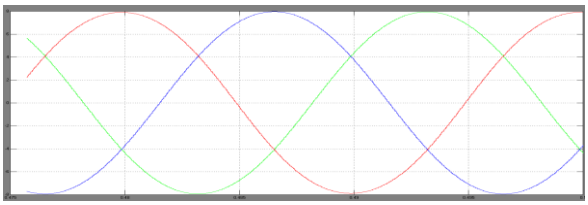
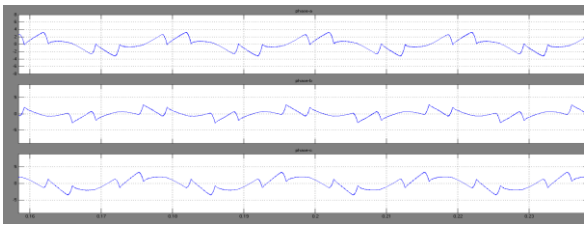


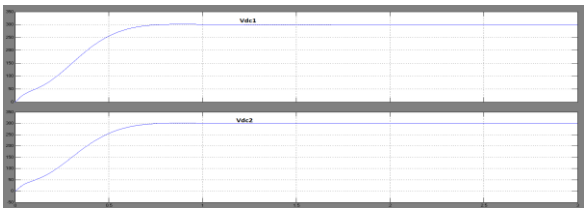
Fig. 8. Simulation results using proposed hybrid topology(V_{dc}=300V) with only 3-Ø bridge converter as load. (a) Source currents after compensation . (b) Filter currents. (c) DC capacitor voltages (top and bottom). (d) Voltage across the interfacing inductor in phase-a. (e) Terminal voltages after compensation.



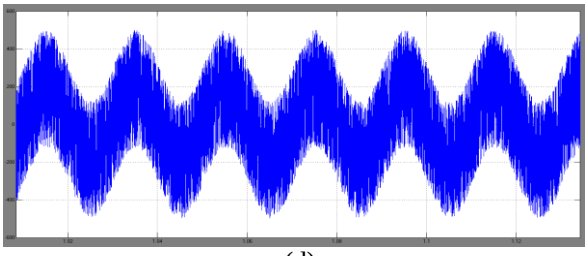
(a)



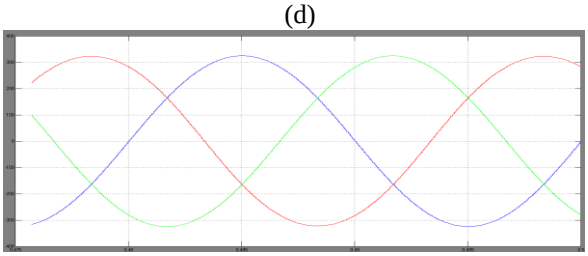
(b)



(c)



(d)



(e)

Fig. 9. Simulation results using proposed hybrid topology (V_{dc} = 300V) with only 3-Ø bridge converter driving BLDC motor as load. (a) Source currents after compensation. (b) Filter currents. (c) DC capacitor voltages (top and bottom). (d) Voltage across the interfacing inductor in phase-a. (e) Terminal voltages after compensation

When the voltage across the inductor is high in case of the conventional topology, the rate of rise of filter current di_f / dt will be higher than that of the proposed topology. This will allow the filter current to hit the hysteresis boundaries at a faster rate and increases the switching, whereas in proposed hybrid topology, the number of switchings will be less.

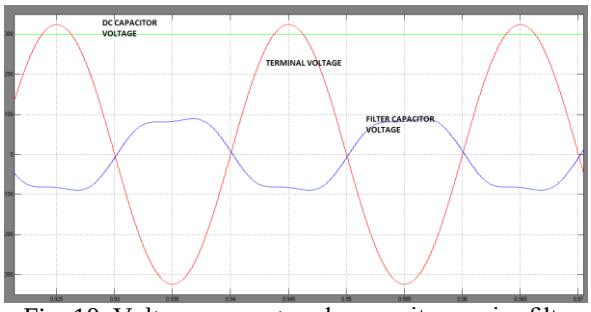


Fig. 10. Voltage across top dc capacitor, series filter capacitor, and terminal voltage in phase-a.

TABLE-II THD of Source Currents and Terminal Voltages for Different Topologies

THD %	Source Current	Terminal Voltage
Without DSTATCOM	11.1%	7.3%
DSTATCOM (reduced DC-link voltage) with Bridge Rectifier	0.7%	0.4%
DSTATCOM (reduced DC-link voltage) with Bridge Rectifier and BLDC	0.7%	0.4%

Since the voltage is reduced, the average switching frequency of the switches in the proposed hybrid topology will be less as compared to the conventional topology which in-turn reduces the switching losses. One more advantage of having less voltage across the inductor is that the hysteresis band violation will be less. This will improve the quality of compensation and total harmonic distortion (THD) will be less. The terminal voltages after compensations are shown in Fig. 8(e) and Fig. 9(e) which are free from the switching frequency components of the inverter. These switching frequency components are absorbed by the shunt capacitor by using state feedback control. The shunt capacitor provides a low impedance path at the high switching frequency. The THD of the source currents and terminal voltages before and after compensation in all the three phases are given in Table-II. This clearly shows the proposed hybrid topology performance is better than the conventional topology with a less dc-link voltage, reduction in switching operation, and regular tracking of reference compensator currents.

VII. CONCLUSION

A new hybrid DSTATCOM with reduced dc-link voltage has been discussed in detail which has the ability to compensate the load improving power quality of distribution system. Design of various parameters and control theories involved in this study were explained. Discussed topology was validated through simulation results in 3-Ø distribution system with neutral clamped DSTATCOM topology even when the non-linear loads are increased. Enlarged comparative discussion was given for different topologies. We can conclude that even with increased non-linear type of loads, this topology effectively reduces THD in source currents and terminal voltages.

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