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A Noble Design of Energy Recovery Flip-Flops

Mashkoor Alam[1] and Rajendra Prasad[2]
[1, 2] *Department of Electronics & Telecommunication Engineering, KIIT University Bhubaneswar*

Abstract
The power consumption of the clock tree dominates over 40% of the total power in high performance VLSI designs. Hence, low power clocking schemes are promising approaches for low power design. We propose energy recovery clocked flip-flops that enable energy recovery from the clock network, resulting in significant energy savings. These flip-flops operate with a single-phase sinusoidal clock which can be generating with high efficiency. In Cadence 180nm CMOS technology, we implemented these energy recovery clocked flip flops through an H tree clock network driven by a resonant clock generator to generate a sinusoidal clock. The proposed flip-flops exhibit more than 80% delay reduction, 47% power reduction, as compared to the conventional energy recovery flip-flop. Simulation results show a power reduction of 90% on the clock tree and total power saving of up to 80% as compared to the conventional square wave clocking schemes and flip flops. In this paper, we also propose clock gating solution for the energy recovery clocked flip flops reduces their power and delay. A pipelined array multiplier is designed which show a total power savings of 25%-69% as compared to the same multiplier using conventional square wave clocking scheme and corresponding flip-flops.

I. Introduction

Flip flops are ubiquitous element in CMOS circuits based designs which make the major portion of the synchronous circuits. As results, the structure of flip flop used in circuits has a large impact on system power consumption. However, the type of flip flop used to determines the amount of clock load, which directly affects dynamic power consumption Pdyn of circuits.

Thus, it is prudent to come up with techniques to reduce the power consumption of flip flops to reduce the overall system power consumption [2]. Also the power dissipated in clock distribution network is 30% to 60% of the total system power. As the power budget of today's portable digital circuit is severely limited, it is important to reduce the power dissipation in the flip flop.

Timing elements, latches and flip-flops, are critical for the performance of digital systems because of the tight timing constraints and requirements of low power [3]. Short set up time and hold time are also required for performance, but often overlooked. In a complex system it is very often necessary to have the ability to scan the data in and out during the test and diagnostic process.

Energy recovery is a technique for low power digital circuits [6]. Energy recover circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on the capacitors by using an oscillating supply voltage. In this paper, we apply energy recovery techniques to the clock network since the clock signal is most capacitive signal. The proposed energy recovery clocking scheme recycles the energy from the capacitance in each cycle of the clock. For an efficient clock generation, we use a sinusoidal clock signal.

In this paper, we proposed high performance and low power energy recovery flip flop that operate with a single phase sinusoidal clock. The proposed flip flops reduction in delay and power as compared to the conventional four phase transmission gate energy recovery flip flop. The energy recovery clocked flip flops are clocked through an H-tree clocking network. A resonant clock generator circuit was designed to generate a sinusoidal clock and drive the clock network and flip flops. We implemented the same clock tree using square wave clocked flip- flops.

Clock gating is another popular technique for reducing clock power [7]. Even though energy recovery clocking results in substantial reduction in clock power, there still remains some energy loss on the clock network due to resistance of the clock network and the energy loss in the oscillator itself due to non adiabatic switching. In this paper, we propose clock gating solutions for the energy recovery clock. We modify the design of the existing energy recovery clocked flip-flops to incorporate a power saving feature that eliminates any energy loss on the internal clock and other nodes of the flip flops. Applying the proposed clock gating technique to the flip-flips reduces their power by a substantial amount 1000 times during the sleep mode. However, the added feature has negligible power and delay overhead when flip-flops are in the active mode.

For high performance is increase the clock frequency with the technology scaling. But in deep sub micrometer generation's higher performance is obtained by parallelism in the architecture level [4]. Deeply pipelined systems exhibit inherent parallelism that requires higher fan out at the register outputs.

These impacts the requirements for higher flip flops driving strengths. The impact of the clock skew on the minimum cycle time increases in deep sub micrometer designs as the clock skew does not follow the technology scaling. Thus the ability to absorb the clock skew without impact on setup time becomes important. The amount of cycle time taken out by the flip flop consists of the sum of setup time and clock to output delay [5]. Therefore, the true measure of the flip flop delay is the time between the latest point of data arrival and corresponding output transition.

The remainder of this paper is organized as follows. In section 2, include system integration the energy recovery clock generation and clock-tree implementation. In section 3, the proposed energy recovery clocked flip-flops are described. In section 4, extensive simulation results of individual flip-flops and their comparisons are presented. In section 5, the clock gating approaches are proposed for energy recovery clocked flip-flops. In section 6, includes the design of an energy recovery clocked pipelined multiplier. Finally, the conclusion of this paper in section 7.

II. Energy Recovery Clock Generator

The energy recovery clock generator is a single phase resonant clock generator as shown in figure 1. Transistor M1 receives a reference pulse to pull-down the clock signal to ground when clock reaches its minimum, thereby maintaining the oscillation of the resonant circuit. This transistor is large transistor, and driven by a chain of progressively sized inverters. The oscillation frequency of this resonant clock is determined by

$$f = \frac{1}{2\pi\sqrt{LC}} \quad \text{..... 1}$$

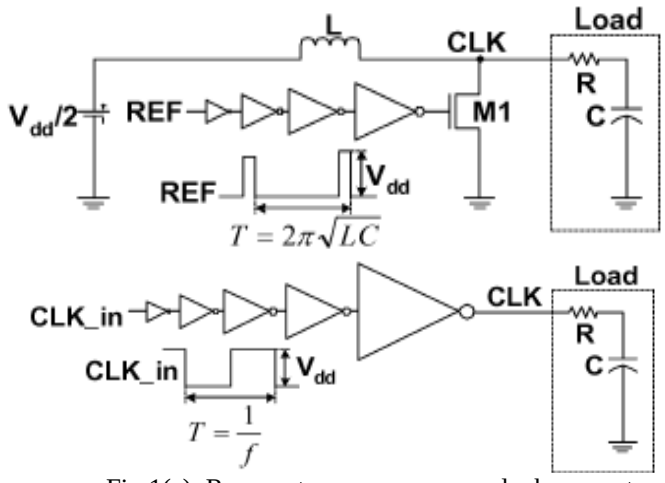

Fig 1(a): Resonant energy recovery clock generator
(b) Non-energy recovery clock driver

Where C is the total capacitance connected to the clock tree including parasitic capacitances of the clock tree and gate capacitances with clock inputs of flip flops. The frequency of reference signal is same as the oscillation frequency of the resonant circuit. Find the value of C. first with a given L and with the REF signal at zero, the whole system, including the flip flops are simulated. The clock signal shows a decaying oscillating waveform settling down to $V_{dd}/2$. From this waveform, the natural decaying frequencies are measured, and then by using equation 1, the value of C is calculated. The system consisting of the energy recovery clock generator, and flip flops are simulated at the frequency of 250 MHz with different data switching activities.

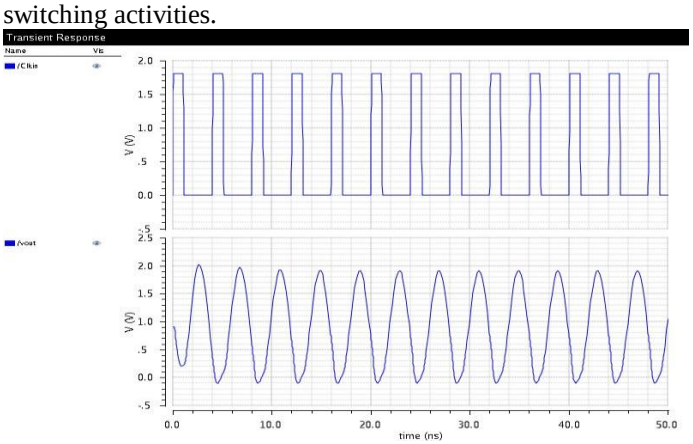

Fig. 2 Output Waveform of Energy Recovery Clock Generator

III. Energy Recovery Flip-Flops and Proposed Energy Recovery Flip-Flops

3.1 Differential Conditional Capturing Energy Recovery Flip-Flops

Differential amplifier circuits accept small input small signals are amplify them to generate small rail to rail swings [8]. They are used extensively in memory core and in low swing bus drivers to either improve performance or reduce power dissipation.

The energy recovery clock is applied to a minimum sized inverter skewed for fast high to low transition. Such skewing creates a sharp high to low transition on CLKB to ensure correct timing for the flip flop operation. The minimum sizing of inverter reduces its short circuit power caused by slow rising of the input clock. The clock signals CLK and inverter output CLKB is applied to transistors MN1 and MN2. The series combination of these transistors conduct for a short period of time during the rising transition of the clock when both the CLK and CLKB signals have voltage above the threshold voltage of the NMOS transistors. Since the clock inverter is skewed for fast high to low transitions, the conducting period occurs only during the rising transitions of the clock, but not on the falling transition. In this way, conducting pulse is generated during the rising transition of the clock. A cascade of three inverters instead of one can give a slightly sharper falling edge for the inverted clock CLKB. However, due to slow rising nature of energy recovery clock, enough delay can be generated by a single inverter.

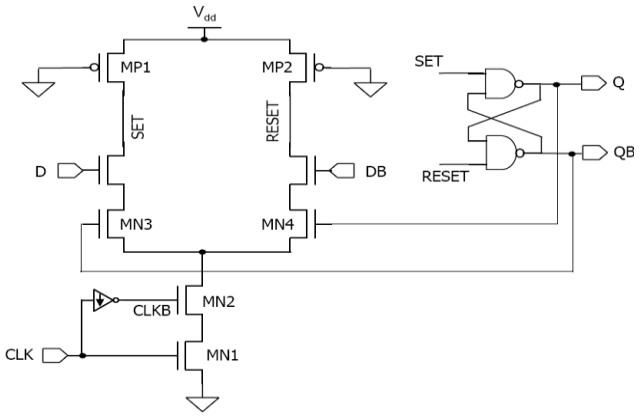

Fig.3 Differential Conditional Capturing Energy Recovery Flip Flop

The above figure 3 show the Differential Conditional Capturing Energy Recovery flip flops. It is a dynamic flip flop because it operates in a precharge and evaluate phase occurs. However, instead of using the clock for precharging, small pull-up PMOS transistors MP1 and MP2 are used for charging the precharge nodes. The DCCER flip flop uses a NAND based SET or RESET latch for the storage mechanism. The conditional capturing is implemented by using feedback from the output to the control NMOS transistors MN3 and MN4 in the evaluation paths. Therefore, if the state of the input data D and DB is same as that of the output Q and QB, both left and right evaluation paths are turned off preventing SET and RESET from being discharged. This results in power saving at low data switching activities when input data remains idle for more than one clock cycle.

3.2 Proposed Work of Differential Energy Recovery Flip-Flops

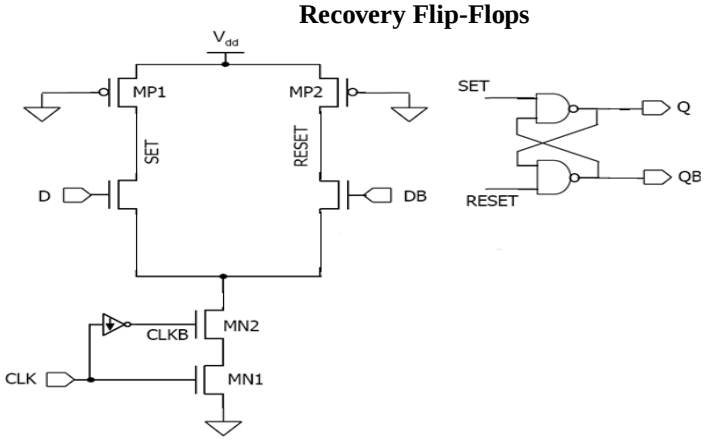

Fig.4 Proposed Differential Conditional Capturing Energy Recovery Flip Flop

The above figure 4 shows my proposed Differential Conditional Capturing Energy Recovery Flip Flop. This is also dynamic flip flop. The Transistors MN3 and MN4 are removed. This flips flop uses also a NAND based SET or RESET latch for mechanism. Therefore, the input of data D and DB are same as that of the output Q and QB. This results in power saving at low data switching activities when input data remains idle for more than one clock cycle. The size of DCCER flip flop is smaller and faster than previous DCCER flip flop.

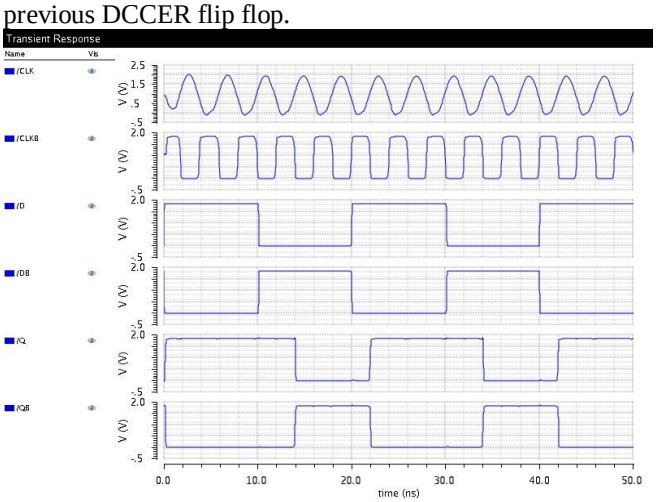

Fig.5 The output Waveform of DCCER Flip Flop

As can be seen in waveform of DCCER flip flop and proposed DCCER flip flop, CLK signal is generally less than $V_{dd}/2$ during a significant part of the conducting window. Therefore, a large transistor is used for MN1. However, since there are four stacked transistors in the evaluation path, significant charge sharing may occur when three of them become ON simultaneously. Sized pull up PMOS transistors MP1 and MP2 instead of clock controlled precharge transistors ensures a constant path to V_{dd} which helps to reduce the effect of charge sharing. Another property of the circuit that helps reduce charge sharing is that clock transistor MN1, which is largest the transistor in the evaluation path, is placed at the bottom of the stack. Therefore, the diffusion capacitance of the source terminal of MN1 is grounded and does not contribute to the charge sharing.

3.2 Single Ended Conditional Capturing Energy Recovery Flip-Flops

The above figure 6 shows a Single Ended Conditional Capturing Energy Recovery flip flop. SCCER is a single ended version of the DCCER flip flop. The transistor MN3 controlled by the output QB, provides conditional capturing. The right hand side evaluation path is static and does not require conditional capturing. Placing MN3 above MN4 in the stack reduces the charge sharing.

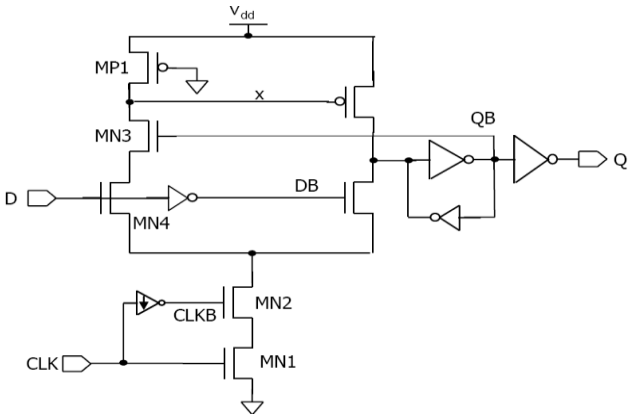

Fig.6 Single Ended Conditional Capturing Energy Recovery Flip Flop

3.4 Proposed Work of Single Ended Conditional Capturing Energy Recovery Flip-Flops

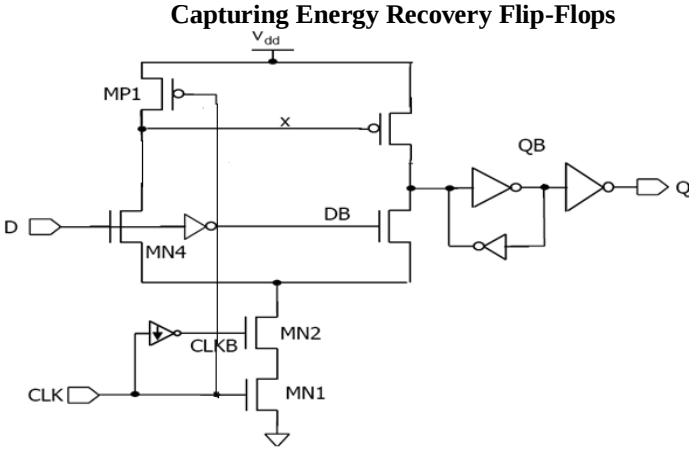

Fig. 7 Proposed of Single Ended Conditional Capturing Energy Recovery Flip Flop

The above figure 7 shows my proposed Single Ended Conditional Capturing Energy Recovery Flip Flop. The PMOS MP1 is directly connected to the energy recovery clock signal and Transistor MN3 is removed. When the clock voltage exceeds the threshold voltage of the clock transistor MN1 evaluation occurs. At the onset of the evaluation, the difference between the data inputs D and DB results in an initial small voltage difference is then amplified by the cross coupled inverter. When the clock voltage fall below V_{dd}-V_{tp}, then PMOS transistor MP1 are precharge. Therefore, if the state of the input data D and DB are same as that of the output Q and QB. The energy is recovered from the clock input capacitance of transistor MN1 and MP1 by applying a sinusoidal clock generated using a resonant clock generator. These results in the power saving at low data switching activities when input data remain idle for more than one clock cycle.

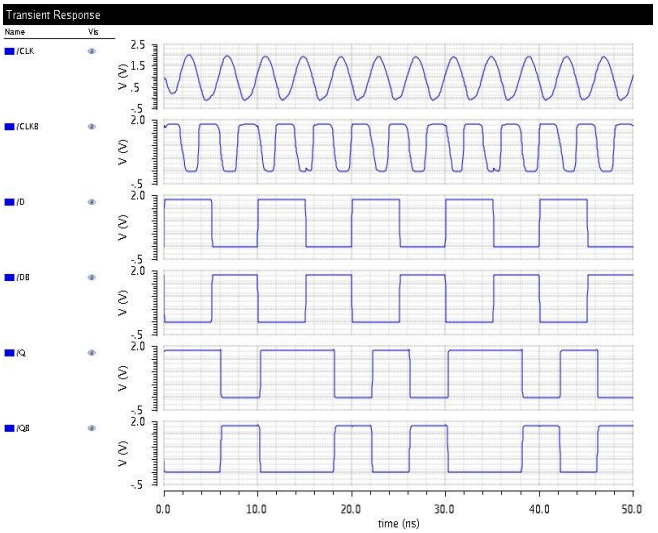

Fig. 8 the waveform of Single Ended Conditional Capturing Energy Recovery Flip Flop

IV. Simulation Results and Comparisions

All the flip flops are simulated using 180nm process technology with a supply voltage of 1.8V in Cadence Virtuoso tool. Netlists were extracted from schematic and simulated using ADEL. However, since the FPTG flip-flop is a dual-edge triggered flip-flop, it was designed to operate at a clock frequency of 250MHz. Figure 9 illustrates our timing definition. Delay is measured between 50% points of signal transitions. Setup time is a time from when data becomes stable to the rising transition of the clock. Hold time is the time from the rising transition of the clock to the earliest time that data may change after being sampled.

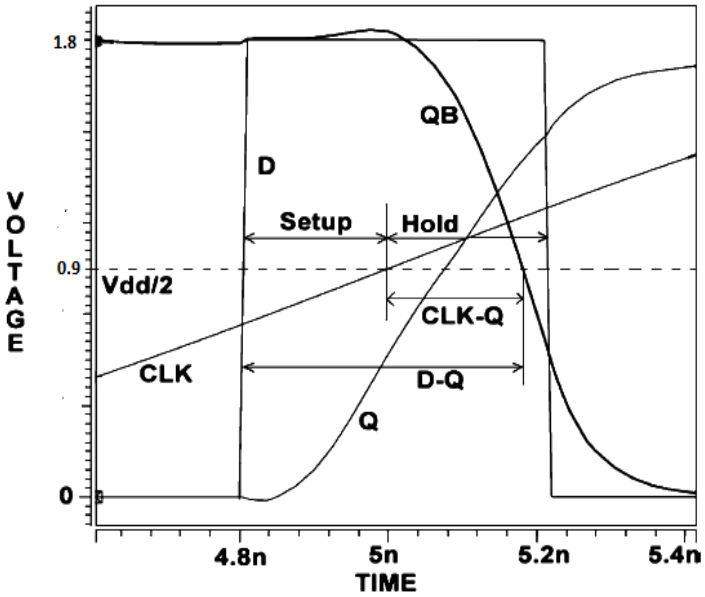

Fig. 9 Waveform of trimming definition

Table1. Summary of Numerical Results of Flip-Flops with 250 MHz Sinusoidal Clock

Flip Flop	D-Q delay(ps)	Setup Time(ps)	Hold Time(ps)	Clk-Q delay(ps)	Power (µW)	PDP* (fJ)	No. of Transistor	Area (μm^2)
FPTG	2350	-130	830	2470	455.7	1070.9	16	236.7
DCCER	405	143	175	190	225.5	91.33	18	150
Proposed DCCER	390	125	160	176.3	209.8	81.82	16	136.9
SCCER	325	280	45	150.4	185.5	60.29	17	210.5
Proposed SCCER	310	255	15	123.5	160.7	49.81	16	196.8

* Power is for long setup time; Power Delay Product (PDP) is the product of Power and D-Q delay

Table2. Summary of Power Consumption of Flip-Flops with different Input

Flip Flop	Square Wave Clock Power (µW)	Energy Recovery Clock Power (µW)	Percentage of Power Reduction
DCCER	415.7	225.5	45.75
Proposed DCCER	395.6	209.8	46.96
SCCER	359.5	185.5	48.4
Proposed SCCER	315.7	160.7	49.0

The proposed flip flops are compared with previous flip flop. For individual flip flop simulations, an ideal sinusoidal clock are used. It is apparent that the delays of the FPTG flip-flop are much larger as compared to the proposed flip-flops. The energy recovery clock shows the lowest power with all flip flops compared to square wave and sine wave clock. In order to compared with the square wave clocking.

The energy recovery systems show less power consumption as compared to the square wave clocking. The energy recovery clocking scheme reduces the power due to the clock distribution by more than 90% compared to non energy recovery clocking.

Table 3 Power Dissipated on Clock Tree

Flip-Flops	Clock Tree Power (mW)	Clock Tree Capacitor (pF)	Clock Power/ Load (mW/pF)	Percentage of Energy Recovery
FPTG	52.51	42.01	1.25	0
DCCER	3.096	46.83	0.066	94.7
Proposed DCCER	2.976	45.97	0.065	94.3
SCCER	2.894	44.68	0.065	94.8
Proposed SCCER	2.763	43.57	0.064	94.7

The numerical results of the power dissipated on the clock tree in each system and the percentage of energy recovered from the clock network of the energy recovery clocked flip-flops. The clock tree capacitance shown includes the wiring capacitance of the clock network and gate capacitance shown by the flip-flop clock inputs.

V. Energy Recovery Clock Gating Technique

The clock power in idle periods can be reduced by the application of clock gating technique to the energy recovery clock. In this section, we propose technique for applying clock gating to the energy recovery clocking system in order to obtained additional power savings in the idle mode The energy recovery clocked flip flops cannot save power during sleep mode if the clock is still running. There are two components of power dissipation inside flip flops: internal clock circuit power (power of logic gates connected to the clock) and the remaining circuit power (power of the rest of the flip flop circuit). We separated the clock circuit power from the remaining circuit power in our power measurements. Disabling the clock circuit in the idle state can eliminate both the clock circuit and remaining circuit power. Hence, disabling of the inverter gates is the proposed approach to implementing clock gating inside energy recovery clocked flip flop. This can be done by replacing the inverter gate with a NOR gate as shown in fig.10.

The NOR gate has two inputs: the clock signal and the enable signal. In active mode, the enable signal is low so the NOR gate behaves just like an inverter and flip flop operates just like the original flip flop. In the idle state, the enable signal is set to high which disables the internal clock by setting the output of the NOR gate to be zero. Figure 10 shows the circuit diagram and its output waveform.

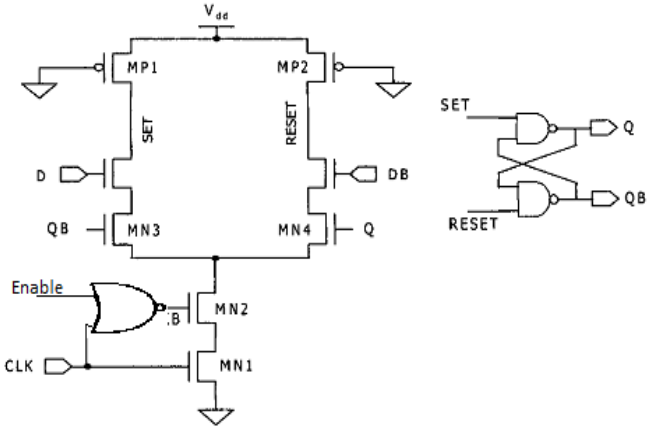

Fig.10 Clock Gating DCCER Flip Flop

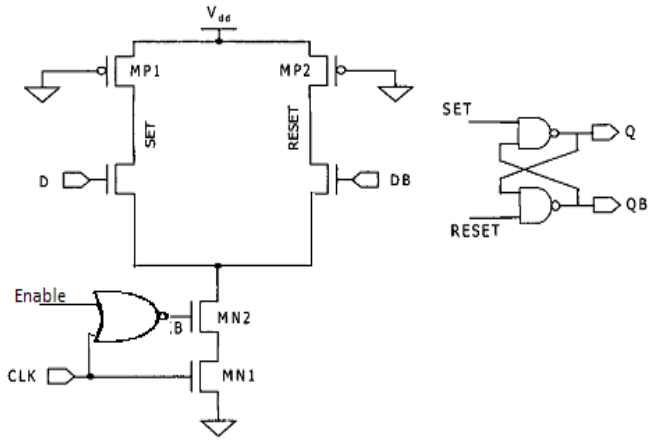

Fig.11 Proposed Clock Gating DCCER Flip Flop

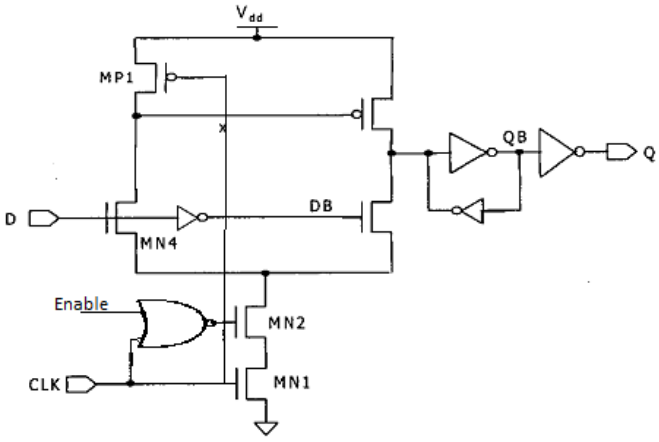

Fig. 14 Clock Gating of Proposed SCCER Flip Flop

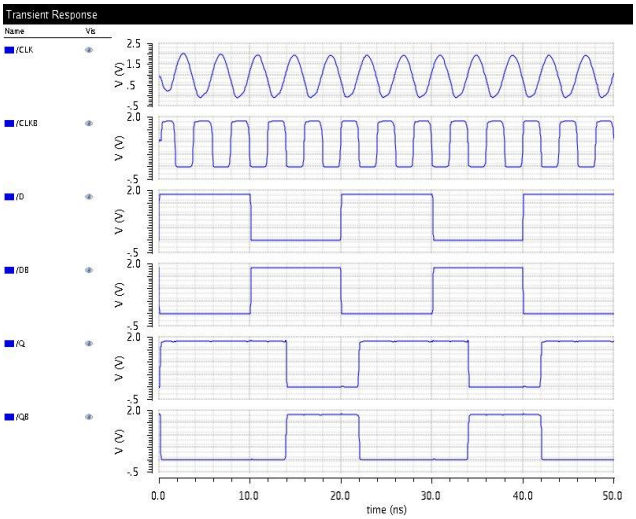

Fig.12 Waveform of Clock Gating Flip-Flops

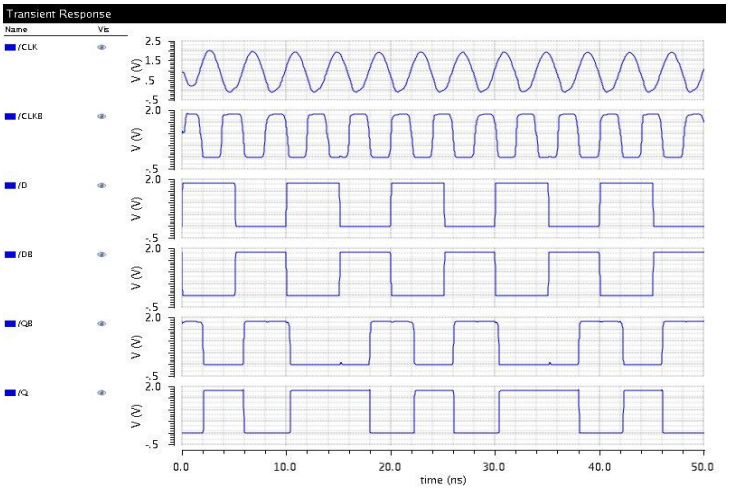

Fig. 15 Waveform of Clock Gating Flip Flop

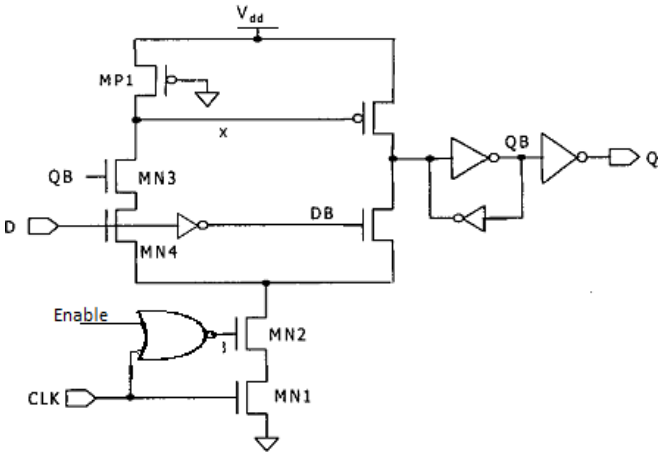

Fig. 13 Clock Gating of SCCER Flip Flop

Table4. Power Consumed by Flip Flop with Active Mode

	Original Flip Flop in Active Mode			Flip Flop with Clock gating in Active Mode		
Flip Flop	Remaining Circuit Power (µW)	Internal Clock Power (µW)	Total Power (µW)	Remaining Circuit Power (µW)	Internal Clock Power (µW)	Total Power (µW)
DCCER	83.2	19.8	103.0	83.5	19.8	103.3
Proposed DCCER	80.1	18.3	98.4	80.5	18.3	98.8
SCCER	75.2	20.2	95.4	74.4	20.2	94.6
Proposed SCCER	70.3	18.3	88.6	69.2	18.3	87.5

Table5. Power Consumed by Flip Flop with Sleep Mode

	Original Flip Flops in Sleep Mode			Flip Flops with Clock Gating in Sleep Mode		
Flip Flop	Remaining Circuit Power (µW)	Internal Clock Power (µW)	Total Power (µW)	Remaining Circuit Power (nW)	Internal Clock Power (nW)	Total Power (nW)
DCCER	83.2	19.8	103.0	5.4	4.5	9.9
Proposed DCCER	80.1	18.3	98.4	2.2	3.5	5.7
SCCER	75.2	20.2	95.4	8.5	3.5	11.0
Proposed SCCER	70.3	18.3	88.6	5.7	3.0	8.7

The results for the power consumed during the sleep (clock gated) mode. Power results significant savings when the clock gating is applied to the flip-flops during idle state. Power saving of more than 1000 times are obtained during the idle state when compared to the power consumed without clock gating. The power saving increase with increase in the data switching activity.

Table6. Observation of Delays with Clock Gating

Original Flip-Flops					Flip-Flops with Clock Gating			
Flips-Flops	Setup Time (ps)	Hold Time (ps)	CLK-Q Delay (ps)	D-Q Delay (ps)	Setup Time (ps)	Hold Time (ps)	CLK-Q Delay (ps)	D-Q Delay (ps)
DCCER	143	175	190	405	143	175	201	417
Proposed DCCER	125	160	176.3	390	125	160	180.5	401
SCCER	280	45	150.4	325	280	45	155.9	287
Proposed SCCER	255	15	123.5	310	255	15	129.5	316

Table 6 shows the delay comparisons between the original flip-flops and flip-flops with clock gating. The results show that the clock gating addition has no impact on setup and hold time of the flip-flops while CLK-Q delay and D-Q delay are increased.

VI. Pipelined Array Multiplier

To demonstrate the feasibility and effectiveness of the proposed energy recovery clocking scheme and flip flops, a pipelined using the proposed clocking scheme. The multiplier is 8x8 bit pipelined multiplier pipelined with SCCER flip flops and DCCER flip flops. The clock input of all flip flops are connected together an H-tree type of clock. The logic part of the design is composed of AND gate and full adder gates. A similar multiplier has been designed using transmission gate flip flop and square wave clock. The clock tree in this multiplier was also H-tree. However, buffer was inserted to properly propagate the square wave clock through the clock network. Results show a power reduction of 70% on the clock tree and total power savings of 25%-69% as compared to the same multiplier using conventional square wave clocking scheme and corresponding flip flops.

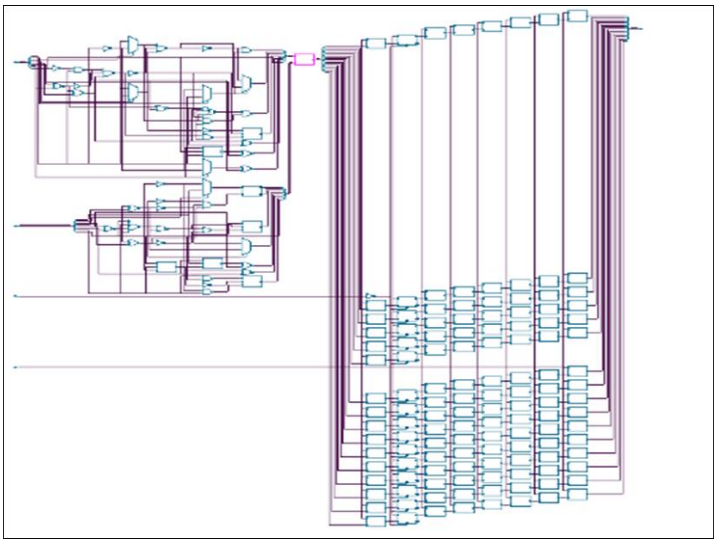

Fig.16 Pipelined Array Multiplier

VII. Conclusion

We proposed energy recovery clocked flip flops that enable energy recovery from the clock network, resulting in significant total energy saving compared to the square wave clocking. The proposed flip flops operate with a single phase sinusoidal clock, which can be generated with high efficiency. We implemented 1024 proposed energy recovery clocked flip-flops through an H-tree clock network driven by resonant clock generator, generating a sinusoidal clock. Simulation results show a power reduction of 90% on the clock tree and power saving of up to 80% as compared to the same implementation using conventional square wave clocking scheme and flip flops. We applied clock gating to energy recovery clocked flip-flops. Clock gating in energy recovery clocked flip flops result in significant power saving during the idle state of the flip flops without any considerable overhead compared to the original flip-flops. Energy recovery clocked pipelined multiplier with an integrated

resonant clock-generator, generating a sinusoidal clock. Results show a power reduction of 70% on the clock tree and total power savings of 25%-69% as compared to the same multiplier using conventional square wave clocking scheme and corresponding flip-flops. The results demonstrate the feasibility and effectiveness of the energy recovery clocking scheme in reducing total power consumption.

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Mashkoor Alam

I completed M. Tech with Electronics & Telecommunication, specialization in VLSI Design & Embedded System from KIIT University Bhubaneswar. I have done B.Sc. Engg. With Electronics & Communication Engineering from Ramgobind Institute of Technology Koderma which is affiliated by Vinoba Bhava University Hazaribag in 2008.

Rajendra Prasad

Rajendra Prasad is with KIIT University in the school of Electronics and Telecommunication as an Assistant Professor. He did his B. Tech from Satyabama University, Chennai in the year 2009. He completed his M. Tech from VIT University, Vellore in the year 2011.