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Design of Approximate Multiplier for Error-Tolerant Applications

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ABSTRACT
CMOS scaling has reached to the level, where process variation has become significant problem hindering further scaling. Various approaches to mitigate process variation effect try to nullify at the cost of increased area/power consumption. There are some applications which accept small errors such as multimedia processing. Designing accurate circuit for these applications is waste of area/power. This paper proposes low power, high speed approximate multiplier. The proposed multiplier outperforms and provides significant improvement in power, area, and delay at the cost of little degrade in accuracy. Experimental result shows that the proposed multipliers consume less power and require less area compared to conventional truncated multiplier.
***Keywords*:** CMOS technology, error-tolerant, low power, multiplier, truncation.

I. INTRODUCTION

In VLSI number of gates per chip area is constantly increasing, while gate switching energy does not decrease at the same rate, so power dissipation raises producing more heat and to remove heat various cooling techniques are used which are expensive and area taking. Power is the most important parameter for battery operated devices like laptops, cell phones etc. Multiplier is the core component in the processor of most of the digital signal processing applications and other arithmetic oriented applications [1-2]. So if approximate design of multiplier is used than there will be a significant improvement in performance of processor. Some an application in which small amount of error is tolerable are called error tolerant applications. These applications are related to human sense such as vision, smell, hear, touch; these do not require exact result. For these applications designing accurate multiplier is wastage of area/power. So multiplier that takes less area, less power consumption and less delay as compared to parallel multiplier called approximate multiplier is designed at the cost of small degradation in accuracy. Presented multipliers are based on truncating the least significant bits. One can get fixed-width multiplier by directly truncating about half the adder cells of parallel multiplier [3].For example [4] gave a simple method by truncating the half least significant partial product terms and to reduce the error probabilistic constant bias is added to the remaining cells. This design takes 50% area as compared to parallel multiplier but has large error because the constant bias is independent to the truncated bits. [5] Presented the fixed width multiplier to reduce the error depending on the partial product. This design gives less error as compared to previous one but error is still large for small numbers. [6] Presented low power shift and add multiplier for high speed multiplication. Some components of conventional serial multiplier which are more responsible for switching activities are replaced. This design provides better result in terms of area and accuracy at the cost of increased delay. To evaluate the performance of the approximate design following parameters are used [7].

Overall Error, OE: It is defined as | Rc-Ra|, where Rc denotes the accurate result and Ra denotes the result from approximate multiplier.
Accuracy: It is defined as (1- OE/Rc) x 100%, its value ranges from 0% to 100%.

Minimum acceptance accuracy (MAA): It is the threshold value of the results derived from the proposed multiplier. If they are higher than the minimum acceptance accuracy (MAA), they are called accepted results and are often defined by the customers/designers according to the specific applications.

Acceptance probability (AP): It is the probability that the accuracy of a multiplier is higher than minimum acceptance accuracy (MAA). It can be expressed as AP =P(ACC> MAA) and its value ranges from 0 to 1.

II. PROPOSED MULTIPLICATION ALGORITHM FOR APPROXIMATE MULTIPLICATION

2.1 PROPOSED APPROACH:

The algorithm for approximate multiplier is shown in fig.1.First; input operands are divided into two parts: accurate part and approximate part. Left part containing the most significant bits is the accurate part and the right part containing least significant bits is called the approximate part. Since least significant bits

contribute less as compared to most significant bits, for most-significant bits accurate multiplication is applied. The length of each part need not necessary be equal. The multiplication process starts from the starting point in two opposite directions simultaneously as shown in fig.1 ,the two 8-bit input operands, the multiplicand "11100110" (230) and multiplier "00110010"(56),are divided into two equal-sized parts , each part containing 4 input bits. As for the least significant bits of input operands (approximate part), a special mechanism is applied. The carry generation part which is responsible for more power consumption is removed and partial products are not generated. Every bit position from left to right is checked and if both input bits are 1 or one of two input bit is 1, the corresponding product term is 1 and from this bit onwards all the product bits of right side are 1, if both the input bits are 0,the corresponding product bit is 0 and it has no effect on the next right side bits.fig.1 shows the operation of approximate multiplier.

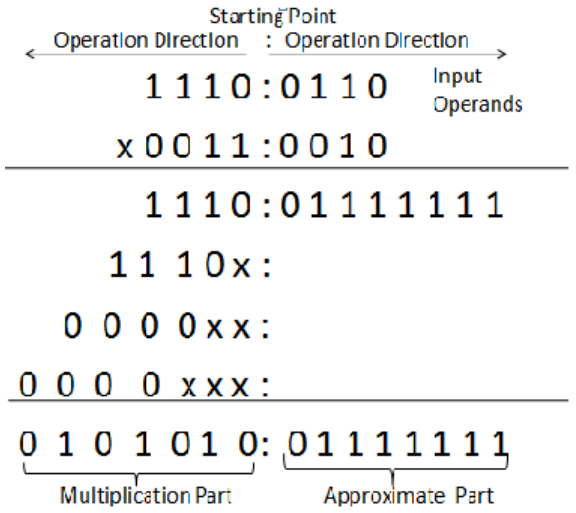


Fig.1 Operation of approximate multiplier

For the most significant bits, input operands fall into accurate part, the operation is conducted as per the normal multiplication operation, from right to left. Its circuit thus designed in the conventional way.

2.2 HARDWARE IMPLEMENTATION

The block diagram of 8-bit approximate multiplier is shown in fig.2. In the proposed design, input A and B are divided into two 4-bit blocks each. The control block contains two, 4-input NOR gates. In the first NOR gate input bits A7-A4 inputs are applied and on the second NOR gate input bits B7-B4 inputs are applied and the outputs of these two NOR gates are applied to the input of NAND gate. The control block is first used for detecting the logic "1" in the MSB position of the inputs, (A7-A4) and (B7-B4). When logic "1" is found, the "ctrl" signal will be activated and the input operands are high enough to operate in: (i) approximate part to give the lower order bits of the final output (P7-P0) and (ii) accurate part to generate the higher order bits of the product (P15-P8). If no logic "1" is detected by the control block, all the most significant bits are 0, the multiplexer selects accurate part to generate the lower order bits of the product (P7-P0).Fig.2 given below shows the hardware for 8-bit approximate multiplier.

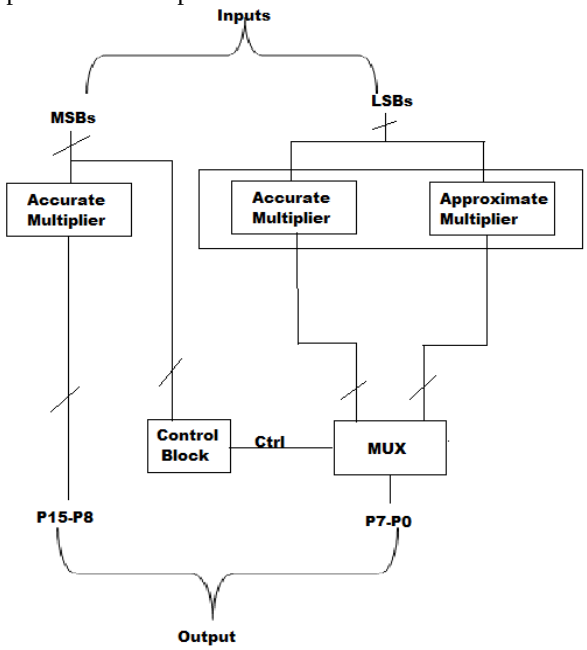


Fig.2 Architecture of Proposed Approximate Multiplier

In the accurate part, the standard 4-bit parallel multiplier is used to produce higher order output product terms (P15-P8) as shown in fig.3.

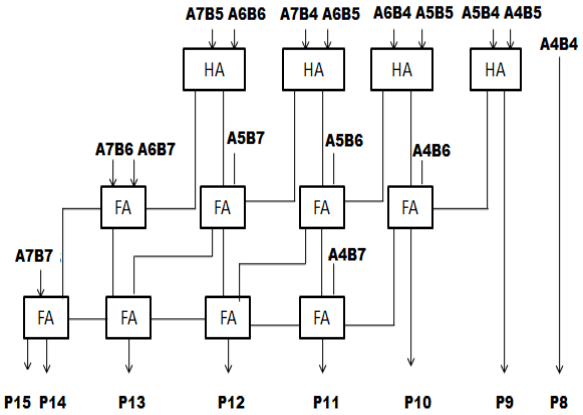
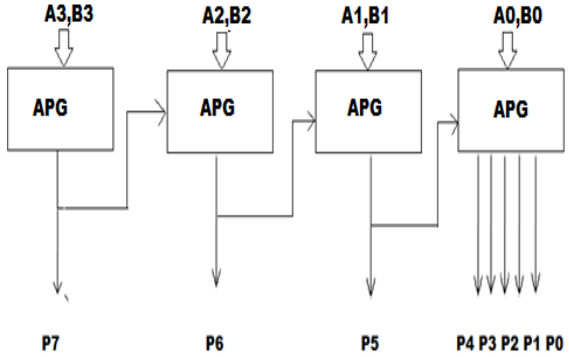
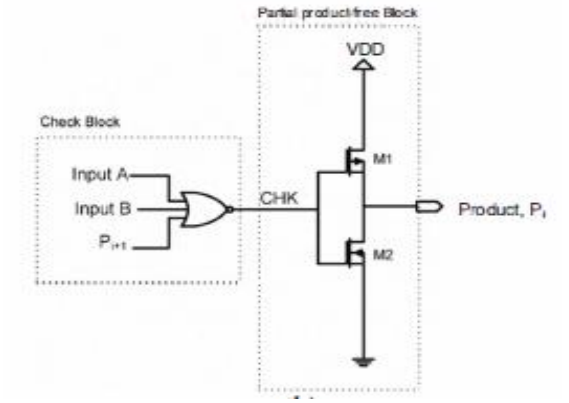


Fig.3 Design of Accurate Part

The approximate part is designed using APGs. For designing 4-bit approximate part 4 APGs are cascaded which generate lower output product (P7-P0).The APG circuit consists of one NOR gate with the inverter at its output.Fig.4 shows the architecture of approximate part using approximate product generators and internal circuit of APG.



(a)



(b)

Fig.4 Approximate part (a) Overall architecture (b) schematic diagram of PGC

As shown in fig.4 (a), when inputs A3 and B3 both are 0, the product P7 is 0 and it has no effect on the next product bits but if P7 is 1 then P6 to P0 all the product terms are set to 1 means if P_{i+1} is 1, the product term pi will be set to high and in this way, the high signal will be propagated to all the bit positions on its right.

III. EXPERIMENTAL SETUP

In this work all circuits are designed on Schematic Editor V14.1 and simulated on Tanner-spice V14.1 simulator with 45nm PTM file. Simulations were performed at 25°C with supply voltage of 1V.The power consumption and propagation delay during different switching activities were measured for proposed approximate multipliers(8-bit, 16-bit). Additionally standard parallel multipliers and truncated multipliers (different size) for all the above given bit-width were also designed to compare performance. The number of bits in truncation multiplier is taken as 2, 4 for 8-bit and 16-bit multipliers respectively. Area was also compared for these multipliers. To evaluate the accuracy of the proposed multiplier, all the designs are implemented on MATLAB. Over 100000 random input patterns were generated and applied to the multipliers.

IV. RESULT ANALYSIS

As shown in table.1, the proposed 8-bit multiplier takes 53% and 15.3% less area as compared to 8-bit standard parallel and truncation multiplier respectively. It takes 53% and 10% less power with 53% and 31% less delay as compared to parallel and truncation multiplier. Note that delay was calculated for different input patterns and worst case delay was considered. So the power delay product (PDP) is 78% and 39% less with the parallel and truncation multipliers.

TABLE1. Simulation Results of 8-Bit Standard Parallel, Truncation and Approximate Multiplier

8-bit Multipliers			
Parameters	Parallel	Truncation	Proposed
Area	2048	1118	946
Power (uw)	30	15.4	13.9
Delay (ns)	0.47	0.32	0.22
PDP (fj)	14.1	4.9	3

As shown in table 2, the proposed 16-bit multiplier takes 51% and 15% less area as compared to 16-bit standard parallel and truncation multiplier respectively. It takes 49% and 15% less power with 67% and 17% less delay as compared to parallel and truncation multiplier So the power delay product(PDP) is 83% and 29% less with the two above given multipliers.

TABLE 2. Simulation Results of 8-Bit Standard Parallel, Truncation and Approximate Multiplier

16-bit Multipliers			
Parameters	Parallel	Truncation	Proposed
Area (#of transistors)	9192	5212	4418
Power (uW)	61	36.5	31.2
Delay (ns)	1.5	0.60	0.50
PDP (fJ)	91.5	21.9	15.6

As the fig.5 shows below, the acceptable results at specific MAA. Note that the numbers of acceptable results are high for large number of bits.

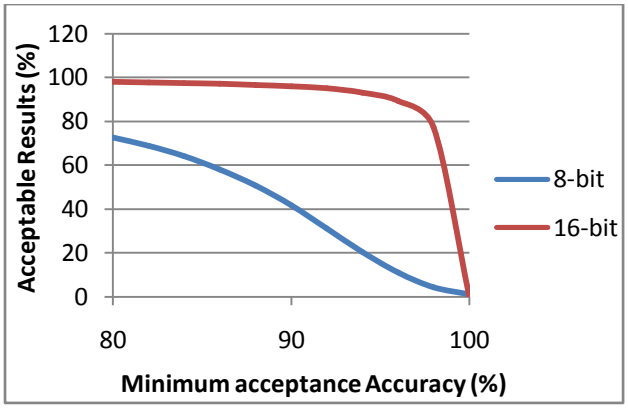


Fig.5 Comparison of Approximate multiplier with different bit sizes between MAA and AR

V. CONCLUSION

In the proposed design strategy, the multiplier circuit is redesigned into two different parts –Accurate part, which is implemented using standard parallel multiplier to achieve greater accuracy for higher order bits and approximate part, which generates small amount of error but this error is acceptable to circuit designer/customer because with small sacrifice of accuracy the proposed design provides noticeable saving in power and high speed operation. Such multipliers are widely used in multimedia and wireless communication.

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