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Fuzzy Controller Based Seven Level Modified H-Bridge Inverter For Grid Connected PV System

P.Srinivasa Reddy[1],S.Shamshul Haq [2], A.Mallikarjuna Prasad [3], S.Thirumalaiah[4]

PG Scholar, Department of EEE, St.Johns College of Engineering, Yemmiganur, India[1]
Assistant Professor, Department of EEE, St.Johns College of Engineering, Yemmiganur, India [2]
Associate Professor, Department of EEE, St.Johns College of Engineering, Yemmiganur, India [3,4]

ABSTRACT
This paper proposes a single-phase seven-level inverter for grid-connected photovoltaic systems, with a novel pulse width-modulated (PWM) control scheme. Three reference signals that are identical to each other with an offset value that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. The inverter is capable of producing seven levels of output-voltage levels (Vdc, 2Vdc/3, Vdc/3, 0, −Vdc, −2Vdc/3, −Vdc/3) from the dc supply voltage. And it recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm. Multilevel inverters offer improved output waveforms and lower THD. The circuit topology, modulation law, and operational principle of the proposed inverter were analyzed in detail. A FUZZY control is implemented to optimize the performance of the inverter. MATLAB/SIMULINK results indicate that the THD of the Fuzzy Controller Circuit is much lesser. Furthermore, both the grid voltage and the grid current are in phase at near-unity power factor. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. The less THD in the seven-level inverter compared with that in the five- and three-level inverters is an attractive solution for grid-connected PV inverters.
INDEX TERMS— Grid connected Photovoltaic system, Maximum power point tracking system, Single phase seven level inverter and fuzzy logic controller.

I. INTRODUCTION

The ever-increasing energy consumption, fossil fuels' soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the Sun's energy directly into electricity. Photovoltaic-generated energy can be delivered to power system networks through grid-connected inverters.

A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW. Types of single-phase grid-connected topology of this inverter are full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact.

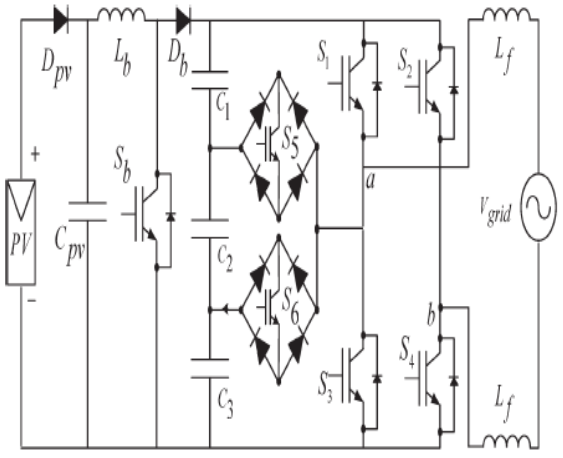


Fig.1. Proposed single-phase seven-level Grid-connected inverter for photovoltaic systems**.**

Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped, flying capacitor or multi cell, cascaded H-bridge, and modified H-bridge multilevel. This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed single-phase seven-level inverter was developed from the five-level inverter in. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by *C*1, *C*2, and *C*3, as shown in Fig. 1. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitors for inverters of the same number of levels. Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance *Lf* was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output-voltage levels (*V*dc, 2*V*dc/3, *V*dc/3, 0, −*V*dc, −2*V*dc/3, −*V*dc/3) from the dc supply voltage. The proposed inverter's operation can be divided into seven switching states, as shown in Fig. 2(a)–(g). Fig. 2(a), (d), and (g) shows a conventional inverter's operational states in sequence, while Fig. 2(b), (c), (e), and (f) shows additional states in the proposed inverter synthesizing one- and two-third levels of the dc-bus voltage. The required seven levels of output voltage were generated as follows.

1) Maximum positive output (*V*dc): *S*1 is ON, connecting the load positive terminal to *V*dc, and *S*4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is *V*dc. Fig. 2(a) shows the current paths that are active at this stage.

2) Two-third positive output (2*V*dc/3): The bidirectional switch *S*5 is ON, connecting the load positive terminal, and *S*4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is 2*V*dc/3. Fig. 2(b) shows the current paths that are active at this stage.

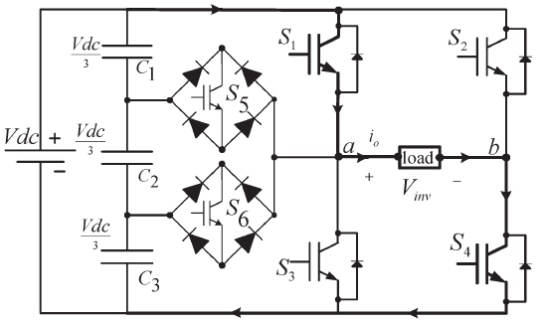
3) One-third positive output (*V*dc/3): The bidirectional switch *S*6 is ON, connecting the load positive terminal, and *S*4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is *V*dc/3. Fig. 2(c) shows the current paths that are active at this stage.

4) Zero output: This level can be produced by two switching combinations; switches *S*3 and *S*4 are ON, or *S*1 and *S*2 are ON, and all other controlled switches are OFF; terminal *ab* is a short circuit, and the voltage applied to the load terminals is zero. Fig. 2(d) shows the current paths that are active at this stage.

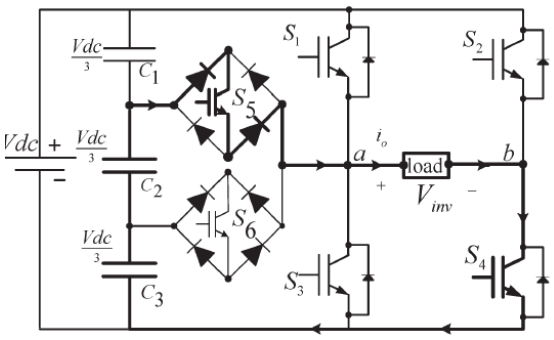
5) One-third negative output (−*V*dc/3): The bidirectional switch *S*5 is ON, connecting the load positive terminal, and *S*2 is ON, connecting the load negative terminal to *V*dc. All other controlled switches are OFF; the voltage applied to the load terminals is −*V*dc/3. Fig. 2(e) shows the current paths that are active at this stage.

6) Two-third negative output (−2*V*dc/3):The bidirectional switch *S*6 is ON, connecting the load positive terminal, and *S*2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to
the load terminals is −2*V*dc/3. Fig. 2(f) shows the current paths that are active at this stage.

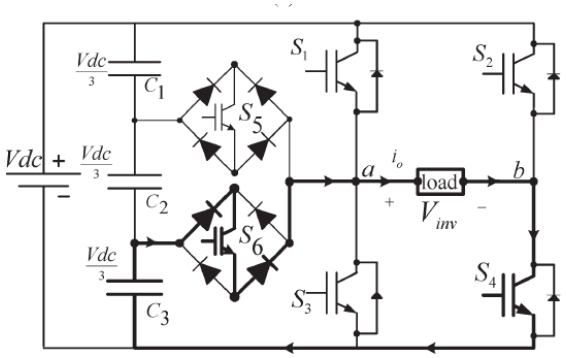
7) Maximum negative output (−*V*dc): *S*2 is ON, connecting the load negative terminal to *V*dc, and *S*3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is −*V*dc. Fig. 2(g) shows the current paths that are active at this stage.



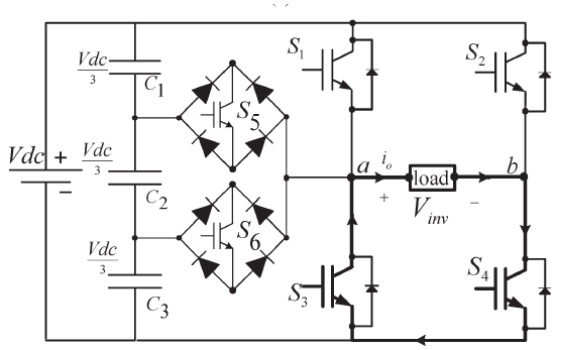
(a)



(b)

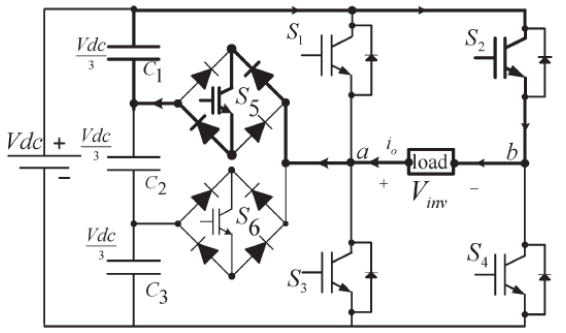


(c)

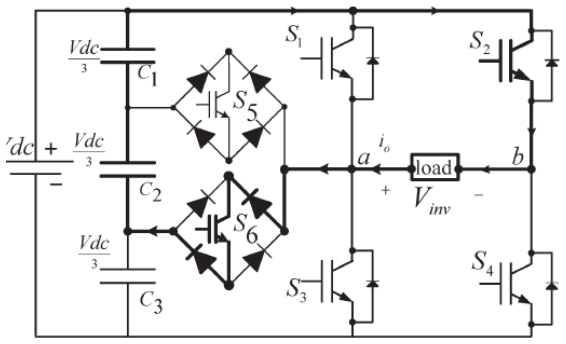


(d)

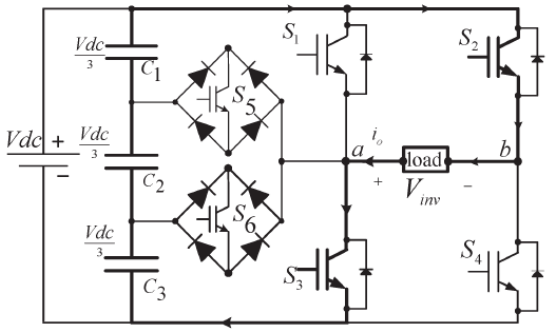
Fig.2. Switching combination required to generate the output voltage (*V*ab).
(a)*V*ab = *V*dc. (b) *V*ab = 2*V*dc/3.
(c)*V*ab = *V*dc/3. (d)*Vab* = 0.



(e)



(f)



(g)

Fig.2. (*Continued*.) Switching combination required to generate the output voltage (*V*ab).
(e)*V*ab=−*V*dc/3. (f)*Vab* = −2*V*dc/3. (g) *V*ab = −*V*dc

TABLE I

OUTPUT VOLTAGE ACCORDING TO THE SWITCHES' ON–OFF CONDITION

v_0	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	on	off	off	on	off	off
$2V_{dc}/3$	off	off	off	on	on	off
$V_{dc}/3$	off	off	off	on	off	on
0	off	off	on	on	off	off
0*	on	on	off	off	off	off
$-V_{dc}/3$	off	on	off	off	on	off
$-2V_{dc}/3$	off	on	off	off	off	on
$-V_{dc}$	off	on	on	off	off	off

Table I shows the switching combinations that generated the seven output-voltage levels (0, −*V*dc, −2*V*dc/3, −*V*dc/3, *V*dc, 2*V*dc/3, *V*dc/3).

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (*V*ref1, *V*ref2, and *V*ref3) were compared with a carrier signal (*Vcarrier*). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If *V*ref1 had exceeded the peak amplitude of *V*carrier, *V*ref2 was compared with *V*carrier until it had exceeded the peak amplitude of *V*carrier. Then, onward, *V*ref3 would take charge and would be compared with *V*carrier until it reached zero. Once *V*ref3 had reached zero, *V*ref2 would be compared until it reached zero.

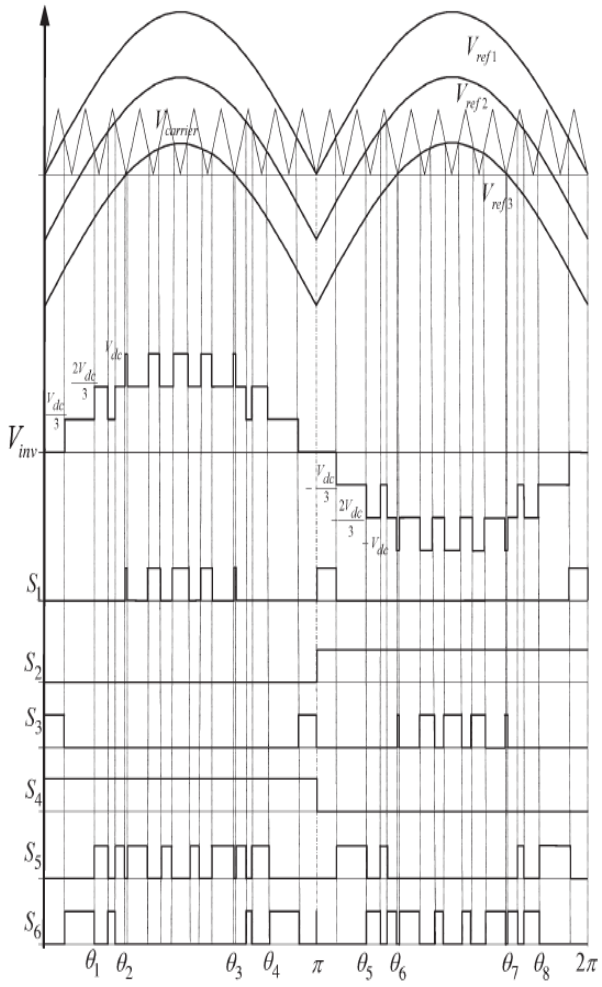


Fig.3. Switching pattern for the single- phase seven-level inverter.

Then, onward, *V*ref1 would be compared with $V_{carrier}$. Fig. 3 shows the resulting switching pattern. Switches *S*1, *S*3, *S*5, and *S*6 would be switching at the rate of the carrier signal frequency, whereas *S*2 and *S*4 would operate at a frequency that was equivalent to the fundamental frequency. For one cycle of the fundamental frequency, the proposed inverter operated through six modes. Fig. 4 shows the per unit output-voltage signal for one cycle.

The six modes are described as follows:

Mode 1: $0 < \omega t < \theta_1$ and $\theta_4 < \omega t < \pi$
Mode 2: $\theta_1 < \omega t < \theta_2$ and $\theta_3 < \omega t < \theta_4$
Mode 3: $\theta_2 < \omega t < \theta_3$
Mode 4: $\pi < \omega t < \theta_5$ and $\theta_8 < \omega t < 2\pi$
Mode 5: $\theta_5 < \omega t < \theta_6$ and $\theta_7 < \omega t < \theta_8$
Mode 6: $\theta_6 < \omega t < \theta_7$. (1)

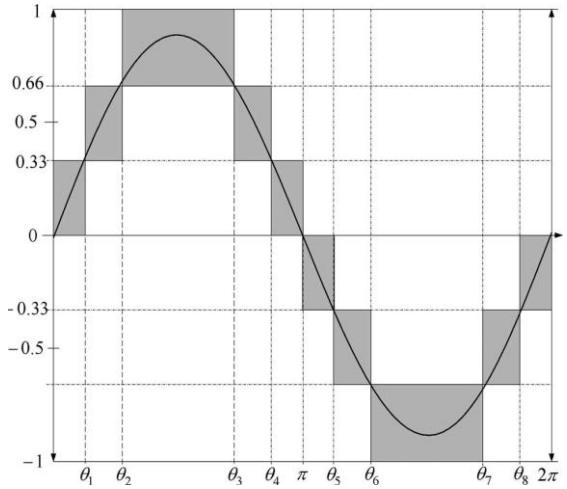


Fig.4. Seven-level output voltage (V_{ab}) and switching angles.

The phase angle depends on modulation index *Ma*. Theoretically, for a single reference signal and a single carrier signal, the modulation index is defined to be

$$M_a = \frac{Am}{Ac} \quad (2)$$

While for a single-reference signal and a dual carrier signal, the modulation index is defined to be

$$M_a = \frac{Am}{2Ac} \quad (3)$$

Since the proposed seven-level PWM inverter utilizes three carrier signals, the modulation index is defined to be

$$M_a = \frac{Am}{3Ac} \quad (4)$$

Where *Ac* is the peak-to-peak value of the carrier signal and *Am* is the peak value of the voltage reference signal V_{ref}.
When the modulation index is less than 0.33, the phase angle displacement is

$$\theta 1 = \theta 2 = \theta 3 = \theta 4 = \frac{\pi}{2} \quad (5)$$

$$\theta 5 = \theta 6 = \theta 7 = \theta 8 = \frac{3\pi}{2} \quad (6)$$

On the other hand, when the modulation index is more than 0.33 and less than 0.66, the phase angle displacement is determined by

$$\theta 1 = \sin^{-1}\left(\frac{Ac}{Am}\right) \quad (7)$$

$$\theta 2 = \theta 3 = \frac{\pi}{2} \quad (8)$$

$$\theta 4 = \pi - \theta 1 \quad (9)$$

$$\theta 5 = \pi + \theta 1 \quad (10)$$

$$\theta 6 = \theta 7 = 3\pi/2 \quad (11)$$

$$\theta 8 = 2\pi - \theta 1 \quad (12)$$

If the modulation index is more than 0.66, the phase angle displacement is determined by

$$\theta_1 = \sin^{-1}\left(\frac{Ac}{Am}\right) \quad (13)$$

$$\theta_2 = \sin^{-1}\left(\frac{2Ac}{Am}\right) \quad (14)$$

$$\theta 3 = \pi - \theta 2 \quad (15)$$

$\theta 4 = \pi - \theta 1$ (16)
$\theta 5 = \pi + \theta 1$ (17)
$\theta 6 = \pi + \theta 2$ (18)
$\theta 7 = 2\pi - \theta 2$ (19)
$\theta 8 = 2\pi - \theta 1$ (20)

For M_a that is equal to, or less than, 0.33, only the lower reference wave (V_{ref3}) is compared with the triangular carrier signal. The inverter's behaviour is similar to that of a conventional full-bridge three-level PWM inverter. However, if M_a is more than 0.33 and less than 0.66, only V_{ref2} and V_{ref3} reference signals are compared with the triangular carrier wave. The output voltage consists of five dc-voltage levels. The modulation index is set to be more than 0.66 for seven levels of output voltage to be produced. Three reference signals have to be compared with the triangular carrier signal to produce switching signals for the switches.

III. CONTROL SYSTEM

As Fig. 5 shows, the control system comprises a MPPT algorithm, a dc-bus voltage controller, reference-current generation, and a current controller. The two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, also under the presence of grid voltage harmonics. The proposed inverter utilizes the perturb-and-observe (P&O) algorithm for its wide usage in MPPT owing to its simple structure and requirement of only a few measured parameters. It periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with that of the previous perturbation cycle. If the power was increasing, the perturbation would continue in the same direction in the next cycle; otherwise, the direction would be reversed. This means that the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm will oscillate around it. The P&O algorithm was implemented in the dc–dc boost converter. The output of the MPPT is the duty-cycle function. As the dc-link voltage V_{dc} was controlled in the dc–ac seven level PWM inverter, the change of the duty cycle changes the voltage at the output of the PV panels. The grid period and phase must be detected. The proposed inverter provides an analog zero-crossing detection circuit on one of its input ports where the grid voltage is to be connected. The zero-crossing circuit then produces an in-phase square-wave output that is fed into the digital I/O port. The feedback controller used in this application utilizes the FUZZY algorithm. The current injected into the grid, also known as grid current I_{grid}, was sensed and fed back to a comparator that compared it with the reference current $I_{gridref}$. $I_{gridref}$ is the result of the MPPT algorithm. The error from the comparison process of I_{grid} and $I_{gridref}$ was fed into the controller. The output of the FUZZY controller, also known as V_{ref}, goes through an anti windup process before being compared with the triangular wave to produce the switching signals for$S1–S6$.Eventually, V_{ref} becomes V_{ref1}; V_{ref2} and V_{ref3} can be derived from V_{ref1} by shifting the offset value, which was Equivalent to the amplitude of the triangular wave.

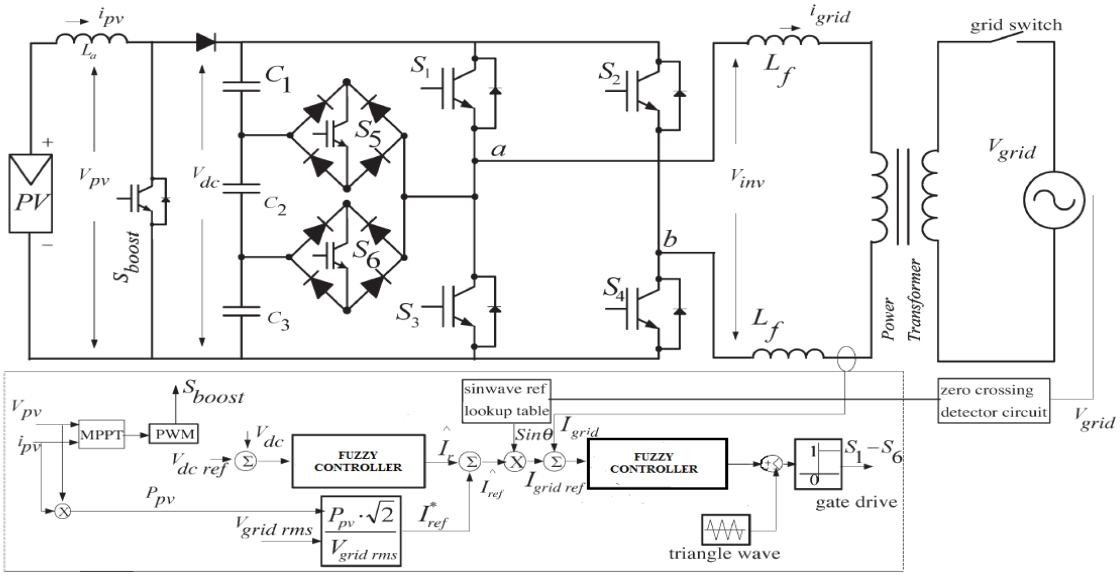


Fig.5. Seven-level inverter with closed-loop control algorithm.

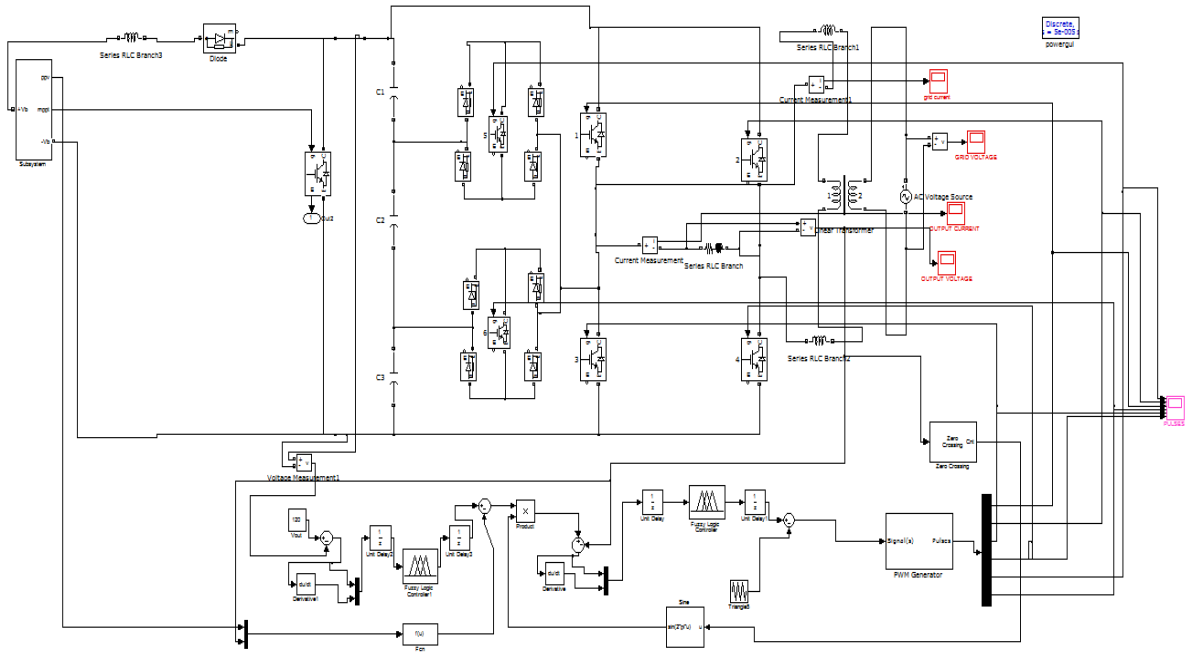


Fig.(6)ATLAB SIMULINK MODEL OF MODIFIED H-BRIDGE INVERTER USING FUZZY CONTROLLER

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented in a prototype. The PWM switching patterns were generated by comparing three reference signals (V_{ref1}, V_{ref2}, and V_{ref3}) against a triangular carrier signal (see Fig. 6). Subsequently, the comparing process produced PWM switching signals for switches *S*1–*S*6, as Figs. 7–9 show. One leg of the inverter operated at a high switching rate that was equivalent to the frequency of the carrier signal, while the Other leg operated at the rate of the fundamental frequency i.e. 50hz. Switches *S*5 and *S*6 also operated at the rate of the carrier signal. Fig. 10 shows the simulation result of inverter output voltage V_{inv}. The dc-bus voltage was set at 300 V ($>\sqrt{2}V$grid; in this case, V_{grid} was 120 V).The dc-bus voltage must always be higher than $\sqrt{2}$ of *V*grid to inject current into the grid, or current will be injected from the grid into the inverter.

Therefore, operation is recommended to be between *Ma* = 0.66 and *Ma* = 1.0. *V*inv comprises seven voltage levels, namely, V_{dc}, $2V_{dc/3}$, $V_{dc/3}$, 0, $-V_{dc}$, $-2V_{dc/3}$, and $-V_{dc/3}$. The current flowing into the grid was filtered to resemble a pure sine wave in phase with the grid voltage (see Fig. 11). As I_{grid} is almost a pure sine wave at unity power factor

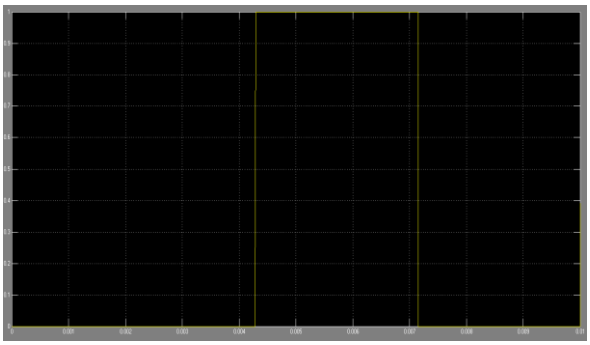


Fig.7. PWM signals for *S*1.

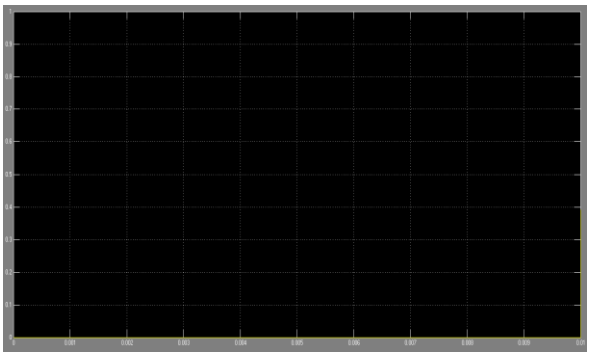


Fig.8. PWM signals for *S*2 .

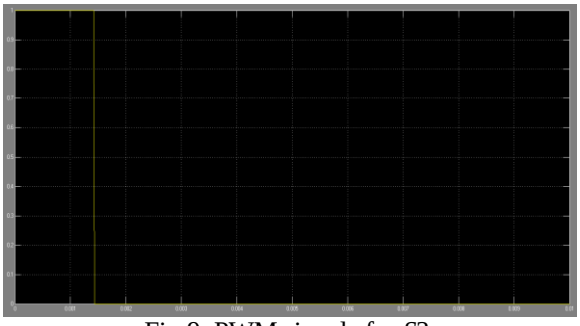


Fig.9. PWM signals for *S*3.

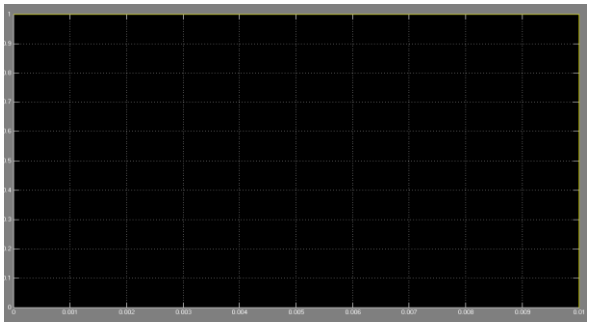


Fig.10. PWM signals for *S*4

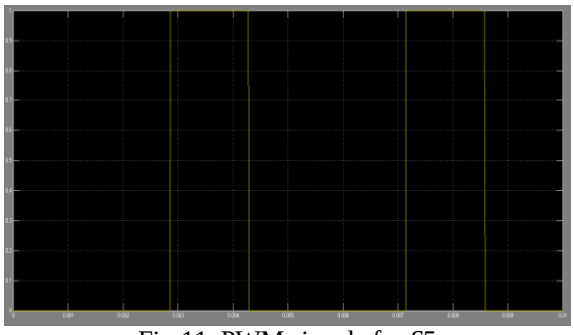


Fig.11. PWM signals for *S*5

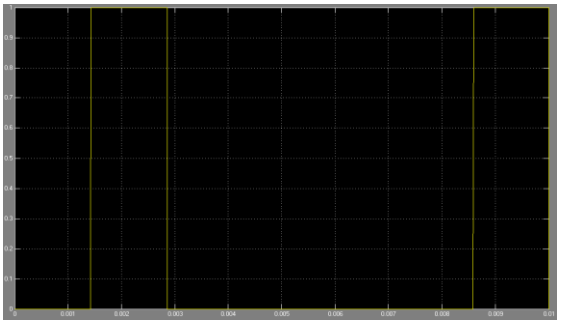


Fig.12. PWM signals for *S*6

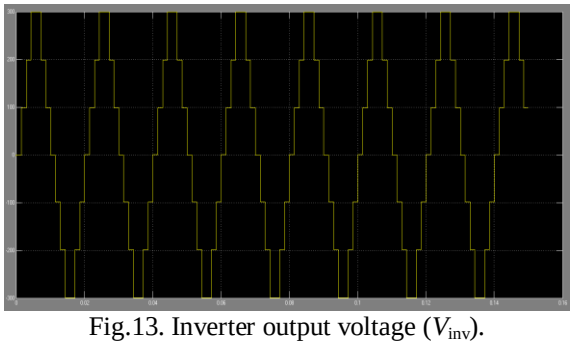


Fig.13. Inverter output voltage (V_{inv}).

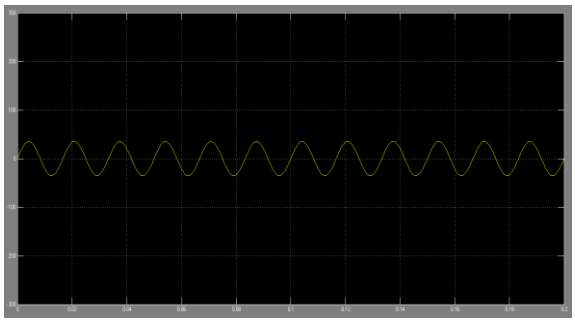


Fig.14. Grid voltage

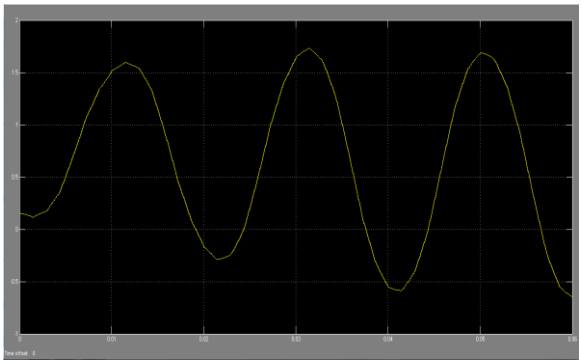


Fig.15. Grid current

V. Multilevel Inverter Specifications and Controller Parameters.

The below table depicts the specifications and parameters of the inverter

TABLEII

PV array rated voltage	1.2 kV
Standard Environmental Condition Solar radiation, G Cell temperature, T	1000 W/m^2 25 0^C
System Frequency	50 Hz
Switching Frequency	2K Hz
L_b	2.2mh
L_f	3mh
C1-C3	220μF
Inverter output voltage	300v

VI.CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes three reference signals and a triangular carrier signal to generate PWM switching signals. The behaviour of the proposed multilevel inverter was analyzed in detail. a FUZZY control is implemented to optimize the performance of the inverter. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. The less THD in the seven-level inverter compared with that in the five- and three-level inverters is an attractive solution for grid-connected PV inverters.

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BIOGRAPHIES

P.SRINIVASA REDDY is doing M.Tech in Power Electronics and Drives in St.Johns College of Engineering, Yemmiganur, Kurnool District. His research interests are Power Electronics, Ac motor drives

S.SHAMSHUL HAQ is the Assistant Professor in the department of EEE, St.Johns College of Engineering, Yemmiganur. He has 6 years of teaching experience. His areas of interests are Power systems, Power Electronics, Ac motor drives.

A.MALLIKARJUNA PRASAD has obtained his B.E from MADRAS University in the year 2001. He has obtained his M.E from Sathyabama University in the year 2004. He has 10 years of teaching experience. Presently he is a research scholar in JNTU, KAKINADA. He is working in the area of high power density dc-dc converters

S.THIRUMALAIAH has obtained his B.TECH from S.K University in the year 2002. He has obtained his M.TECH from J.N.TU HYDERABAD in the year 2008. He has 6 years of teaching experience. Presently he is a research scholar in JNTU, ANATAPUR. He is working in the area of power system control with application of power electronics.