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Comparison of Characteristic Curve of Drain-Source Electron Transport Properties   in ZnO and GaAs Based MOSFETs Using Monte Carlo Simulation

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Abstract
The effect of gate length and Thickness on the characteristic curve of drain-source current verse gate voltage in ZnO and GaAs MOSFETs have been simulated. Three transistors with gate lengths of 30, 40 and 50 nm are simulated. Simulations show that with a fixed channel length, when the gate length is increases, the output drain current would be increased, the Moreover, with increasing oxide Thickness the drain current is reduced, which results in the reduced drain barrier lowering. At last, A comparison between thickness and gate lengths of two semiconductors have been discussed.
Keywords: MOSFET, ZnO, GaAs, Gate Length, Oxide thickness, Drain voltage.

I. Introduction

Zinc oxide (ZnO) a wide band-gap *II-VI* compound semiconductor, has a stable wurtzite structure . It has attracted intensive research effort for its unique properties and versatile applications in transparent electronics, ultraviolet (UV) light emitters, piezoelectric devices, chemical sensors and spin electronics [1],[2] . ZnO has been proposed to be a more promising UV emitting phosphor than GaN because of its larger exciton binding energy. Gallium arsenide (GaAs) is a compound of the element s gallium and arsenic. It is a III-V semiconductor and is used in the manufacture of devices such as microwave frequency integrated circuits, monolithic microwave Infrared light-emitting diodes , Laser diodes , Solar cells and optical windows.

The goal of this paper is to investigate the effects of changing gate lengths and oxide thicknesses on the characteristic curve of drain-source current verse gate voltage in ZnO and GaAs MOSFETs individually and a comparison between these two materials has been determined afterwards.

This paper is organized as follows. Details of simulation model are presented in section 2 , the results of the method to the cases of ZnO and GaAs mosfets   are discussed in section 3 And some conclusion remarks will be reported in section 4.

II. Model details

The Monte Carlo (MC) method solves the Boltzmann transport equation by simulating the montion of electron and holes in the bulk semiconductor medium or device structure The main feature of the MC method is that a carrier is treated as a point-like semiclassical particle moving under the action of the local electric field and the scatering processes. The individual trajectories of carriers are computed by the follwing steps,

1. **Each carrier is moved in real and reciprocal space in the " free flight"**
   Between collisions under the action of the electric field.
2. **The carrier scatter** conditionally at the end of their free flights . The duration of a free flight and the new state after scattering are chosen stochastically in accordance with quantum mechanical theory.

In this survey, we have assumed a three-valley model for the conduction band. The first-principles band structure of wurtzite band structure predicts a direct band gap located at the Γ point and lowest energy conduction band satellite valleys at the U point and at the K point. In our Monte Carlo simulation, the Γ valley, the six equivalent U valleys, the two equivalent K valleys, are represented by ellipsoidal, non-parabolic dispersion relationships of the following Form

$$E(k) = [1 + \alpha_i E(k)] = \frac{\eta^2}{2} \left[\frac{k_x^2 + k_y^2}{m_{\parallel}^*} + \frac{k_z^2}{m_{\perp}^*} \right]$$

Where m* is effective mass at the band edge and α_i is the non- parabolicity coefficient of the i-th valley given by Kane model [26] . For each simulation, the motion of thirty thousand electron particles at an averaging time of 10e-14 are examined, the temperature being set to 300 K. Electrons in bulk material suffer intravalley scattering by polar optical, non-polar optical and acoustic phonons scattering, internally phonons, and ionized impurity scattering. Band edge energies, effective masses and non-

parabolicities are derived from empirical pseudopotential calculations. In this study, two thin transistors were investigated. The channel length was held constant, but the gate length covers part or all of the channel length. Then by holding the channel length constant, the effect of the change of the gate length on the characteristics of the transistor was studied.

III.   RESULTS AND DISCUSSION

The effect of gate length on electron transport in both ZnO and GaAs based MOSFETs with 30, 40 and 50nm gate lengths have been illustrated separately in figures 1a to 1b.
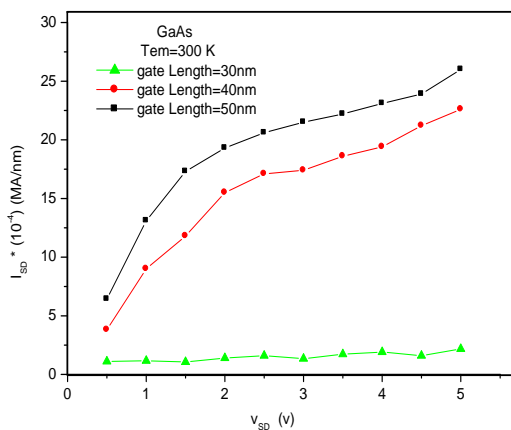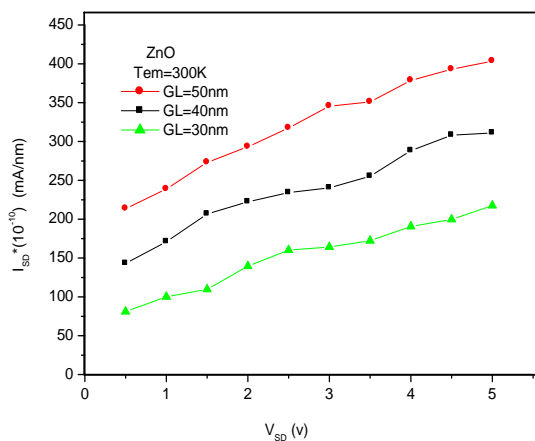
Figures 1a and 1b : Various gate lengths for ZnO and GaAs respectively.

Both figures indicate that as the gate length decreases, the output current would decrease as well. This decrease is probably due to the lessen of longitudinal electric field under the gate region which results in reduced electron velocity, Since the gate produces the channel by making inversion layer .Therefore, as the gate length increase from 30nm to 50nm, we see an increase in the current curve as a function of source – drain voltage .

The diagrams of oxide thicknesses in ZnO and GaAs –based MOSFETs are presented below .
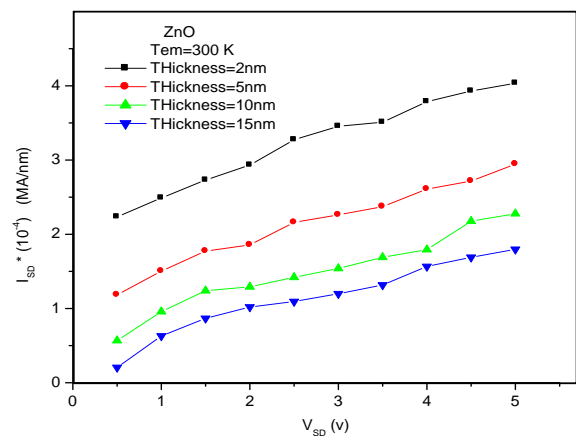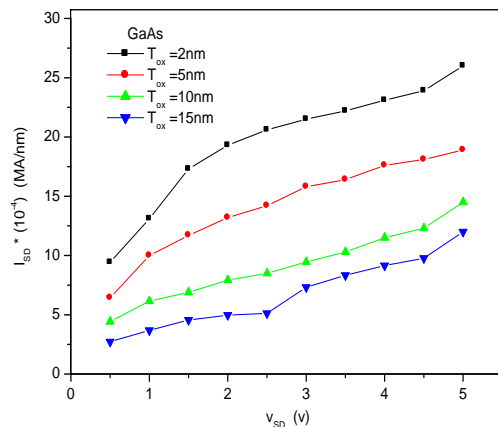
Figures 2a and 2b: Various Thicknesses for ZnO and GaAs respectively.

According to the equation (2) below , In order to support the reduction of L_g at each new technologynode, l_d must be reduced in proportion to L_g. This means that we must reduce T_{ox}, W_{dep} and X_j . In reality all three are reduced at each node to achieve the desired reduction in l_d . The minimum acceptable L is several times of l_d.

$$I_d \propto \sqrt[3]{T_{ox} W_{dep} X_j}$$

Reducing T_{ox} increases the gate control or C_{oxe}. Reducing X_j decreases C_d by reducing the size of the drain electrode. Reducing W_{dep} also reduces C_d by introducing a ground plane   that shields the channel from the drain. One way to summarize the message of equation above, is that vertical dimensions in a MOSFET (T_{ox}, W_{dep}, X_j) must be reduced in order to support the reduction of gate length.

In summary, scaling improves cost, speed, and power per function with every new technology generation. All of these attributes have been improved by 10 to 100 million times in four decades . An

engineering achievement unmatched in human history, When it comes to ICs, small is beautiful.

There are two reasons to reduce the oxide thickness. First, a thinner oxide, i.e. a larger Cox raises Ion. A large Ion is desirable for maximizing the circuit speed . The second reason is to control V_t roll-off in the presence of falling L. Although thinner oxide is desirable, it prevents engineers from using arbitrarily thin gate oxide films due to complexity of manufacturing and oxide break dawn. If the oxide is too thin, the electric field in the oxide can be so high as to cause destructive breakdown [3] .

Finally, two comparative schema of variation in thicknesses and gate lengths have been surveyed in the following with constant gate volte 3(v).

In both figures we see GaAs has upper current rate rather than ZnO. Due to their extremely small transport mass leading to high injection velocity , III-V compounds appear to be very attractive candidates as channel materials for highly scaled n-MOSFETs . However , III-V materials have many significant and fundamental issues, which may prove to be severe bottlenecks to their implementation.
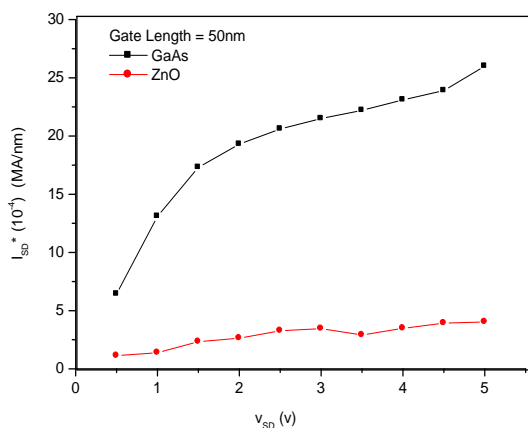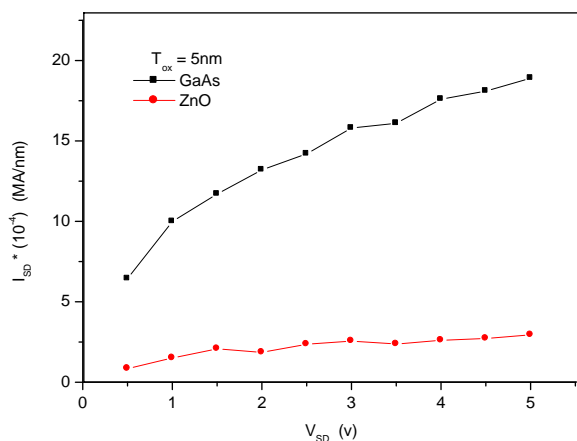
IV.   Conclusion

The effect of gate length on electron transport in ZnO and GaAs MOSFETs has been studied. The I-V characteristics show that higher currents are reached as the gate length is increased as a result of the increase in longitudinal electric field .The results are in good agreement with other simulation works . The results show that higher velocities are reached as the gate length is reduced as a result of the increase in longitudinal electric V materials have more current density as compared to Si and Ge, which is highly desired for channel material.

References

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Figure 3a and 3b : Comparison of two semiconductors ZnO and GaAs in constant thickness and length gates .