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A Novel Technique For Simulation & Analysis Of SVPWM Two &Three Level Inverters

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ABSTRACT:
This paper proposes a software implementation for two level & three level inverter using space vector modulation techniques. This software implementation is performed by using MATLAB/SIMULINK software. This paper gives comparison between SVPWM Three phase two level & three level inverter. Two level inverter is the basic technique to implement any level. The main advantage of the two level inverter is simple in computation and also switching device selection is simple. It is becomes difficult in high voltage & high power applications due to the increased switching losses and limited rating of the dc link voltage. Multilevel inverters are used in high voltage and high power applications with less harmonic contents. The harmonic contents of a three level inverter are less than that of two level inverters. And also rating of the dc link voltage is high. The simulation study reveals that three level inverter generates less THD compared to two-level inverter.
Key words—SVPWM, THD, TWO LVEL &THREE LEVEL INVERTERS

I. INTRODUCTION

Three phase voltage-fed PWM inverters are recently growing popularity for multi-Megawatt industrial drive applications. The main reasons for this popularity are easy Sharing of large voltage between the series devices and the improvement of the harmonic quality at the output as compared to a two level inverter. The Space Vector PWM of a three level inverter provides the additional advantage of superior harmonic quality. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases significantly. It is well known that multi-level inverters are suitable in high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and attains higher voltages with limited maximum device ratings. As the number of levels is increased, the amount of switching devices and other component are also increased, making the inverter becoming more complex and costly [6].

In case of the conventional two level inverter configurations, the harmonic contains reduction of an inverter output is achieved mainly by raising the switching frequency. However in the field of high voltage, high power applications, and the switching frequency of the power device has to be restricted below 1 KHz due to the increased switching losses. So the harmonic reduction by raised switching frequency of a two-level inverter becomes more difficult in high power applications. In addition, as the D.C. link voltage of a two-level inverter is limited by voltage rating of the switching device. From the aspect of harmonic reduction and high Dc-link voltage level, three-level approach looks like a most alternative.

II. ANALYSIS OF TWO LEVEL SVPWM INVERTER

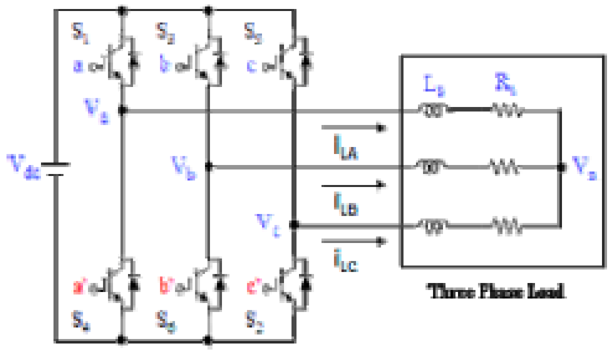


Figure.1 Three phase two level voltage source inverter

Space Vector Modulation (SVM) [1] was originally developed as vector approach to Pulse Width Modulation for three phase inverters. It is a more sophisticated technique for generating sine wave that provides higher voltages with lower total harmonic distortion. The circuit model of a typical three-phase two level voltage source PWM inverter is shown in “Figure.1”. S_1 to S_6 are the six power switches that shape the output, which are controlled by the switching variable a, a’, b, b’, c and c’. When an upper transistor is switched on, i.e., when a, b or c is 1, the corresponding lower transistor is switched on, i.e., the corresponding a’, b’ or c’ is zero .Therefore, the on and off states of the transistors can be used to determine the output voltage. In this PWM technique180^0 conduction is used for generating the gating signals. If two switches, one upper and one lower switch conduct at the same time such that the output voltage is ± Vs. the switch state is 1.If these two switches are off at the same time, the switch state is 0.

2.1 .SWITCHING STATES

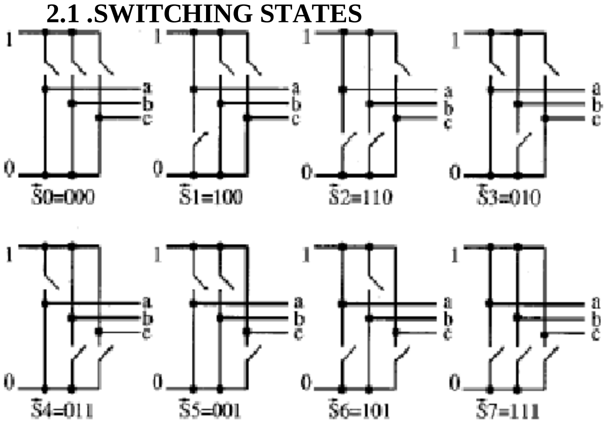


Figure.2 Switching states of two level inverter [5]

The total number of switching states in an "N" level inverter is "N^3".So the total number of switching states in a "2" level inverter is "2^3" that is 8 switching states. . They are S_0, S_1, S_2, S_3, S_4, S_5, S_6, and S_7. S_0 and S_7 are called as zero switching states because during which there is no power flow from source to load.S_1 to S_6 are called as active switching states.

2.2 SPACE VECTOR DIAGRAM OF TWO-LEVEL INVERTER

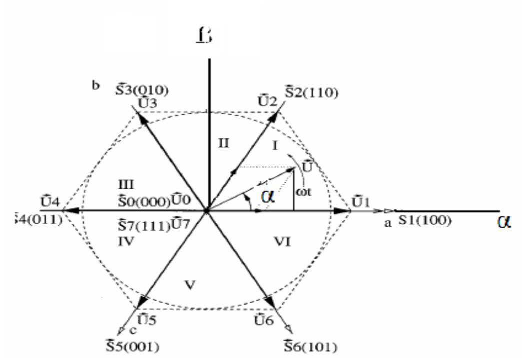


Figure.3 Space vector diagram of two level inverter [5]

Space vector diagram is divided into six sectors. The duration of each sector is 60^0. V_1, V_2, V_3, V_4, V_5, V_6 are active voltage vectors and V_0 & V_7 are zero voltage vectors. Zero vectors are placed at origin. The lengths of vectors V_1 to V_6 are unity and lengths of V_0 and V_7 are zero. The space vector V_s constituted by the pole voltage V_{ao}, V_{bo}, and V_{co} is defined as [4]

$V_s = V_{ao} + V_{bo}\, e^{j(2\pi/3)} + V_{co}\, e^{j(4\Pi/3)}$

$V_{ao}=V_{an} + V_{no}$, $V_{bo}=V_{bn} + V_{no}$ and $V_{co}=V_{cn}+ V_{no}$

$V_{an}+V_{bn}+V_{cn}=0$

$V_{no}= (V_{ao}+V_{bo}+V_{co}) /3$

The relation between the line voltages and the pole voltages is given by

$V_{ab} = V_{ao} – V_{bo}$, $V_{bc} = V_{bo} – V_{co}$, $V_{ca} = V_{co} – V_{ao}$

FOR example voltage vector V_1 that is 100

$V_{ao}=V_{dc}$, V_{bo}=0and V_{co}=0, then V_n= $(V_{dc}+0+0)/3=V_{dc}/3)$

$V_{an}=V_{ao}-V_{no} = (2/3)\ V_{dc}$, $V_{bn}=V_{bo}-V_{no}= (-1/3)\ V_{dc}$, $V_{cn}=V_{co}-V_{no}= (-1/3)\ V_{dc}$

$V_{ab}=V_{ao}-V_{bo}=V_{dc}$, $V_{bc}=V_{bo}-V_{co}=0$ & $V_{ca}=V_{co}-V_{ao}=-V_{dc}$

TABLE.I
SWITCHING VECTORS, PHASE VOLTAGES, OUTPUT VOLTAGES

Voltage Vectors	Switching vectors			Line to neutral voltages			Line to line voltages		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

(Note: Resp. voltages should be multiplied by V_{dc})

III. ANALYSIS OF THREE LEVEL INVERTER

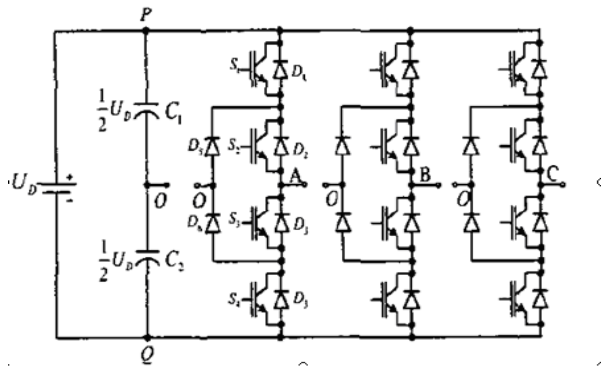


Figure.4. Three Phase three level voltage source inverter

The circuit [2] employs 12 power switching devices and 6 clamping diodes. Each arm contains four IGBTs, four anti parallel diodes and two neutral clamping diodes. And the dc bus voltage is split into three levels by two series connected bulk capacitors C_1, C_2 two capacitors have been used to divide the DC link voltage into three voltage levels, thus the name of 3-level.The middle point of the two capacitors can be defined as the neutral point 0.

The output voltage V_{ao} has three different states: $V_{dc}/2$, 0 and $-V_{dc}/2$.For voltage level $+V_{dc}/2$, switches S_1 & S_2 need to be turned on .For voltage level 0, switches S_2 & S_3 need to be turned on. For voltage level $-V_{dc}/2$ switches S_3 & S_4 need to be turned on. We can define these states as 2, 1, and 0. Using switching variable S_a and dc bus voltage V_{dc}, the output phase voltage V_{ao} [2] is obtained as follows:

$V_{ao} = (S_a\text{-}1)/2 \times V_{dc}$

TABLE.II
THE SWITCHING VARIABLES OF PHASE A

V_{ao}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_a
$+V_{dc}/2$	1	1	0	0	2
0	0	1	1	0	1
$-V_{dc}/2$	0	0	1	1	0

TABLE III
SWITCHING STATES OF THREE LEVEL INVERTER

Switching states	S_a	S_b	S_c	Voltage Vectors
S_1	0	0	0	V_0
S_2	1	1	1	V_0
S_3	2	2	2	V_0
S4	1	0	0	V_1
S_5	1	1	0	V_2
S_6	0	1	0	V_3
S_7	0	1	1	V_4
S_8	0	0	1	V_5
S_9	1	0	1	V_6
S_{10}	2	1	1	V_7
S_{11}	2	2	1	V_8
S_{12}	1	2	1	V_9
S_{13}	1	2	2	V_{10}
S_{14}	1	1	2	V_{11}
S_{15}	2	1	2	V_{12}
S_{16}	2	1	0	V_{13}
S_{17}	1	2	0	V_{14}
S_{18}	0	2	1	V_{15}
S_{19}	0	1	2	V_{16}
S_{20}	1	0	2	V_{17}
S_{21}	2	0	1	V_{18}
S_{22}	2	0	0	V_{19}
S_{23}	2	2	0	V_{20}
S_{24}	0	2	0	V_{21}
S_{25}	0	2	2	V_{22}
S_{a26}	0	0	2	V_{23}
S_{27}	2	0	2	V_{24}

3.1 SPACE VECTOR DIAGRAM OF THREE LEVEL SVPWM INVERTER

The plane can be divided into 6 major triangular sectors (I to VI) by large voltage vectors and zero voltage vectors. Each major sector represents $60^0$of the fundamental cycle. Within each major sector, there are 4 minor triangular sectors. There are totally 24 minor sectors in the plane. Large voltage vectors are V_{13}, V_{14}, V_{15}, V_{16}, V_{17}, and V_{18}. Medium voltage vectors are V_7, V_8, V_9, V_{10}, V_{11}, and V_{12}. Small voltage vectors are V_1, V_2, V_3, V_4, V_5, and V_6. Zero voltage vector is V_0. Each major sector can be identified by using space vector phase angle. α is calculated and then sector , in which the command vector V* is located , is determined as:

If α is between $0 \le \alpha < 60^0$, and V* will be in major sector I. If α is between $60 \le \alpha < 120^0$, and V* will be in major sector II. If α is between $120 \le \alpha < 180^0$, and V* will be in major sector III. If α is between $180 \le \alpha < 240^0$, and V* will be in major sector IV. If α is between $240 \le \alpha < 300^0$, and V* will be in major sector V. If α is between $300 \le \alpha < 360^0$, and V* will be in major sector VI.

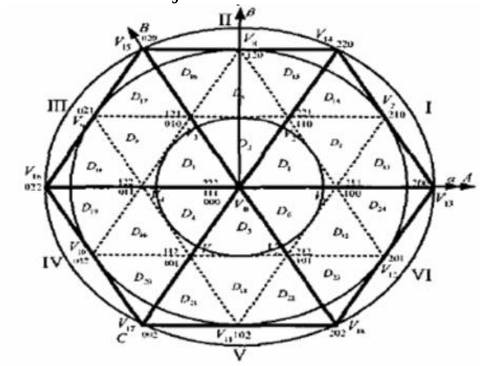


Figure.5 space vector diagram of three level inverter

3.2 DETERMINATION OF REGION IN A PARTICULAR SECTOR

For example we are taking the space vector diagram of sector I for determining the particular region in a sector 1. Sector I contains 4 minor triangular sectors. D_1, D_7, D_{13} and D_{14} are 4 minor triangular sectors. In each of the four minor regions, the reference vector V_{ref} is located in one of the 4 regions, where each region is limited by three adjacent vectors. Then

$V_{ref} = V^* = V_x (T_x/ T_s) + V_y (T_y/ T_s) + V_z (T_z/ T_s)$
$T_x / T_s + T_y/ T_s + T_z/ T_s = 1,$
$T_x / T_s = X$, $T_y/ T_s = Y$ and $T_z/ T_s = Z$
$T_x + T_y + T_z = T_s$

Based on the principle of vector synthesis, the following equations can be written as:
$X + Y + Z = 1$
$V_x X + V_y Y + V_z Z = V^*$
Modulation ratio $M = (V^* / 2/3\ V_{dc}) = (3\ V^* /2\ V_{dc})$

As shown in figure.5, the boundaries of modulation ratio are Mark1, Mark 2, and Mark3.The equation [2] forms of them are obtained as follows:

$$Mark1 = \frac{\sqrt{3}/2}{\sqrt{3}\cos\theta + \sin\theta}$$

$$Mark\ 2 = \frac{\sqrt{3}/2}{\sqrt{3}\cos\ \theta - \sin\ \theta}, \theta \le \pi/6$$

$$= \frac{\sqrt{3}/4}{\sin\ \theta}\ , \frac{\pi}{6} < \theta \le \frac{\pi}{3}$$

$$Mark3 = \frac{\sqrt{3}}{\sqrt{3}\cos\ \theta + \sin\ \theta}$$

3.3 CALCULATION OF ACTIVE VECTOR SWITCHING TIME PERIOD

a) When the modulation ratio M < Mark1, then the rotating voltage vector V* will be in sector D_1 (Region 1). In a three level inverter, switching time calculation is based on the location of reference vector with in a sector. In one sampling interval, the output voltage vector V* can be written

$V^* = V_x (T_x/T_s) + V_y (T_y/T_s) + V_z (T_z/T_s)$.As shown in figure.5 V* is synthesized by V_0, V_1, and V_2. In sector D_1, the length of zero voltage vector V_0 is zero and length of large voltage vector is 1. Then

$V^* T_s = V_1 (T_1/T_s) + V_2 (T_2/T_s) + V_0 (T_0/T_s)$

$V_1 X + V_2 Y + V_0 Z = V^*$ $\quad V^* = M(\cos\theta + j \sin\theta)$,

$V_1 = ½$, $V_2 = ½ (\cos 60^0 + j \sin 60^0)$ and $V_0 = 0$.

$M(\cos\theta + j\sin\theta) = ½ X + ½ (\cos 60^0 + j \sin 60^0) Y$ (1)

$X + Y + Z = 1$

(2) Using (1) & (2), we can obtain X, Y and Z as follows

$$\begin{cases} X = 2m.\left[\cos\theta - \dfrac{\sin\theta}{\sqrt{3}}\right] \\ Y = m.\dfrac{4\sin\theta}{\sqrt{3}} \\ Z = 1 - 2m\left[\cos\theta + \dfrac{\sin\theta}{\sqrt{3}}\right] \end{cases}$$

b) Similarly when the modulation ratio Mark1<M< Mark2, then V* will be in sector D_7 (Region 2). V* can be synthesized by V_1, V_2, and V_7.

$V^* = V_x (T_x/T_s) + V_y (T_y/T_s) + V_z (T_z/T_s)$

In sector D_7, the length of zero voltage vector V_7 is zero, and length of large voltage vector is 1

$V^* T_s = V_1 (T_1/T_s) + V_2 (T_2/T_s) + V_7 (T_7/T_s)$

$V_1 X + V_2 Y + V_7 Z = V^*$ (3)

Using (3) & (2), we can obtain X, Y, and Z as follows

$$\begin{cases} X = 1 - m.\dfrac{4\sin\theta}{\sqrt{3}} \\ Y = 1 - 2m\left[\cos\theta - \dfrac{\sin\theta}{\sqrt{3}}\right] \\ Z = -1 + 2m\left[\cos\theta + \dfrac{\sin\theta}{\sqrt{3}}\right] \end{cases}$$

c) Similarly When the modulation ratio Mark2 < M < Mark3 and 0 <θ < 30 deg, then V* will be in sector D_{13} (Region 3). V_1, V_{13} and V_7 are selected to synthesize V*.

$V^* = V_x (T_x/T_s) + V_y (T_y/T_s) + V_z (T_z/T_s)$

In sector D_7, the length of zero voltage vector V_7 is zero, and length of large voltage vector is 1.

$V^* T_s = V_1 (T_1/T_s) + V_{13} (T_{13}/T_s) + V_7 (T_7/T_s)$

$V_1 X + V_{13} Y + V_7 Z = V^*$ (4)

Using (4) & (2), we can obtain X, Y, and Z as follows

$$\begin{cases} X = -1 + 2m\left[\cos\theta - \dfrac{\sin\theta}{\sqrt{3}}\right] \\ Y = m.\dfrac{4\sin\theta}{\sqrt{3}} \\ Z = 2 - 2m\left[\cos\theta + \dfrac{\sin\theta}{\sqrt{3}}\right] \end{cases}$$

d) When the modulation ratio Mark2 < M < Mark3 and 0 <θ < 30 deg, then V* will be in sector D_{13} (Region 3). V_2, V_7 and V_{14} are selected to synthesize V*.

$V^* = V_x (T_x/T_s) + V_y (T_y/T_s) + V_z (T_z/T_s)$

In sector D_{14}, the length of zero voltage vector V_7 is zero, and length of large voltage vector is 1

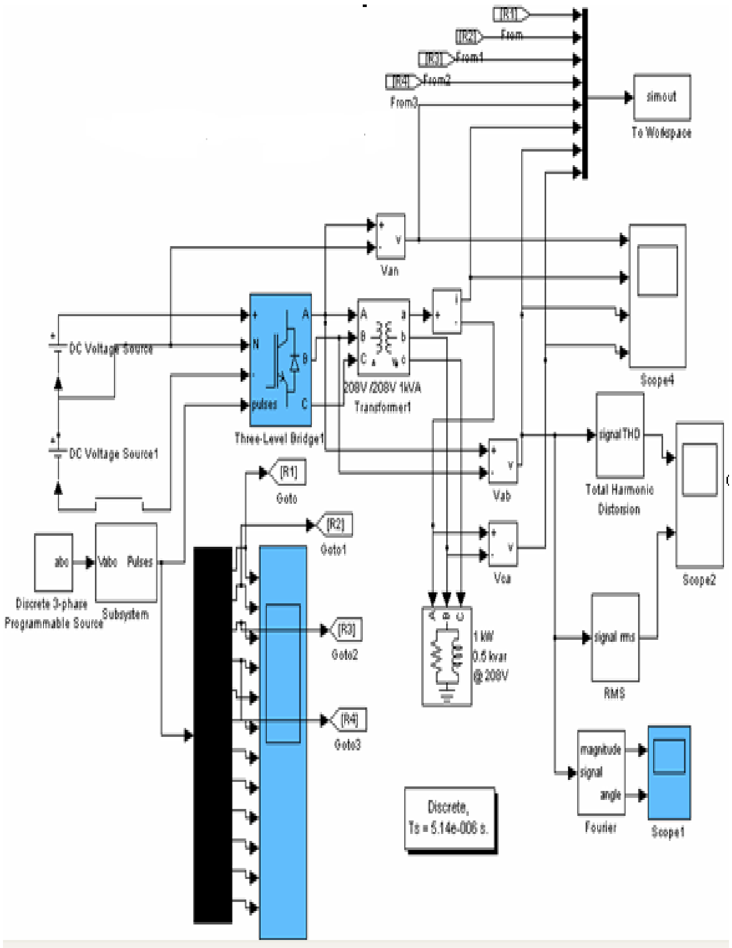
$V^* T_s = V_1 (T_1/T_s) + V_{13} (T_{13}/T_s) + V_7 (T_7/T_s)$

$V_1 X + V_{13} Y + V_7 Z = V^*$ (5)

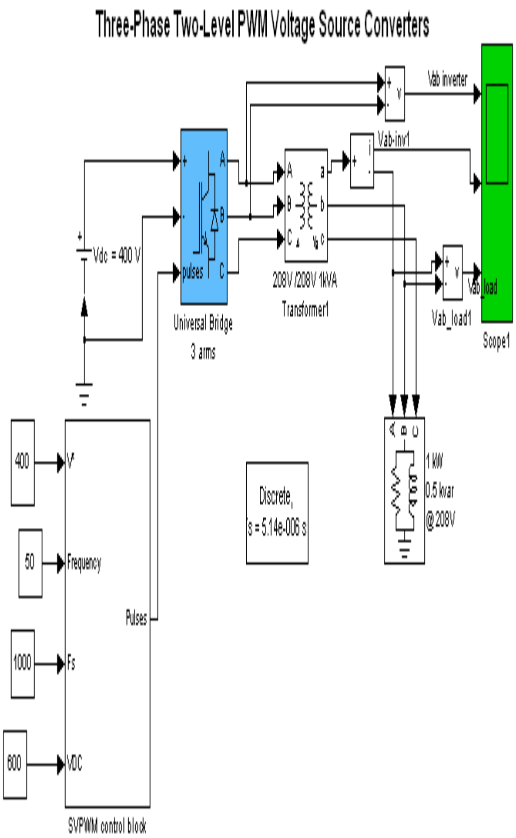
Using (5) & (2), we can obtain X, Y, and Z as follows

$$\begin{cases} X = 2m\left[\cos\theta - \dfrac{\sin\theta}{\sqrt{3}}\right] \\ Y = -1 + m.\dfrac{4\sin\theta}{\sqrt{3}} \\ Z = 2 - 2m\left[\cos\theta + \dfrac{\sin\theta}{\sqrt{3}}\right] \end{cases}$$

IV. SIMULINK MODEL OF THREE LEVEL SVPWM INVERTER



V. SIMULINK MODLE OF TWO LEVEL SVPWM INVERTER



VI. SIMULATION RESULTS

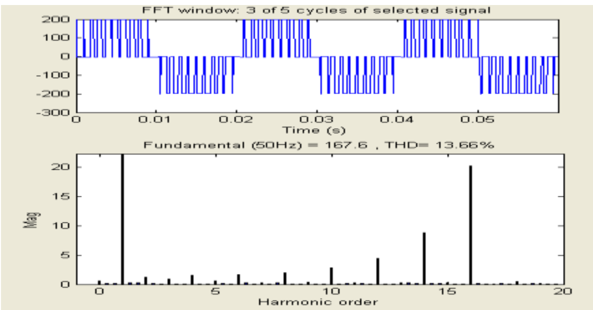


Figure.6THD waveforms of 2 level inverter voltage

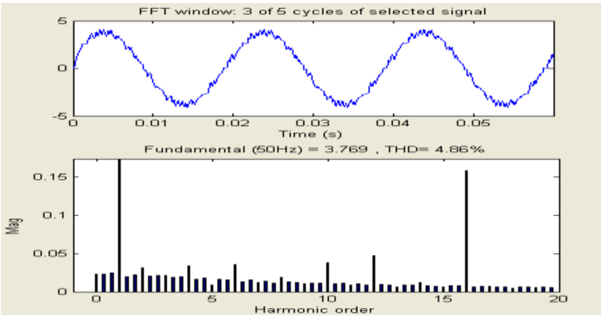


Figure.7 THD waveforms of 2 level inverter current

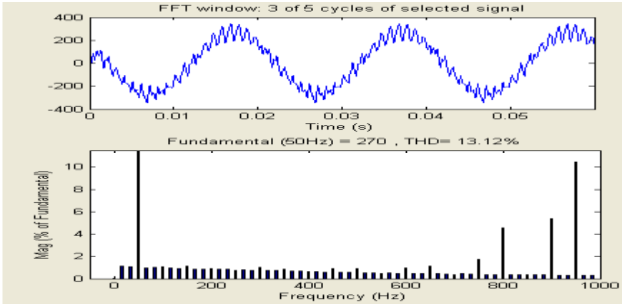


Figure.8 THD waveforms of 2 level inverter load voltage

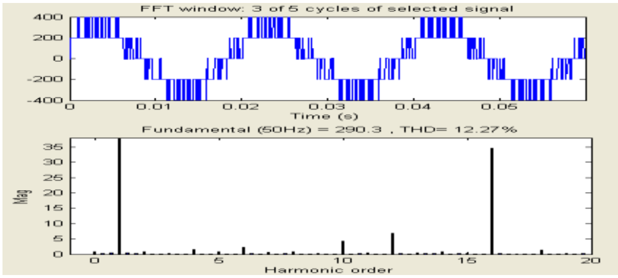


Figure.9 THD waveforms of 3 level inverter voltages

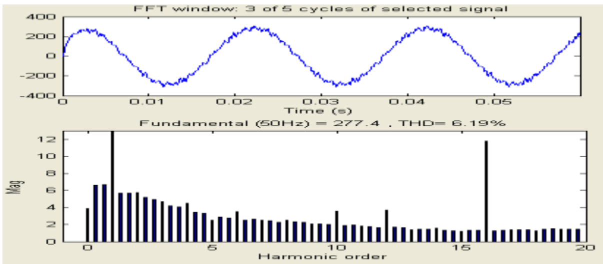


Figure.10THD waveforms of 3 level inverter load voltage

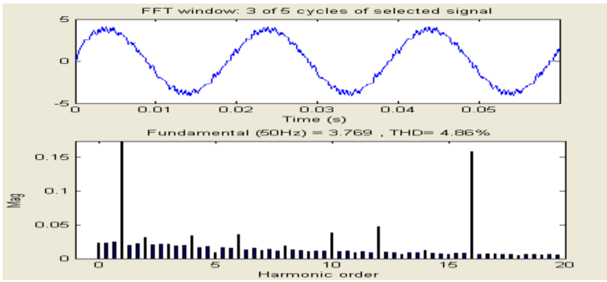


Figure.11 THD waveforms of 3 level inverter current

TABLE.IV
COMPARISION OF 2 LEVEL & 3 LEVEL INVERTERS

Type	V_{ab} inverter	V_{ab} load	Inverter current
TWO LEVEL INVERTER	38.74%	13.12%	11.80%
THREE LEVEL INVERTER	12.27%	6.19%	4.86%

The simulation results suggest that three-level SVPWM can achieve less harmonic distortion compared to two-level SVPWM. And also these results shows that when the number of levels increasing, harmonics are reduced.

VII. CONCLUSION

In this paper, SVPWM technique is used to reduce the harmonics. SVPWM technique has an advantage of fast dynamic response, Easy digital implementation, Lower switching losses, Better harmonic performance. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases significantly. But the main difficulty in this SVPWM is it becomes very difficult when the levels increases and it is complex in some steps that is selection of switching states. A low harmonic content of a proposed 3-level NPC inverter simulation model has been successfully developed with RL load in this paper. The basic implementation is used for future works with high levels that is more than three level inverters. And also the present implementation is used for a new simplified space vector PWM method for three-level inverters.

TABLE.V
SIMULATION PARAMETERS FOR TWO LEVEL & THREE LEVEL SVPWM INVERTER

Input DC link voltage (V_{dc}) for 2 level inverter	400V
Input DC link voltage (V_{dc1}) for 3 level inverter	200V
Input DC link voltage (V_{dc2}) for 3 level inerter	200V
Input voltage (V*) for 2 & 3 level inverter	400V
Fundamental frequency (F) for 2 & 3 level inverter	50HZ
Switching frequency (Fs) for 2 & 3 level inverter	1000hz
Transformer for 2 & 3 level inverter	Ratio on Transformer (208/208V 1KVA)
Three phase ac RL load Active power for 2 & 3 level inverter	1kw
Three phase ac RL load Reactive power	500KVAR

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