RESEARCH ARTICLE OPEN ACCESS

Performance Analysis of Modified CHB Multilevel Inverter using Various Carrier Modulation Schemes

G. Prem Sunder[1], Dr.B.Shanthi[2], Dr.Alamelu Nachiappan[3], Dr.S.P.Natrajan[4]
[1](Associate professor, Department of Electrical and Electronics Engineering, Mailam Engineering College, Mailam, Tamilnadu-604304, India)
[2] (Professor, Centralised Instrumentation and Service Laboratory, Annamalai University, Annamalai Nagar, Tamilnadu-608002, India)
[3] (Professor, Department of Electrical and Electronics Engineering, Pondicherry Engineering College, Pondicherry- 605014, India)
[4] (Professor & Head, Department of Instrumentation Engineering, Annamalai University, Annamalai Nagar, Tamilnadu-608002, India)

ABSTRACT
This paper describes various Carrier Modulation PWM scheme and its performance analysis for nine-level Modified Cascaded H-Bridge Multilevel Inverter (M-CHB-MLI). This M-CHB-MLI topology with a multi conversion cell consists of four equal voltage sources with four controlled switches and four diodes. Instead of 16-controlled switches used in conventional topology for 9-level output voltage, only eight controlled switches are required for 9-level M-CHB-MLI topology which in turn reduces the switches losses and also improves its performance parameters. The various carrier modulation schemes are applied for this M-CHB-MLI to analyze its output voltage harmonics and V_{rms}.
Keywords – Carrier Overlapping Phase Disposition PWM (CO-PD PWM), Carrier Overlapping Phase Opposition Disposition PWM (CO-POD PWM), Carrier Overlapping Alternate Phase Opposition Disposition PWM (CO-APOD PWM), Variable Carrier Frequency PWM (VCF PWM), Modified Cascaded H-Bridge Multilevel Inverter (M-CHB-MLI), Multicarrier sinusoidal PWM.

I. INTRODUCTION

In recent years, the ongoing research in Multilevel Inverter is to further improve its capabilities, to optimize its control techniques and to minimize the device count and thereby reducing the manufacturing cost. Multilevel inverter concept is now incorporated over a wide range of high-power and medium power industrial applications which can be operated at high switching frequencies to produce lower order harmonic components [1].

A multilevel inverter is a power-electronic system that generates a desired output voltage by synthesizing several levels of dc input voltages. The main advantages of multilevel inverters are lower cost, higher performance, less EMI, and lower harmonic content [2]. The most common multilevel inverter topologies are the diode-clamped, flying-capacitor, and cascaded H-bridge inverters with separate dc voltage sources [3]. The cascaded H-bridge multilevel inverters (CHB-MLI) have found wide applications owing to the following advantages of the CHB-MLI first, due to modularity and the ability to operate at higher voltage levels. Second, the increased number of output voltage levels improves the quality of the inverter output voltage waveform which will be closer to a sinusoidal waveform [4]. Moreover, high voltages can be managed at the dc and ac sides of the inverter, while each unit endures only a part of the total amount of dc voltage. The drawbacks of Cascaded H-Bridge inverters are i) Need for high number of semiconductor switches, ii) Involves separate DC source for each H-bridge, iii) DC voltage balance control across all dc capacitors of the H-bridge units [5]. Furthermore, balancing unit's output fundamental voltages and minimizing harmonic distortion level still remain challenging issues [6].

A topology with reduction in number of switches used, will be considered as some form of enhancement in the plant on comparing with the traditional Cascaded H-Bridge inverters, for the same nine level output, in this modified cascaded multilevel inverter topology, the number of switches used reduces from 16 switches to 8 switches. Consequently this Modified cascaded multilevel inverter has value of significance. Hence this paper focuses on analysis and comparison of various parameters like THD & V_{rms} by applying various carrier modulation techniques.

II. MODIFIED CASCADED MULTILEVEL INVERTER TOPOLOGY

The general structure of the Modified cascaded multilevel inverter is shown in Fig. 1.

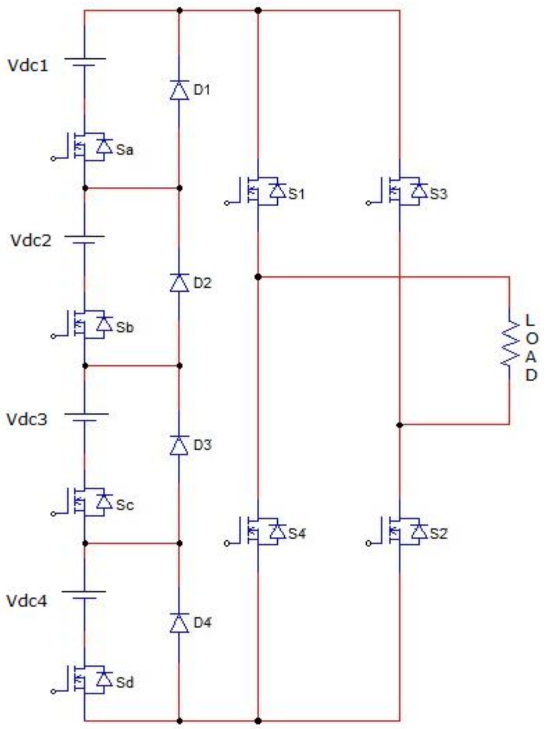

Fig.1 Circuit Diagram of Modified Cascaded H-Bridge Multilevel Inverter (M-CHB-MLI)

This inverter consists of an H Bridge and multi conversion cell which consists of four separate voltage sources (V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4}), four switches and four diodes. Each source connected in cascade with other sources through a circuit consists of one active switch and one diode that can make the output voltage source only in positive polarity with several levels. Only one H-bridge is connected with multi conversion cell to acquire both positive and negative polarity. By turning on controlled switches S1 (S2, S3 and S4 turn off) the output voltage $+1V_{dc}$ (first level) is produced across the load. Similarly turning on of switches S1, S2 (S3 & S4 turn off) $+2V_{dc}$ (second level) output is produced across the load. Similarly $+3V_{dc}$ levels can be achieved by turning on S1, S2, S3 switches (S4 turn off) and $+4V_{dc}$ levels can be attained by turning on S1, S2, S3 & S4 as shown in below Table I.

It is observed that for each voltage level, among the paralleled switches only one switch is switched ON. The input DC voltage is converted into a stepped DC voltage, by the multi conversion cell, which is further processed by the H Bridge and outputted as a stepped or approximately sinusoidal AC waveform. In the H Bridge, during the positive cycle, only the switches Q1 and Q3 are switched on. And during the negative half cycle, only the switches Q2 and Q4 are switched on.

Table I Switching Patterns for 9-level M-CHB-MLI

S. No	Multi Conversion Cell		H-Bridge		Voltage levels
	On switch	Off switch	On switch	Off switch	
1	S1,S2, S3,S4	D1,D2 D3,D4	Q1,Q2	Q3,Q4	$+4V_{dc}$
2	S1,S2, S3,D4	S4,D1, D2,D3	Q1,Q2	Q3,Q4	$+3V_{dc}$
3	S1,S2, D3,D4	S3, S4, D1,D2	Q1,Q2	Q3,Q4	$+2V_{dc}$
4	S1,D2, D3,D4	S2, S3, S4,D1	Q1,Q2	Q3,Q4	$+1V_{dc}$
5	D1,D2, D3,D4	S1, S2, S3,S4	Q1,Q2	Q3,Q4	0
6	S1,D2, D3,D4	S2, S3, S4,D1	Q3,Q4	Q1,Q2	$-1V_{dc}$
7	S1,S2, D3,D4	S3, S4, D1,D2	Q3,Q4	Q1,Q2	$-2V_{dc}$
8	S1,S2, S3,D4	S4,D1, D2,D3	Q3,Q4	Q1,Q2	$-3V_{dc}$
9	S1,S2, S3,S4	D1,D2 D3,D4	Q3,Q4	Q1,Q2	$-4V_{dc}$

The S number of DC sources or stages and the associated number output level can be calculated by using the equation as follows

$N_{level} = 2S+1$ ……………………………….... (1)

For an example, in this topology S=4, the output waveform will have nine levels (±4Vdc ±3Vdc, ±2Vdc, ±1Vdc and 0). Similarly voltage on each stage can be calculated by using the equation as given

$A_i = 1\ V_{dc}\ (1, 2, 3, 4)$ ……………………..….. (2)

The main advantage of proposed modified cascaded multilevel inverter is nine levels with only use of eight switches. The number switches used in this topology is given by the equation as follows

$N_{Switch} = 2S+ 4$ ……………………..…………... (3)

III. MULTIPLE CARRIER PULSE WIDTH MODULATION TECHNIQUES

This paper emphases on applying carrier based PWM techniques to the M-CHB-MLI by using multiple carrier modulation schemes which has more than one carrier that can be triangular wave. The modulating / reference wave can be sinusoidal. For the particular reference wave, there is also multiple Control Freedom Degree including frequency, amplitude, phase angle of the reference wave. Similarly, carrier signal too have multiple Control Freedom Degree including frequency, amplitude, phase of each carrier and offsets between carriers.

In these Multi carrier PWM schemes, several triangular carrier waves are compared with the single Sinusoidal reference wave. The number of carriers required to produce N level output is (m-1) where m is the number of carrier waveforms.

The single sinusoidal reference waveform has peak to peak amplitude of A_m and a frequency f_m. The multiple triangular carrier waves are having same peak to peak amplitude A_c and frequency f_c (4). The single sinusoidal reference signal is continuously compared with all the carrier waveforms. A pulse is generated, whenever the single sinusoidal reference signal is greater than the carrier signal. The frequency ratio m_f is as follows

$M_f = f_c / f_m$ ………………………….……………...(4)

Though there are many carrier wave arrangements, in this paper, the following four arrangements have been carried out. THD and Vrms values for these four strategies for various modulation indexes are compared.

1. Carrier Overlapping Phase Disposition PWM strategy (CO-PD PWM).
2. Carrier Overlapping Phase Opposition Disposition PWM strategy (CO-POD PWM).
3. Carrier Overlapping Alternate Phase Opposition Disposition PWM strategy (CO-APOD PWM).
4. Variable Carrier Frequency PWM strategy (VCF-PWM).

A. Carrier Overlapping Phase Disposition PWM Scheme (CO-PD PWM)

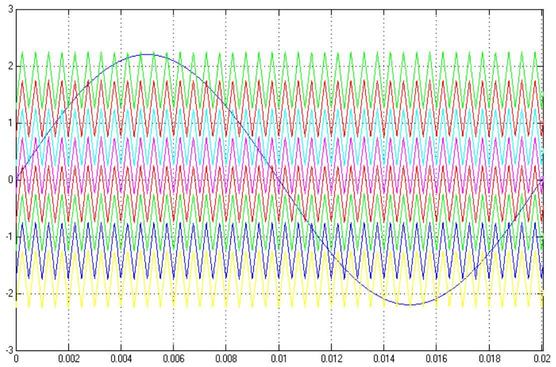

Fig.2 Carrier arrangement for Carrier Overlapping PD PWM strategy

The above Fig. 2 illustrates the Carrier overlapping PD PWM strategy (CO-PD PWM), where the carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlaps each other; the overlapping vertical distance between each carrier is A_c / 2. The reference waveform is centered in the middle of the carrier set. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off. Amplitude modulation index for (CO-PD PWM) is

$m_a = A_m / 2 A_c$…………………………………...(5)

The below Fig. 3 demonstrates the complete switching signal pattern for 9-level M-CHB-MLI using CO-PD PWM scheme.

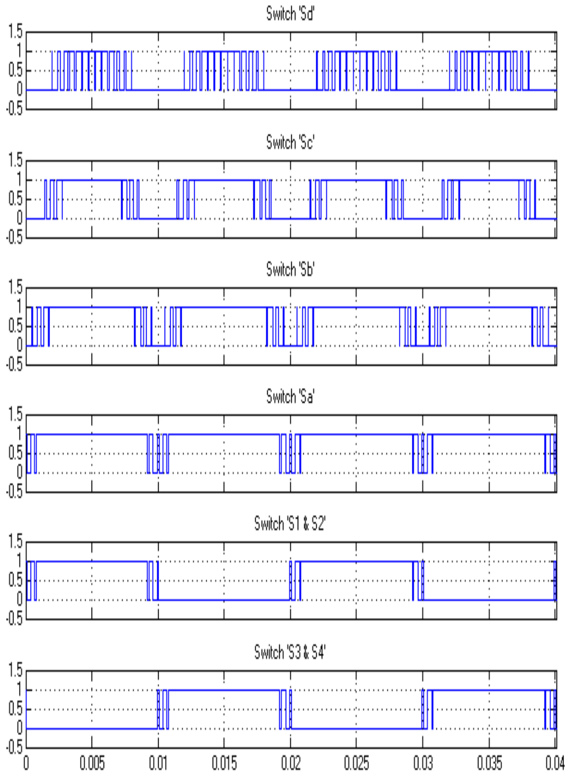

Fig.3 Complete Gate signal for 9-level M-CHB-MLI using Carrier overlapping PD PWM strategy

B. Carrier Overlapping Phase Opposition Disposition PWM Scheme (CO-POD PWM)

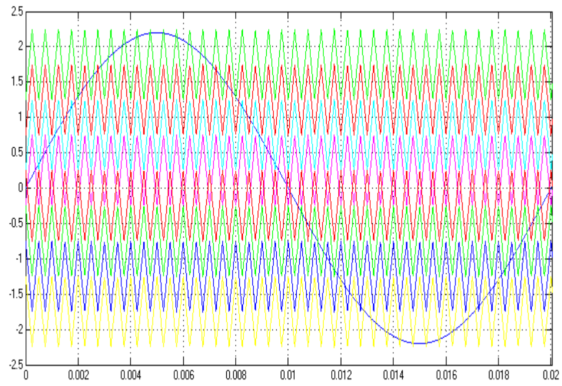

Fig. 4 Carrier arrangement for Carrier Overlapping POD PWM strategy

The above Fig. 4 illustrates the Carrier overlapping POD PWM strategy (CO-POD PWM), where the carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlaps each other; the overlapping vertical distance between each carrier is $A_c/2$.

The reference waveform is centered in the middle of the carrier set. The carrier waveforms above the zero reference are in phase. The carrier waveforms below are also in phase, but are 180 degrees phase shifted from those above zero. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off. Amplitude modulation index for Carrier Overlapping Phase Opposition Disposition PWM Scheme (CO-POD PWM) is

$m_a = A_m / 2 A_c$

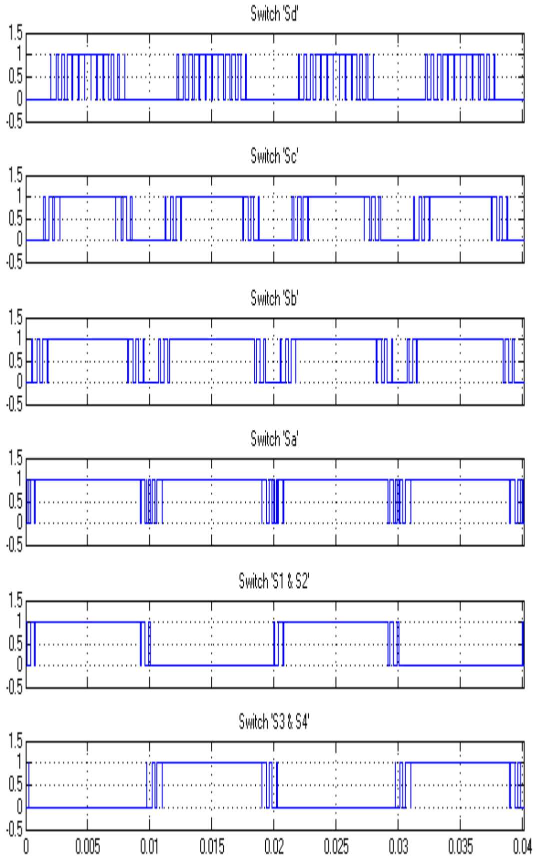

Fig. 5 Complete Gate signal for 9-level M-CHB-MLI using Carrier Overlapping POD PWM strategy

The above Fig. 5 shows Complete Gate signal for 9-level MC-MLI using Carrier overlapping POD PWM strategy.

C. Carrier Overlapping Alternate Phase Opposition Disposition PWM Scheme (CO-APOD-PWM)

The above Fig. 6 shows the Carrier Overlapping – APOD-PWM strategy (CO-APOD PWM), where the carriers with the same frequency f_c and same peak-to-peak amplitude A_c are phase displaced from each other by 180 degrees alternately and disposed such that the bands they occupy overlaps each other; the overlapping vertical distance between each carrier is $A_c/2$.

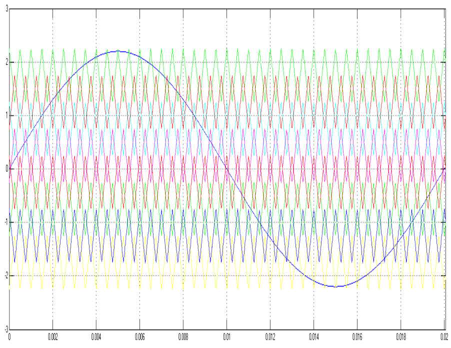

Fig. 6 Carrier arrangement for Carrier overlapping – APOD –PWM strategy

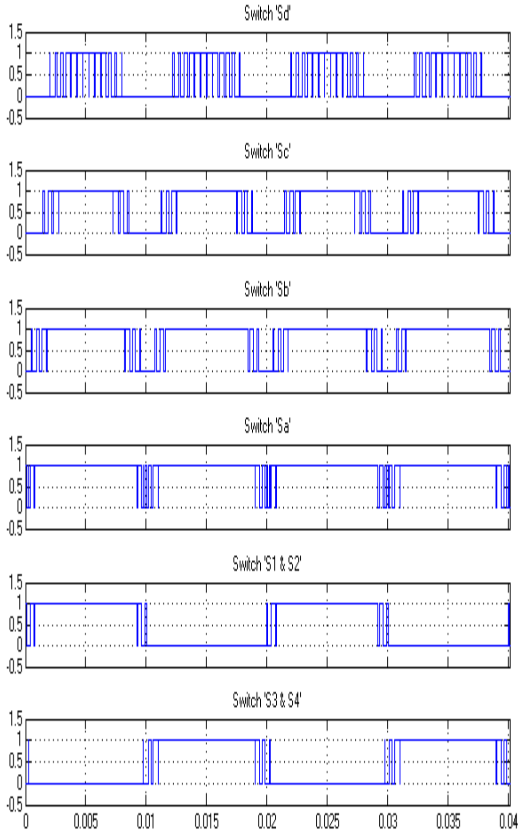

Fig. 7 Complete Gate signal for 9-level M-CHB-MLI using Carrier Overlapping APOD-PWM strategy

The reference waveform is centered in the middle of the carrier set. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off. Amplitude modulation index for (CO-APOD PWM) is $m_a = A_m / 2 A_c$. The above Fig. 7 shows Complete Gate signal for 9-level MC-MLI using Carrier overlapping APOD type PWM strategy

D. Variable Carrier Frequency PWM strategy: (VCF-PWM)

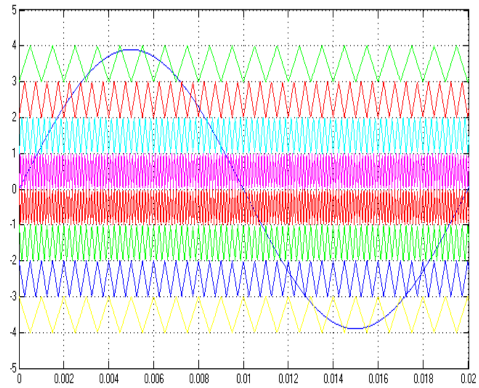

Fig. 8 Carrier arrangement for Variable Carrier Frequency PWM strategy

The above Fig. 8 shows the Variable Carrier Frequency PWM strategy (VCF-PWM). For all PWM using constant frequency carriers, the number of switching operation for upper and lower devices of chosen multilevel inverter is much more than that of intermediate switches.

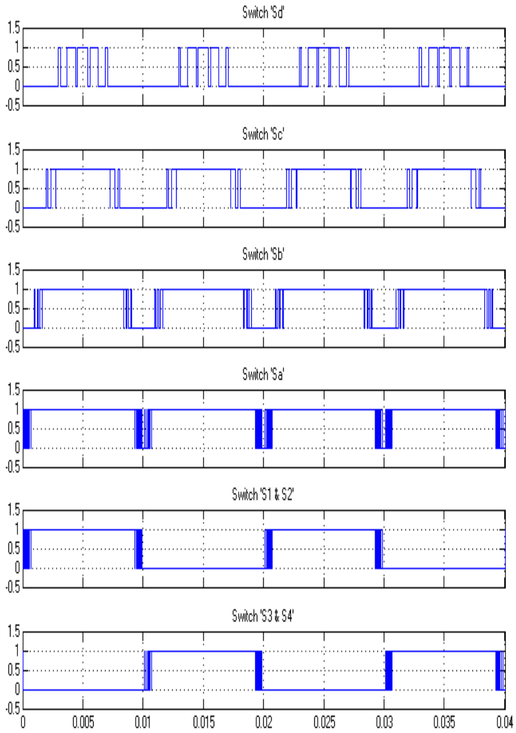

Fig. 9 Complete Gate signal for 9-level M-CHB-MLI using VCF-PWM strategy

In order to equalize the number of switching operation for all the switches, variable frequency PWM strategy is used. The various carrier waveforms are in phase, but their frequencies are different. The carrier waveforms above and below the zero reference are in phase. The above Fig. 9 shows Complete Gate signal for 9-level M-CHB-MLI using VCF-PWM strategy. Amplitude Modulation index for the VCF-PWM is

$m_a = 2A_m / (m-1) A_c$…………………(6)

IV. SIMULATION RESULTS

The Fig. 10 shown below is the simulink model of the 9-level Modified Cascaded H-Bridge Multilevel inverter (M-CHB-MLI). The following parameter values are used for simulation: V1 =100V, V2 =100V, V3 = 100V, V4= 100V, fc=2 KHz and fm=50 Hz. Gating signals for four different multi carrier strategies are simulated for 9-level M-CHB-MLI. Simulations are done for various values of M_a and the corresponding THD are observed using FFT block and listed in Table II. The V_{rms} (fundamental) of the output voltage for various values of M_a and the corresponding Voltages are listed in Table III.

The Simulated 9-level Output Voltage waveform of M-CHB-MLI using CO-PD PWM, CO-POD PWM, CO-APOD PWM and VCF-PWM Strategies are shown in the following Fig. 13 to Fig. 20. The Comparison of THD &V_{rms} for various Multicarrier PWM Techniques is shown in Table II & III.

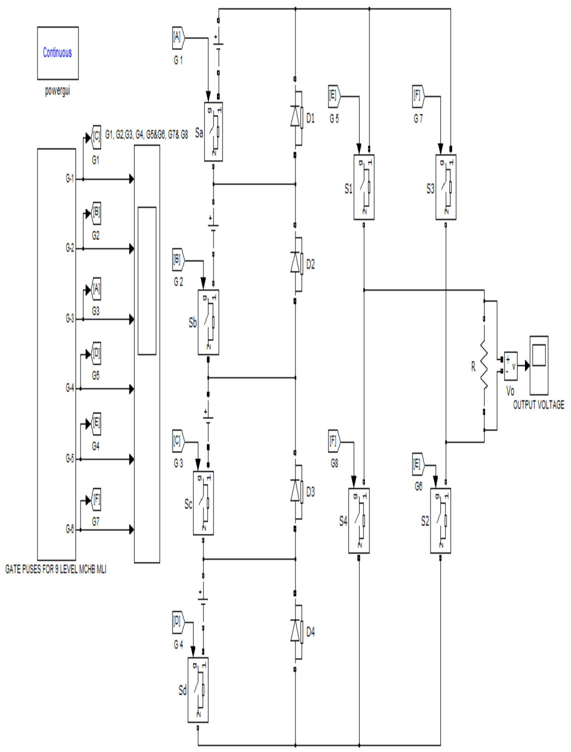

Fig. 10 Simulink Modeling of the 9 level - Modified Cascaded H-Bridge Multilevel Inverter (M-CHB-MLI)

Table II Comparison of THD for various Multi carrier PWM Techniques.

M_a	CO-PD PWM	CO-POD PWM	CO-APOD PWM	VCF-PWM
1	18.52	17.86	13.65	13.83
0.9	21.32	20.80	15.94	16.35
0.8	24.54	23.71	17.67	16.90

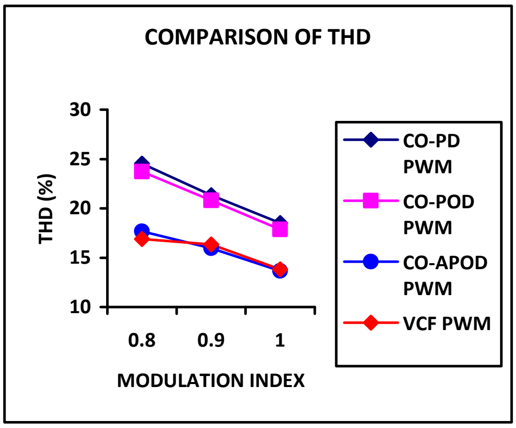

Fig. 11 Comparison of THD

Table III Comparison of V_{rms} for various Multi carrier PWM Techniques

M_a	CO PD PWM	CO POD PWM	CO APOD PWM	VCF PWM
1	421.8	421.9	420.9	400.4
0.9	392.1	392.1	391.2	358.3
0.8	357.7	357.6	356.8	318.3

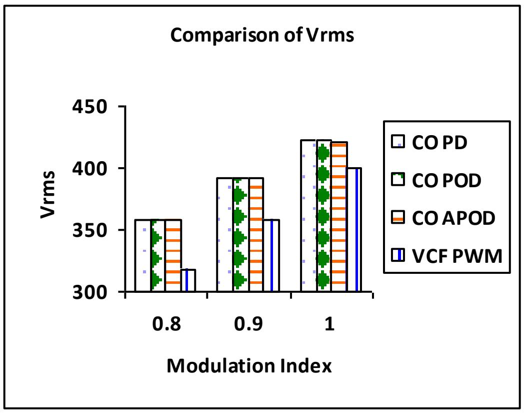

Fig. 12 Comparison of Vrms

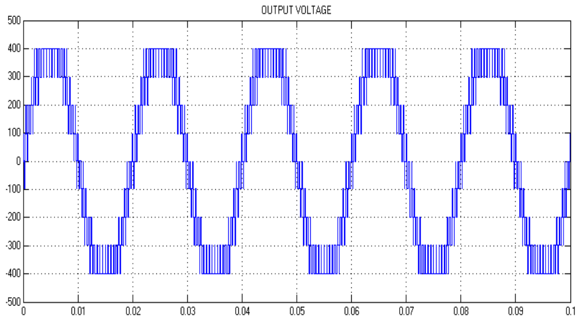

Fig. 13 Simulated 9-level Output Voltage waveform of M-CHB-MLI using CO-PD PWM Strategy

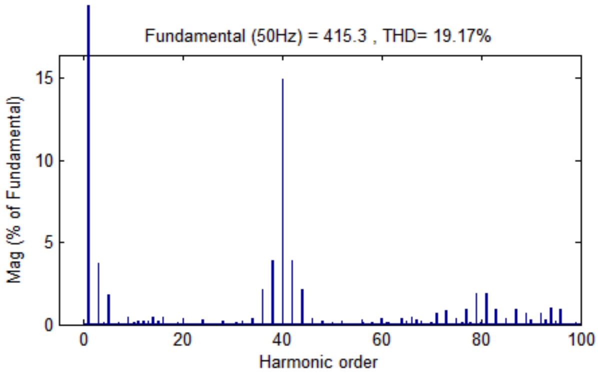

Fig. 14 FFT plot of 9-level M-CHB-MLI using CO-PD PWM strategy

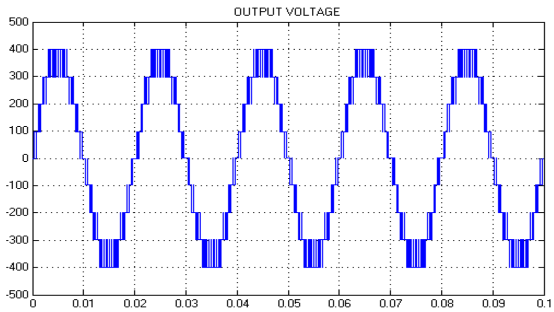

Fig. 15 Simulated 9-level Output Voltage waveform of M-CHB-MLI using CO-POD PWM Strategy

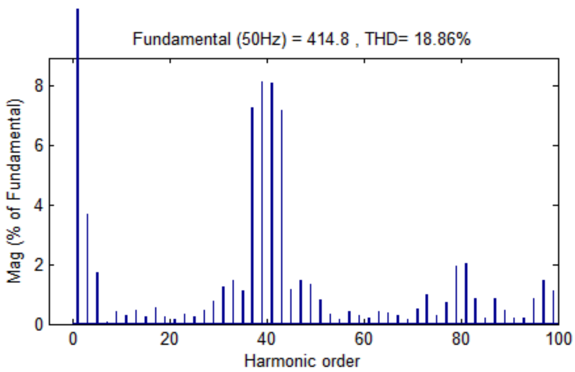

Fig. 16 FFT plot of 9-level M-CHB-MLI using CO-POD PWM Strategy

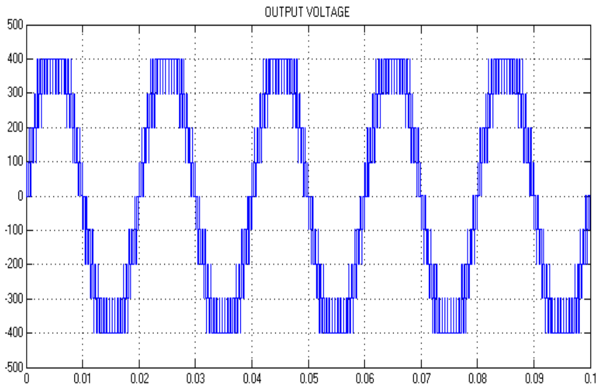

Fig. 17 Simulated 9-level Output Voltage waveform of M-CHB-MLI using CO-APOD PWM Strategy

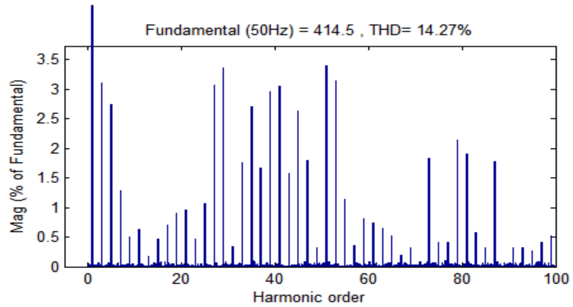

Fig. 18 FFT plot of 9-level M-CHB-MLI using CO-APOD PWM Strategy

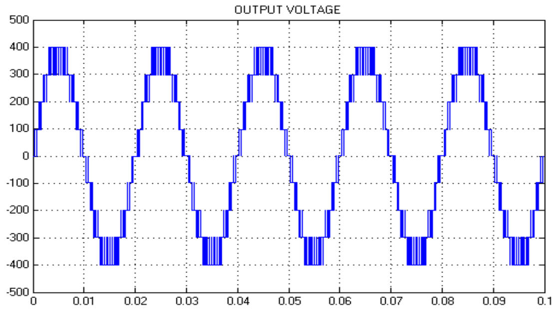

Fig. 19 Simulated 9-level Output Voltage waveform of M-CHB-MLI using VCF PWM Strategy

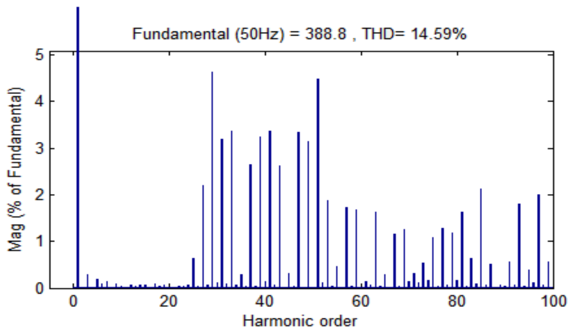

Fig. 20 FFT plot of 9-level MC-MLI using VCF PWM Strategy

V. CONCLUSION

In this paper, Multi Carrier Sinusoidal Pulse Width Modulation strategies for Single phase nine level Modified Cascaded H-Bridge Multilevel Inverter have been presented. Four different carrier wave arrangements have been applied to the Single phase nine levels Modified cascaded multilevel inverter and the performance factors like THD and V_{RMS} have been analyzed and presented. It is inculcated that the Carrier overlapping Alternate Phase Opposition Disposition PWM strategy (CO-APOD-PWM) provides lower THD and higher V_{RMS} with less number of dominant harmonics than the other strategies. This nine level M-CHB-MLI engages only eight switches with four diodes, which eases switching losses, cost and circuit complexity. Moreover it meritoriously diminishes lower order harmonics.

REFERENCES

[1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind.Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.*

[2] Z.Du, L.m.Tolbert, J.N.Chiasson, and B.Opineci, "A cascaded multilevel inverter using a single dc power source", in *Proc. IEEE APEC, pp.426-430, 2006*

[3] Fang Zheng Peng "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", *IEEE Trans. Ind .Appl., Vol.37, No.2, March/April 2001*

[4] J. I. Leon, R. Portillo, S. Vazquez, J. J. Padilla, L. G. Franquelo, and J.M. Carrasco, "Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters," *IEEE Trans.Ind. Electron., vol. 55, no. 9, pp. 3239–3248, Sep. 2008.*

[5] Y. Li and B. Wu, "A novel dc voltage detection technique in the chb inverter-based statcom," *IEEE Trans. Power Del., vol. 23, no. 3, pp.1613–1619, Jul. 2008.*

[6] J. Rodriguez, J. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron, vol.49, no. 4, pp. 724–738, Aug. 2002.*

[7] Ebrahim Babaei "A Cascaded Multilevel converter Topology With Reduced Number of Switches*", IEEE Trans. Power Electron vol.23,no.6, Nov 2008.*

[8] Rokan Ali Ahmed, S. Mekhilef, Hew Wooi Ping, ''New multilevel inverter topology with reduced number of switches'',*Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10), Cairo University, Egypt, December 19-21, 2010, Paper ID 236.*