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Design and Implementation of Robust Router Using Vlsi

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Abstract
In his paper we attempt to give a networking solution by applying VLSI architecture techniques to router design for networking systems to provide intelligent control over the network. Networking routers today have limited input/output configurations, which we attempt to overcome by adopting bridging loops to reduce the latency and security concerns. Other techniques we explore include the use of multiple protocols. We attempt to overcome the security and latency issues with protocol switching technique embedded in the router engine itself. The approach is based on hardware coding to reduce the impact of latency issues as the hardware itself is designed according to the need. We attempt to provide a multipurpose networking router by means of Verilog code, thus we can maintain the same switching speed with more security as we embed the packet storage buffer on chip and generate the code as a self-independent VLSI Based router. Our main focus is the implementation of hardware IP router. The approach enables the router to process multiple incoming IP packets with different versions of protocols simultaneously, e.g. for IPv4 and IPv6. The approach will results in increased switching speed of routing per packet for both current trend protocols, which we believe would result in considerable enhancement in networking systems.

Keywords: *Robust Router, packets, FPGA, RTL, IP*

I. INTRODUCTION

Our approach here is to design a variable hardware router code by using Verilog and the same to be implemented for the SOC (System On Chip) level router. In this paper we are making a VLSI design for the implementation at the synthesizable level the same can be further enhanced to SOC level, but our main aim is limited to the NetList generation level which would give the result prediction and workable module vision. Our focus being in this is to make this router as much variable as we can which will give the robustness for the design to be called even as a Robust Router in which we can make the same router to not only go for N number of connections but also to detect all variety of packets and route the same. To do so we have to add the code with specific case's for every type of packets we want to add to our router to route, with this paper of hardware code our approach is to get the basic packets routing with multiple protocols starting with the IPv4 and IPv6.

II. LITERATURE SURVEY

In this we are comparing the existing generic router architecture and our new robust router architecture. This will give the difference in the designing and would reflect our paper enhancements that we are upgrading in our robust router paper.

A. Generic Router Architecture

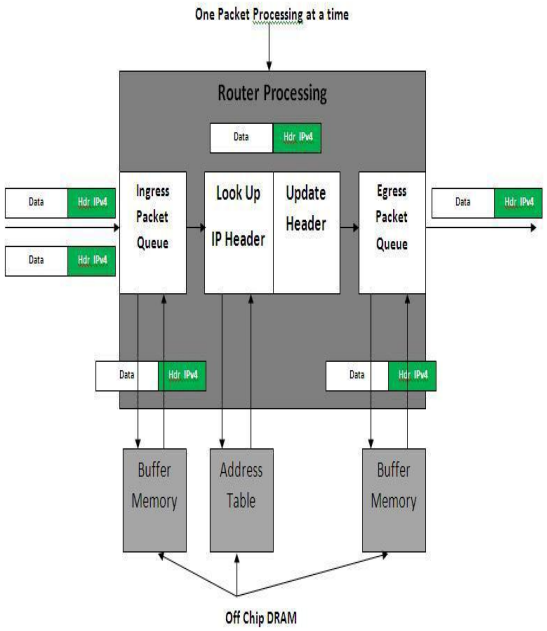

Figure 1 Generic architecture

In the architecture we can look that the generic architecture is processing a single packet of a specific protocol at a given time and the output queue buffer also one for one egress channel ring by which there is the

overloading of the queue buffer and will result in the congestion. The congestion flow is as shown below.

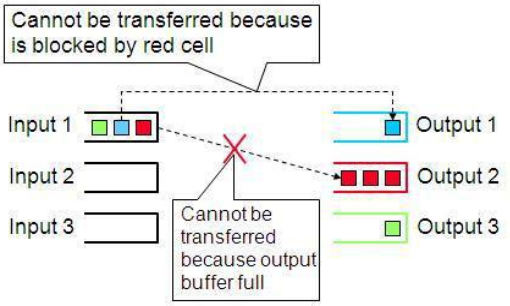

Figure 2 Congestion flow

III. A NEW ROBUST ROUTER ARCHITECTURE

The architecture of robust router is totally based on the Verilog code which would enable our design in the implementation of parallel packet processing for N number of channels. This intern enables the multi packet processing at the same time. With the Verilog code being the base of design we have an option for the addition of protocol case and respective look-up table makes us go for the Multi-protocol processing at the same time. By which we are unable to provide the multi-packet multi-protocol routing at the same time with same speed.

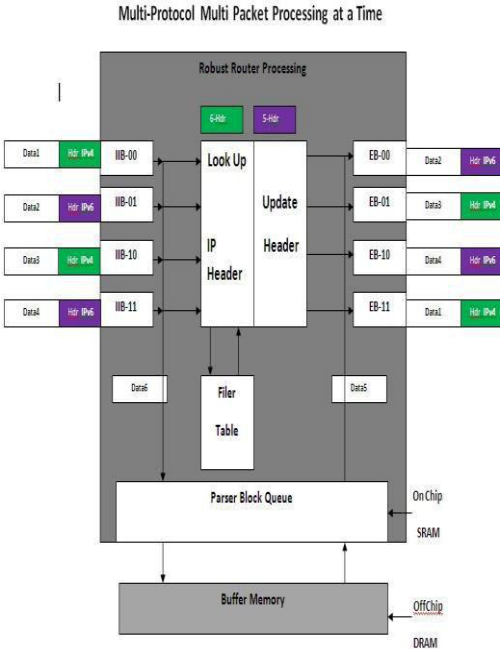

Figure 3 Multi-protocal Multi packet processing at a tree

While designing the robust router a special concern is kept in the mind of the switching speed issue to give the maximum speed with parallelism being added.

The egress output buffer queuing problem was also solved by providing a separate queue for every ingress channel in the egress channel with N vertical queue by which we can avoid the congestion to a remarkable level which is as shown below.

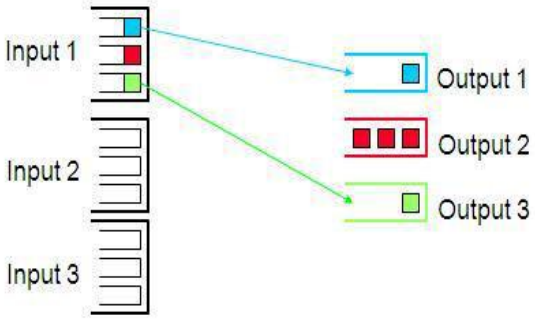

Figure 4 Congestion flow with vertical queue

The size issue is another special feature of our robust router which makes our robust router a unique system. As discussed earlier in the paper we are trying to make the Robust router on to the chip level design so we further advance it to the level of Ethernet based router which will make the router to be implemented on the standalone systems, which will be a revolutionary enhancement in size matter from room full of router to just the PCI slot operating Router and will make network work more faster. It looks something like this below.

Generally, the router can be interfaced with 'N' number of I/O devices. Block diagram given below.

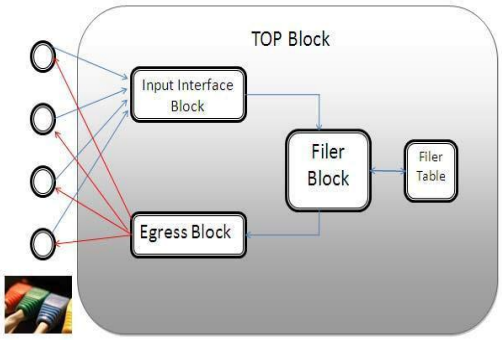

Figure 5 Block diagram

The paper design has the following modules.

A. Input Interface Block

This block is mainly responsible for receiving the incoming IP packets over multiple input channels. This block asserts the necessary response signals in order to communicate with the IP packet driver modules. After receiving the IP packets, this block forward the same to the Ingress Block for the further process. This block forwards the same to packet store block as well as parser block.

B. Packet Store Block

This is responsible for storing the error free received packets. This module receives the packet contents from Ingress block and dispatches the same based on the request from Egress block.

C. Parser Block

This block is mainly responsible for parsing the complete packet into multiple set of data according to its field. The parsed contents will be inputted to the filer block.The above three blocks are merged all together as IIB in code to single file.

D. Filer Block

This block is responsible for selecting the egress ring. The block receives the parsed data from the parser block. The parsed data will be forwarded to the filer table. In response to this, the filer table provides the output ring number. Then, the received output from the filer table will be forwarded to the egress block.

E. Filer Table

It is a user configurable table. This table contains a set of data in its each slot, against which the data sent by the filer block will be compared. If the filer block inputted data matches with the data of any slot of filer table, then that slot's data will be used as egress ring through which received packet will be forwarded.

F. Egress Block

This block receives the data from filer block as egress ring number through which the received packet shall be forwarded. Upon receiving the egress ring number, this block initiates the communication with packet store block to fetch the packet to be forwarded. Then, the fetched IP packet will be forwarded to the output interface block with the output channel details, over which the packet has to be transmitted.

G. Output Interface Block

Upon receiving the packet with output port details from the egress block, this block forwards the IP packet over mentioned output channel. This block is also responsible for asserting all the necessary handshaking signals for the receiving device while transmitting the packets. The Egress Block and Output Interface Block are merged together in code as single file.

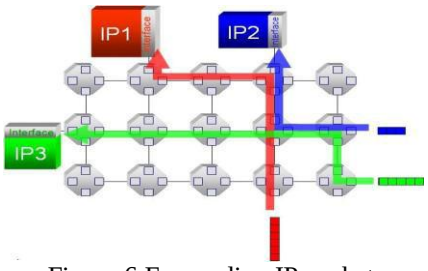

Figure 6 Forwarding IP packet

IV. SYSTEM FLOW DIAGRAM

The system flow diagram is as shown below which makes us to understand the flow of the signals through the system from each block by block and transaction carried between the blocks to accomplish the task of the robust router. The flow diagram described here is a brief one, which helps us to understand the flow of every block. Every block have the state machine cycle included in them to enhance the system logical transaction to the level of parallelism. The flow diagram is as shown in Figure 7 below.

First the packet is received from the ingress channel ring to the input interface block the packet is parsed to data packet and header packet, the data packet is stored in the parser queue and the header is sent to the filer block. The flier block then checks weather the packet is IPv4 or IPv6 and accordingly send the request to the filer table to router the packet to required destination. The filer table cross verifies the egress ring channel with it Dest-IP address and send the egress ring ID to the filer block. The filer block send and enables the particular egress ring in egress blocks and gives the command to the particular egress ring in egress block. Then in egress block the stored data packet in the parser queue is added back with header and is sent out with the specified egress ring channel. In this way the every packet is processed and routed in robust router.

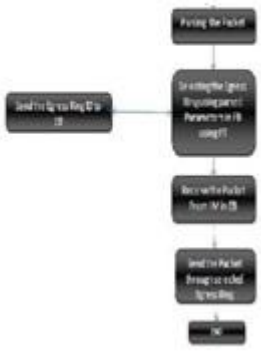

Figure 7 System flow diagram

V. SIMULATION AND DISCUSSION

A. Net List of the Robust Router

The Net List is RTL level of the robust router system, which is syntasizable and can be extracted on the Xilinx tool. By which we can get preface look of the system and a transition from the frontend of the VLSI designing to backend of the VLSI designing. Which means the same can run on FPGA kit and test its robustness and errors of the system can be debugged before it is taken to SOC Level and to Fab-Labs.

The snap below is the Pin configuration of the proposed Robust Router.

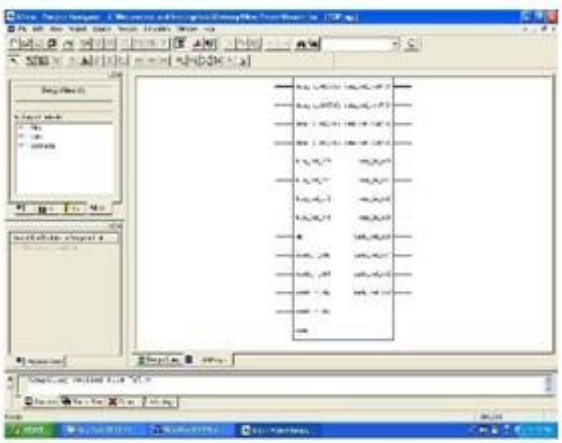

Figure 8 Net List

The NetList level can further go after I/O Padding get the exact pin configuration which can be derived accordingly but will be similar one.
The Snap below is the Top level system view of the system at the RTL.

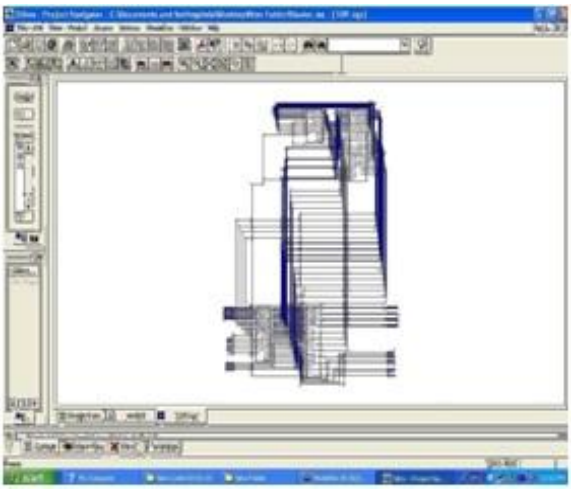

Figure 9 View of the system at the RTL

B.SOC Designing

The further movements of the VLSI Designing will require the sharp knowledge of the VLSI backend designing and can be fabricated at the 45 nano technology using the Cadence Encounter Tool which will enable us to take the system to SOC level the steps are as shown below.

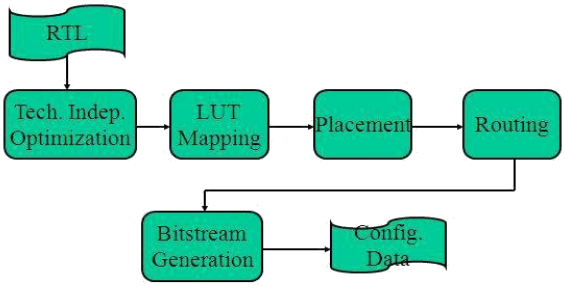

Figure 10 System to SOC level the steps

The RTL level of design which we get from the Net List of the system will have gate delay, propagation delay and wire delays included in them. These are all calculated and made into an optimization level. Then the design is fixed into LUT'S and the mapped between the LUT'S further the placement of the LUT'S are prissily done keeping mind the power utilization and the delay calculated earlier. Then the routing is done between the CLB'S. Further the bit-stream is generated to test the system and verification done across the Net List output to get the exact design. Then the system design is masked and made to the GDSSI Level further to be sent on to the Fab-Labs for fabrication.

C. Design under Test

The design under test [DUT] is made to test the system robustness under different cases. The DUT

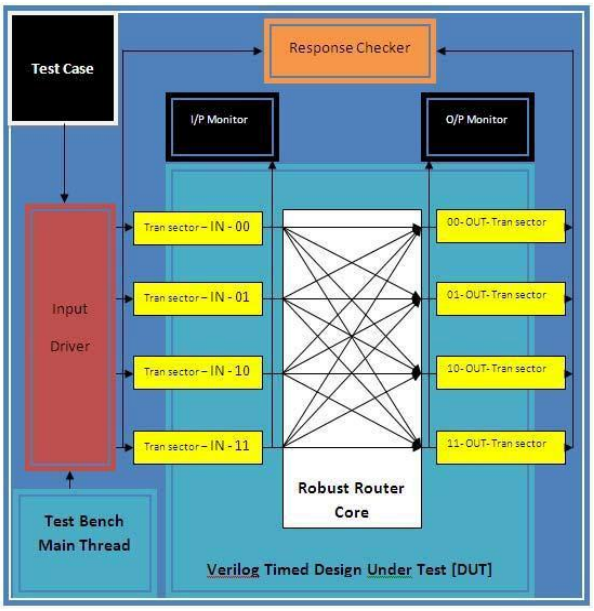

Figure 11 DUT architecture

For the testing of the robustness here we are mixing theIPv4 and IPv6 packets and we testing the system in different cases.

VI. CONCLUSIONS

We summarise the advantages and applications below.

A. Advantages

architecture includes the Test case which will define the test. The input driver block will generate the test input signals for the system testing. The input and output transacted will make the system get the input and output according to the system core requirement. The input and out monitor are placed to compare the system testing. At last the Response checker is to give the system testing pass or fail. The DUT is as shown below.
General purpose router

Router hardware code is variable
More secured
Robust router can handle all type of packets (Implemented on IPv4 and IPv6)

B. Application

Can be used as public internetworking router
Can be used as corporate router
Software company private router (client to client, developer to client)
Router for networking research
In other words one point networking solution

REFERENCES

[1] Y. Katsube, K. Nagami, and H. Esaki, "Toshiba's Router Architecture Extensions for ATM: Overview," IETF RFC2098, April 1997.
[2] Y. Rekhter, B. Davie, D. Katz, E. Rosen, and G. Swallow, "Cisco Systems' Tag Switching Architecture Overview," IETF RFC 2105, Feb. 1997. Amir.Palnitkar. 2nd Edition
[3] J. Moy, OSPF: Anatomy of an Internet Routing Protocol, 1998
[4] Tobias Bjerregaard and Shankar Mahadevan. A survey of research and practices of network-on-chip. ACM Comput. Surv., 38(1):1, 2006.
[5] Charles.H.Roth,Jr Digital System Design Using VHDL
[6] Jenkins,jesse H.Designing with FPGAs and CPLDs
[7] Abromovici,M,Breuer Digital System Testing and Testable Design.
[8] James Balfour and William J. Dally. Design tradeoffs for tiled cmp on-chip networks. In ICS '06: Proceedings of the 20th annual international conference on Supercomputing, pages 187–198, 2006.