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Design and Synthesis of Fault Tolerant Full Adder/Subtractor Using Reversible Logic Gates

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ABSTRACT

Reversible logic is most popular concept in energy efficient computations and this will be demand for upcoming future computing technologies. Reversible logic is emerging as an important research area and it will be having wide applications in many fields such as optical information processing, quantum computing and Low power CMOS design. Under ideal conditions, the reversible logic gates will produce zero power dissipation. So this concept will helpful for Low power VLSI design. This paper will proposes the design of Full adder/subtractor circuit using fault tolerant reversible gates. The design can work singly as an adder/subtractor. The proposed design offers less hardware complexity and is efficient in terms of gate count, delay, constant inputs and garbage outputs compared to previous Fault tolerant Full Adder/Subtractor design. A parallel adder/subtractor design using fault tolerant reversible gates also proposed in this paper. The proposed circuits will be simulated using ModelSim simulator and implemented in Xilinx FPGA platform.

Keywords **–** Adder/Subtractor, Parity preserving reversible gates, Parallel Adder/Subtractor, Reversible logic gates.

I. INTRODUCTION

Today's new technology offers faster, smaller and complex circuits. Moore's law states that Performance (speed) of an integrated circuit per unit cost increased by a factor two for every 18 months. In order to achieve higher speed the clock frequency must be high and for smaller, complex circuit's the number of transistors in the IC must be large and they are more closely packed in order to save area. As the IC will be faster, complex means that will increases the power dissipation in the circuit. Almost all conventional computers comprises of million numbers of gates that are irreversible in nature. During logical operations in the circuit some information is erased or lost that will causes heat dissipation and energy loss.

R Landauer [1] has shown that circuit with irreversible components, during computation each bit loss generates kTln2 joules of energy, where k is Boltzmann's constant and T is absolute temperature. At a temperature T for one bit loss it will generates 2.86×10^{-21} J of energy that will be small but we cannot neglect this value. The heat dissipated in the circuit will gradually decrease the performance and also life span of the circuit or device. In order to overcome these types of problems we require low power consumption and less dissipation components in the circuit. C H Bennet [2] shown that if we use reversible logic gates instead of irreversible components in the circuit, we can achieve zero energy dissipation in the circuit. He proposed two conditions of reversibility.

1st condition: For any device to be reversible if its input and output will be uniquely retrievable from each other called *logical reversibility.*

2nd condition: A device can run actually backwards then it is called *physically reversible.*

The reversible circuits are those in which reversible logic gates are basic building blocks and there is no energy loss. The reversible logic gates will be having n-input and n-output i.e. equal number of input and equal number of output, and also with one-to-one mapping i.e. inputs can be uniquely recovered from the outputs.

II. REVERSIBLE LOGIC GATES

The reversible logic gates will generates unique output vector form unique input vector or vice-versa [3]. In reversible logic Input vector is $I_v=(I_{i,j} , I_{i+1,j} , I_{i+2,j} , \ldots, I_{k-1,j}, I_{k,j})$ and Output vector is $O_v=(O_{i,j} , O_{i+1,j} , O_{i+2,j} ,\ldots, O_{k-1,j}, O_{k,j})$, For each particular vector j $I_v \leftrightarrow O_v$.

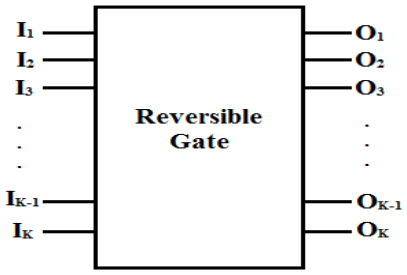
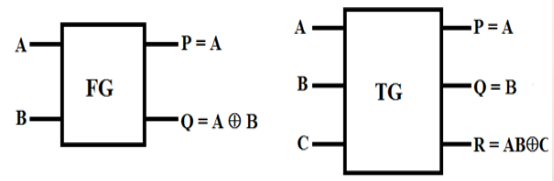


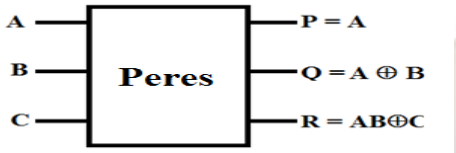
Fig. 1. General Reversible Gate

The Fig. 1 shows General reversible gate the gate will be having **k** inputs and **k** outputs and it is called **k*k** reversible gate [4]. In reversible gates fan out are not permitted, if there it must not exceed more than one. No feedback paths are allowed i.e. circuit is acyclic. Some important factors are Garbage output, constant input etc. Garbage output is the unutilized output from the reversible gate, very much essential to achieve reversibility and it must be not used for further computation. Constant inputs are those that will be added to **k*k** function to make it reversible. For an optimized reversible circuit, the number of garbage outputs, the number of constant inputs and the number of reversible gates used should be a minimum.

There exist several reversible gates; some of the basic reversible gates are 2*2 Feynman [5] gate, Peres gate [6] and Toffoli [7, 8] gate etc. The Fig. 2 shows few basic reversible gates.



(a) Feynman gate (b) Toffoli gate



(c) Peres gate

Fig. 2. Few Basic Reversible Gates

Parity Preserving Reversible Gates:

Fault tolerance is the property that will enables the system to continue its operation properly when failure occurs in any of the component. If the system will be made up using fault tolerant components then the error detection and correction process will much easier. In communication and other systems fault tolerance is achieved by parity. Parity checking is most widely used method for error detection in digital logic circuits. It will most commonly used in arithmetic and other processing systems because those systems do not preserve the parity of the data, there have been attempts at performing arithmetic operations on specially encoded operands in a manner to check the parity. These types of methods will require more development and they are not widely used. B Parhami [9] shown some methods of error detection in reversible circuits, those standard methods of error detection will presents some problems because in reversible logic circuits fan out are not permitted and we have to take care of garbage bits. For parity preserving output data, the data can be checked in manner i.e. in a computational critical path. For parity preserving gate the ex-or of input will matches with the ex-or of output. For a 3*3 reversible gate it will satisfies the condition of $A \oplus B \oplus C = P \oplus Q \oplus R$, where $A \oplus B \oplus C$ is input parity and $P \oplus Q \oplus R$ is output parity. This means that the gate will be parity preserving. Therefore parity preserving circuits will be future design trends to design fault tolerant reversible systems in the field of nanotechnology. Several parity preserving reversible gates are proposed by authors. Few preferable parity preserving gates are as follows:

Feynman Double Gate (F2G):

Fig. 3 shows 3*3 Feynman Double Gate (F2G) [9]. It has A, B and C input vector and output vector as P = A, Q = $A \oplus B$, and R = $A \oplus C$. Quantum cost is equal to 2.

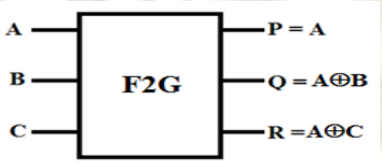


Fig. 3. Feynman Double Gate (F2G)

Fredkin Gate (FRG):

Fig. 4 shows 3*3 Fredkin gate (FRG) [10]. It has A, B and input vector and output vector as P = A, Q= A'B $\oplus$ AC and R = A'C $\oplus$ AB. Quantum cost is equal to 5.

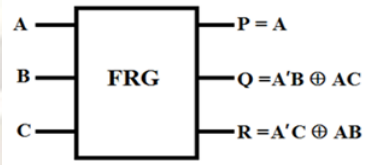


Fig. 4. Fredkin Gate (FRG)

Modified IG Gate (MIG):

Fig. 5 shows 4*4 Modified IG [11] gate. It has A, B, C and D input vector and output vector as P = A, Q = $A \oplus B$, R = AB $\oplus$ C and S = AB' $\oplus$ D.

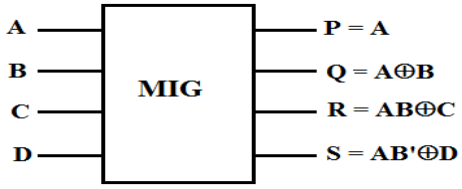


Fig. 5. Modified IG Gate (MIG)

TABLE I, TABLE II and TABLE III shows that the gates Feynman double gate (F2G), Fredkin gate (FRG) and MIG gate are parity preserving respectively.

TABLE I
PARITY PRESERVING FEYNMAN DOUBLE GATE (F2G)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

TABLE II
PARITY PRESERVING FREDKIN GATE (FRG)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

TABLE III
PARITY PRESERVING MODIFIED IG GATE (MIG)

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

III. PROPOSED WORK

We have studied adder design using reversible gates by several authors. Some authors are demonstrated that a reversible adder circuit can be realized with at least two garbage output and one constant input. For designing fault tolerant adder circuits these requirements are not applicable. Because in fault tolerant circuits the input parity must matches with the output parity. In the below section first we discuss fault tolerant half adder/subtractor design [12] and after that fault tolerant full adder/subtractor design [12] because the design full adder requires half adder circuit. This fault tolerant full adder/subtractor block can used to realize other arithmetic circuits such as ripple carry adder, carry look ahead adder, carry skip logic and multiplier/divisors. This paper also proposes the design of parallel adder/subtractor design.

The proposed design will work singly a unit which consists of both adder and subtractor. The design will consists of control line ctrl which will selects adder or subtractor according the control logic input.

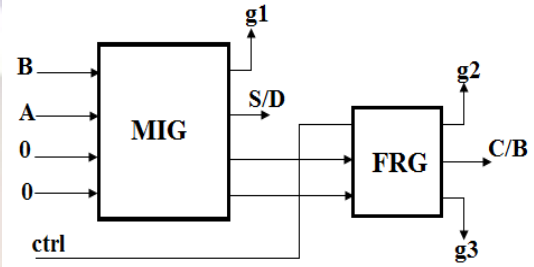


Fig. 6. Reversible Fault Tolerant Half Adder/Subtractor circuit

The fault tolerant half adder/ subtractor is realized using one Modified IG (MIG) gate and one Fredkin gate (FRG) shown in Fig. 6. The design will be having two inputs A & B and a control line ctrl which will controls mode of operation i.e. when ctrl is at logic 0, the circuit will acts as half adder and when ctrl is at logic 1, the circuit will acts as half subtractor. The S/D in Fig. 6 represent sum & difference line .The C/B in Fig. 6 represents carry & borrow line.

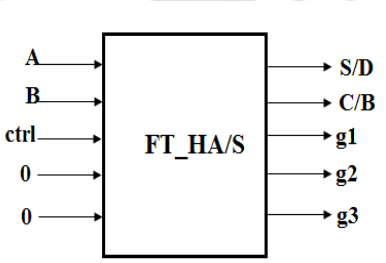


Fig. 7. Fault Tolerant Half Adder/Subtractor circuit (FTHA_S)

The Fig. 7 represents the Fault Tolerant Half Adder/Subtractor (FT_HA/S) circuit with two constant inputs are forced at logic 0 and three garbage bits g1 to g3.

As per conventional approach for designing reversible full adder it requires two half adders. So the fault tolerant reversible full adder/subtractor (FT_FA/S) circuit is built using two fault tolerant half adder/subtractor (FT_HA/S) circuits. The fault tolerant Full adder/ subtractor is realized using Two Modified IG (MIG) gate, two Fredkin gate (FRG) and one Feynman double gate (F2G) is shown in

Fig. 8. The circuit will be having three inputs A, B & C_{in} (For full subtractor A, B & B_{in} are inputs) and a control line ctrl which will controls mode of operation i.e. when ctrl is at logic 0, the circuit will acts as full adder and when ctrl is at logic 1, the circuit will acts as full subtractor.

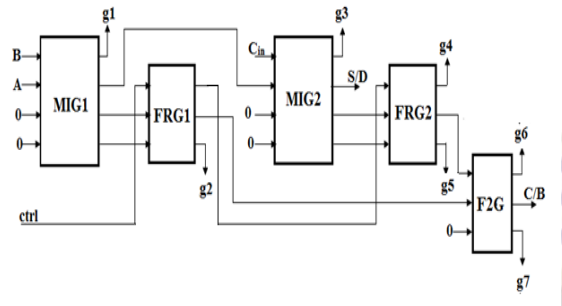


Fig. 8. Reversible Fault Tolerant Full Adder/Subtractor circuit

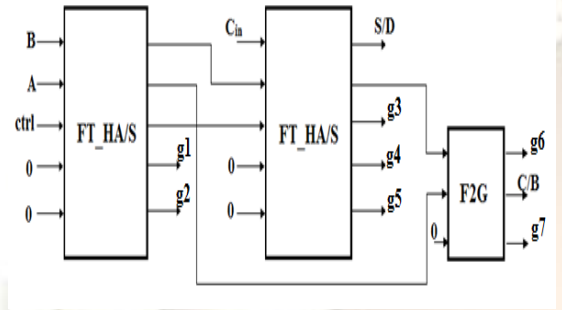


Fig. 9. Fault Tolerant Full Adder/Subtractor circuit (FT_FA/S)

The Fig. 9 represents the Fault Tolerant Full Adder/Subtractor (FT_FA/S) circuit with Five constant inputs are forced at logic 0 and Seven garbage bits g1 to g7.

Parallel Adder/Subtractor:

The n-bit Parallel adder/subtractor can be realized by cascading n number of full adder/subtractor. The carry/borrow from one full adder/subtractor will be propagated to the next full adder/subtractor. In this type of adder/subtractor the inputs are presented simultaneously (parallel) therefore these adder/subtractor arte called Parallel Adder/Subtractor.

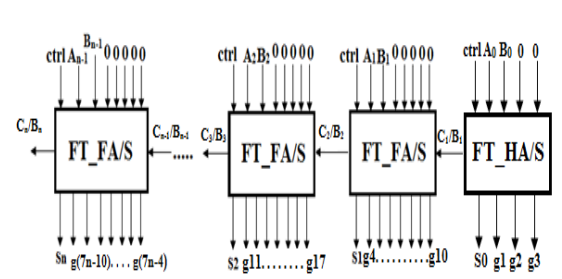


Fig. 10. Reversible Fault Tolerant n bit Parallel Adder/Subtractor

The Fig. 10 shows fault tolerant n-bit parallel adder/subtractor with a control line ctrl that will controls the mode of operation i.e. when ctrl is at logic 0, the circuit will acts as parallel adder and when ctrl is at logic 1, the circuit will acts as parallel subtractor.

IV. RESULTS

The entire architecture is modelled using Verilog. The coding is done on Xilinx ISE13.2 on Spartan 3 using target device: XC3S50-PQ208 at speed grade of -5. Simulation can be done using ModelSim SE 6.3f simulator. The simulation result for FT_HA/S is shown on Fig. 11 & Fig. 12 and FT_FA/S is shown on Fig. 13 & Fig. 14 and Parallel Adder/Subtractor is shown on Fig. 15 & Fig. 16 respectively.

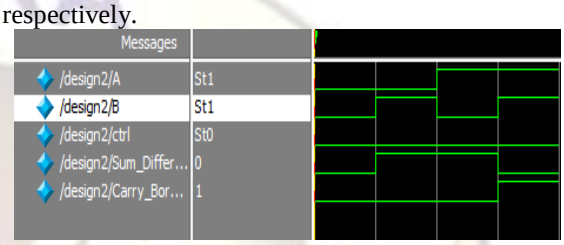


Fig. 11. Simulation result of Fault Tolerant Half Adder/Subtractor when ctrl=0 (acts as Half Adder)

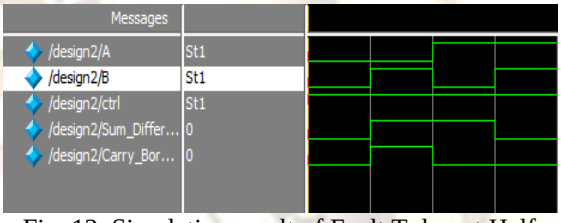


Fig. 12. Simulation result of Fault Tolerant Half Adder/Subtractor when ctrl=1(acts as Half Subtractor)

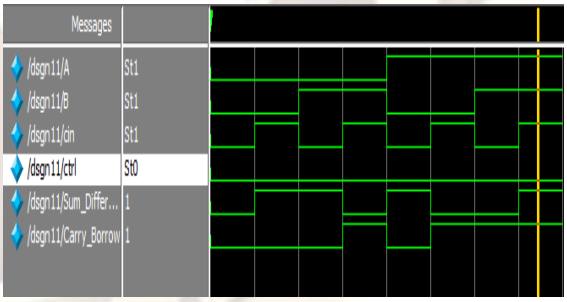


Fig. 13. Simulation result of Fault Tolerant Full Adder/Subtractor when ctrl=0 (acts as Full Adder)

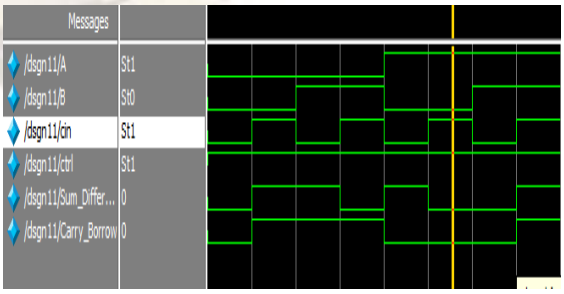


Fig. 14. Simulation result of Fault Tolerant Full Adder/Subtractor when ctrl=1 (acts as Full Subtractor)

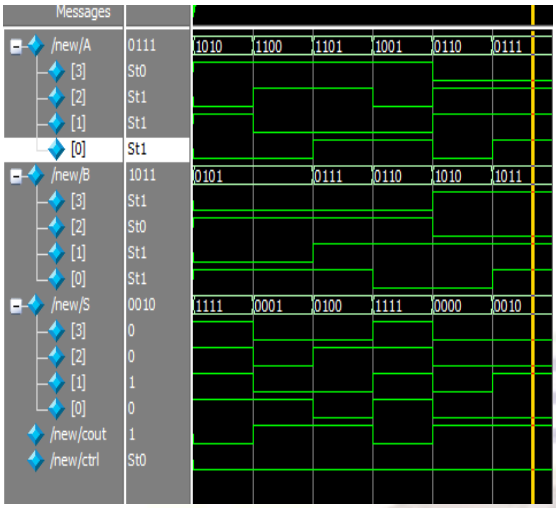


Fig. 15. Simulation result of Fault Tolerant 4-Bit Parallel Adder/Subtractor when ctrl=0 (acts as Parallel Adder)

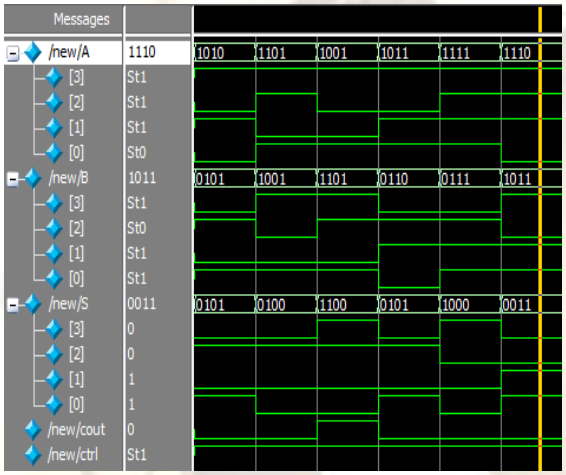


Fig. 16. Simulation result of Fault Tolerant 4-Bit Parallel Adder/Subtractor when ctrl=1 (acts as Parallel Subtractor)

The TABLE IV and TABLE V shows the comparative results of different Fault Tolerant Full Adder/Subtractor and Fault Tolerant Parallel Adder/Subtractor.

TABLE IV
COMPARATIVE RESULTS OF DIFFERENT FAULT TOLERANT FULL ADDERS/SUBTRACTORS

	No. Of gates	No. of Constant Inputs	No. of Garbage Bits
Existing Work [12]	5 F2G's & 4 FRG's = 9	9	11
This Study	2 MIG's, 2 FRG's & 1 F2G = 5	5	7
Percentage Reduction	44.45%	44.45%	36.36%

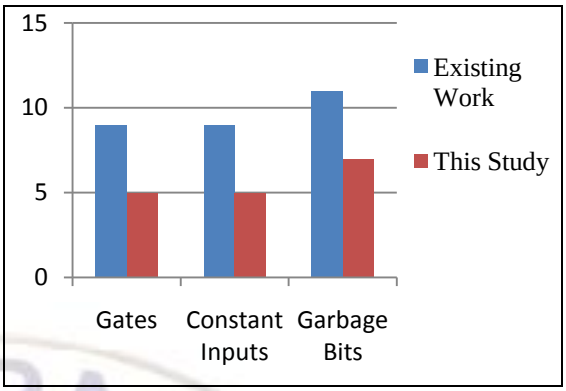


Fig. 17. Graphical representation of comparison of two design works of Fault Tolerant Full Adder/Subtractor

TABLE V
COMPARATIVE RESULTS OF DIFFERENT FAULT TOLERANT 4- BIT PARALLEL ADDERS/SUBTRACTORS

	No. Of gates	No. of Constant Inputs	No. of Garbage Bits
Existing Work [12]	17 F2G's & 14 FRG's = 31	31	38
This Study	7 MIG's, 7 FRG's & 3 F2G = 17	17	24
Percentage Reduction	45.16%	45.16%	36.84%

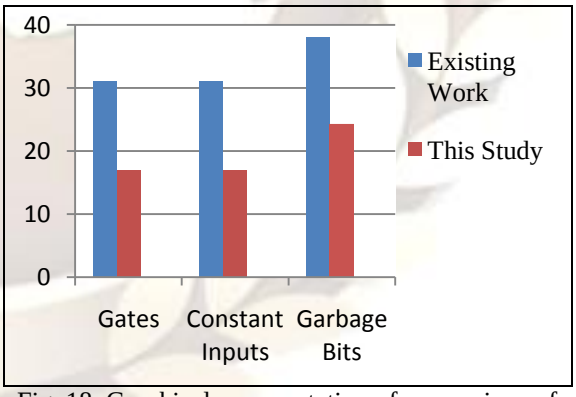


Fig. 18. Graphical representation of comparison of two design works of Fault Tolerant 4-bit Parallel Adder/Subtractor

V. APPLICATIONS

The reversible logic will have many applications. Some important areas of reversible logic include the following [13, 14]

- Nanocomputing
- Bio Molecular Computations
- Laptop/Handheld/Wearable Computers
- Spacecraft

- Low power CMOS.
- Design of low power arithmetic and data path for digital signal processing (DSP).

VI. CONCLUSION AND FUTURE WORK

This paper presents efficient approach for the design of fault tolerant full adder/subtractor and parallel adder/subtractor. The proposed design can work as single unit that can acts as adder as well as subtractor depending upon our requirement. The proposed design offers less hardware complexity, less gate count, less garbage bits and constant inputs. The reversible computation can be done efficiently with less number of garbage bits and constant inputs. The proposed Fault tolerant Adder/Subtractor design can be used to realize some arithmetic components such as carry save adder, carry skip adder and multiplier/divisors etc,. In future we are planning to design more optimized Fault tolerant Adder/Subtractor design and other fault tolerant circuits i.e. less garbage bits and constant input.

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