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Single Event Upset (SEU) in SRAM

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ABSTRACT

Radiation in space is potentially hazardous to microelectronic circuits and systems such as spacecraft electronics. Transient effects on circuits and systems from high energetic particles can interrupt electronics operation or crash the systems. This phenomenon is particularly serious in complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) since most of modern ICs are implemented with CMOS technologies. The problem is getting worse with the technology scaling down. Radiation-hardening-by-design (RHBD) is a popular method to build CMOS devices and systems meeting performance criteria in radiation environment. Single-event transient (SET) effects in digital circuits have been studied extensively in the radiation effect community.

The goal of this research is the implementation of a radiation hardened MOS devices using ORCAD that is able to accurately compute in the presence of radiation induced SEUs. This research specifically concentrates on the ability of the system to detect and mark or correct SEUs in semiconductor memory systems. This work does not address error detection and correction (EDAC) of memory systems. It only address the areas where fault can be likely found in MOS based devices and then make a circuit which perfectly work in radiation environment too.

Keywords- linear energy transfer (LET), single event upset (SEU), single event error (SEE), single event transient (SET)

I. INTRODUCTION

In microelectronics, Single-event effects can cause changes in memory state in space borne, airborne, and even terrestrial electronics. They are result of charge collection from a radiation particle strike. Since the sensitivity of microelectronics to single-event upset is expected to increase as technology scaling continues, therefore single event effects are a severe problem nowadays. In complementary metal-oxide-semiconductor (CMOS) transistor technology, single event effects are a key of research interest. As devices are downscaled, a reduction in the amount of charge held on memory storage nodes increases CMOS vulnerability to single-event upset.

Single Event Effects (SEE) are caused by the interaction of ionizing particles with semiconductor devices. The passing of an ionizing particle through a semiconductor device generates electron-hole pairs (ehps) along the track path and may be collected at the terminals of a device. Linear Energy Transfer (LET) is defined as the energy loss per unit path length, normalized by the density of the material. LET has units of MeV/mg/cm^2. A calculation of the charge deposited per unit length can be determined if the LET of the ion, average energy needed to create an ehp for a material, and density of the material are known [1]. For silicon, an ion with a LET of 97 MeV/mg/cm$_2$ will deposit 1pC of charge per micron length of the ion track [2].

The charge collection process in semiconductor devices normally occur in reversed biased p/n junctions due to the presence of the high electric field in the reverse-biased junction depletion region (drift collection). Diffusion collection process is due to the presence of carriers outside of the depletion region that can diffuse back toward the junction. Bipolar amplification process is another collection mechanism. This collection mechanism is due to a lowering of the body potential and turns-on of a parasitic bipolar transistor for CMOS submicron technologies [3] Single Event Upsets (SEU) occur when the SEE leads to a logic gate switch, voltage transients, or alteration of stored information. The first reported instance of SEU was in 1975 by Binder, et al [4].

SEUs don't just happen in deep space or when high levels of radiation are present. The same cosmic rays that warm the earth's atmosphere carry energetic particles that cause upsets in earth-based equipment. In 1979, James Ziegler of IBM and W.A. Lanford first described how terrestrial cosmic rays could cause single event upsets in electronics. Over the next 15 years, IBM, led by Ziegler, continued to study SEUs, finding that while the rate of upset decreases as altitudes approach sea level, on average, every device – such as an image (memory cell) in a digital camera – experiences an SEU approximately once a year. Because this is the average, it's reasonable to expect that some cameras may experience no upsets in a one year period while others may experience multiple instances. In addition to IBM, other companies including Motorola have studied SEUs extensively. Their findings have determined additional causes of upsets here on Earth, such as power glitches, Alpha particles, impurities in chips, software bugs, product quality. The number of upsets has been found to increase as the amount of

storage capacity of the affected devices increases. Therefore, as memory capacities have multiplied significantly over the years, the number of SEUs in those devices has also increased .

II. SENSITIVE NODES

In CMOS circuits, the "off" transistors struck by a heavy ion in the junction area are most sensitive to single event upset (SEU) by particles with high enough LET (linear energy transfer) of around 20 MeV-cm^2/mg. which is shown in (fig 1).

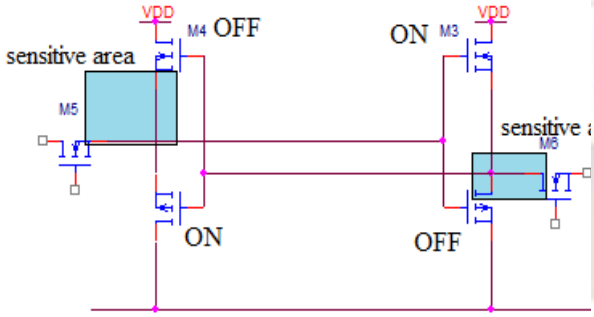


Figure 1: Diagram of critical nodes within an FPGA circuit [6].

When these particles hit the silicon bulk, the minority carriers are created and if collected by the source drain diffusion regions, the change of the voltage value of those nodes occurs. The induced transient voltage pulse may propagate through several of logic gates. Because a particle can induce an SEU when it strikes either the channel region of an off NMOS transistor or the drain region of an off PMOS transistor, we will consider the strike at an off PMOS drain area.

A particles can induce SEU when it strikes at the channel region of an off NMOS transistor or the drain region of an off PMOS transistor. The ionization can induce a current pulse in a p-n junction. A schematic view of how the SEE induced current pulse translate into an SEE induced voltage pulse is given in figure1.

The amount of charge deposited per unit time is therefore quantified as the linear energy transfer (LET). As the amount of charge deposited by a radiation strike is directly proportional to the Let (L) and charge collection depth (t) which is seen in the following equation.

Q=0.01036.L.t (1)

Here L is expressed in MeV-cm^2/mg, t in microns, and Q in pC. For example, an alpha particle with 5 MeV-cm^2/mg LET deposits around 50fC/µm [3]. The minimum amount of deposited charge that is required to cause an SEU is defined as critical charge (Q_{crit}). Additionally, the probability distribution of energetic particles drops off rapidly with increasing LETs [6]. The largest population of particles have an LET of 20MeV-cm^2/mg or less, and particles with an LET greater than 30MeV-cm^2/mg are exceedingly rare [4]. The current pulse that results from a particles strike is traditionally describe as a double exponential function. The radiation particles strike is modeled by

current pulse as

$$I_{seu}(t) = \frac{Q}{\tau_\alpha - \tau_\beta}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (2)$$

Here Q is the amount of charge collected as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment constant. Time constant τ_α and τ_β depends upon several process related parameters, and typically τ_α is on the order of 100ps and τ_β is on the order of tens of picoseconds. In our experiments, we have used Q=150pC, τ_α=150ps and τ_β=38ps. The radiation induced current always flows from n-diffusion to p-diffusion.

Single event upsets are events in which an incident particle can strike key node within a device (Fig2)

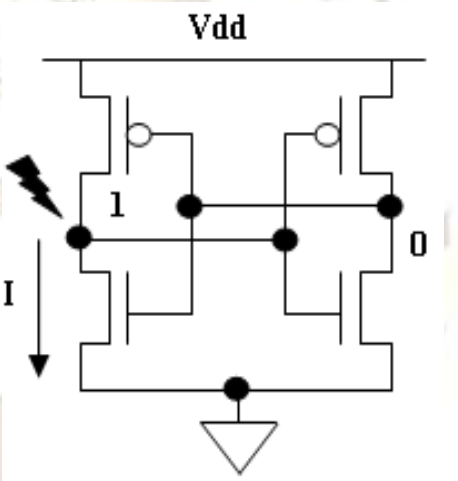


Figure 2: SEU in memory cell due to a heavy ion strike.

resulting in a local ionization that can cause a state change in a bit with sufficient voltage [3]. Experiments with similar device types have shown that the minimum free charge required to change the state of a logic cell is approximately 100 fC. Given that the average energy to create an electron-hole pair in the Silicon is 3.6 eV and the average thickness of an active volume of a device is on the order of 2 µm, an ionization of 1 MeV µm is required - well beyond the average ionizing energy loss of protons (where dE dX ≈ 40keV µm at an energy of 1 MeV) [20]. Thus, upsets are associated primarily with ion strikes in the Silicon which result in the creation of heavier secondary fragments such as (Figure 3.1) and through elastic collisions with the Silicon nuclei (Figure 3.2) which result in nuclear "recoils", leaving a local trail of heavy ionization [3, 4]. Experimental testing by Xilinx at Texas A&M University with their radiation-tolerant devices has yielded SEU (and other

fault condition) cross-sections for configuration logic bits for protons and heavy ions [4].

Electron-hole pair is generated when radiation is incident on silicon substrate as shown in figure and SEU effect is induces in the device.

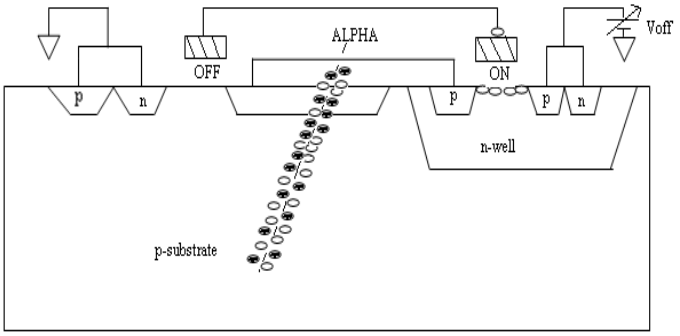
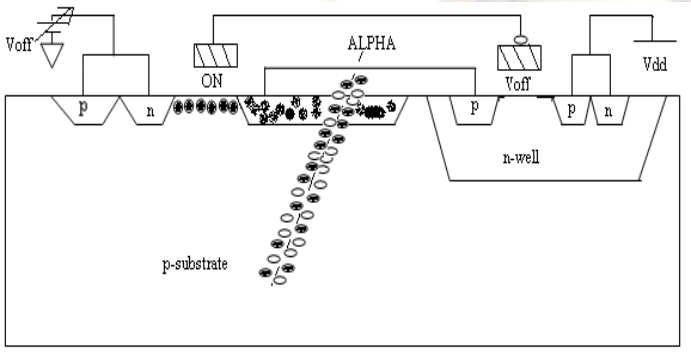


Figure (3.1)



Figure(3.2)

Figure 3: Electron –hole pair tracks from an alpha particles strike through (3.1) an n^+ in P-substrate junction, and through (3.2) a p^+ in n-well junction where truncation of the collected charge occurs.

In CMOS circuits, the "off" transistors struck by a heavy ion in the junction area are most sensitive to SEU by particles with high enough LET (linear energy transfer) of around 20 MeV-cm^2/mg. When these particles hit the silicon bulk, the minority carriers are created and if collected by the source/drain diffusion regions, the change of the voltage value of those nodes occurs. The induced transient voltage pulse may propagate through several levels of logic gates [6]. Because a particle can induce an SEU when it strikes either the channel region of an off NMOS transistor or the drain region of an off PMOS transistor, we will consider the strike at an off PMOS drain area [10].

A particle can induce SEU when it strikes at the channel region of an off NMOS transistor or the drain region of an off PMOS transistor. The ionization can induce a current pulse in a p-n junction.

A schematic view of how the SEE induced current pulse translates into an SEE induced voltage pulse is given in Figure 3.

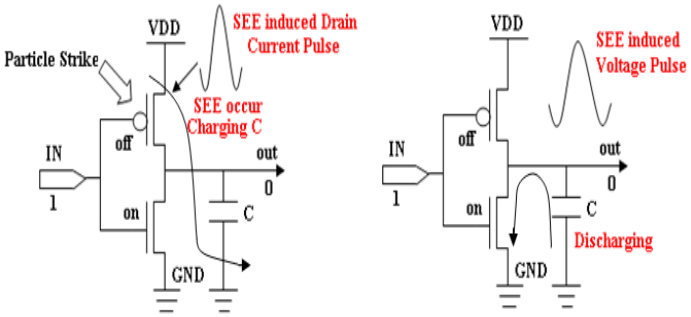


Figure 4: Generation of SEE induced voltage pulse

Due to reduction of feature size the SEUs play an increasing role in failures observed during operation of digital circuits, particularly in environments with remarkable rediation level (avionics, nuclear, high energy, physics instrumentation etc.). in a few years SEUs will significantly affect the digital electronics not only in this special radiation environment but at the normal operating conditions as well. Therefore the counter measure against SEUs gains importance as technology feature size drops down [5]. The electronic sysyem can be build using radiation-hardened semiconductor devices but they skyrocket the system cost.

Most other circuit level approaches model the effect of a particle strike[12] with the help of a transient current source as shown in figure

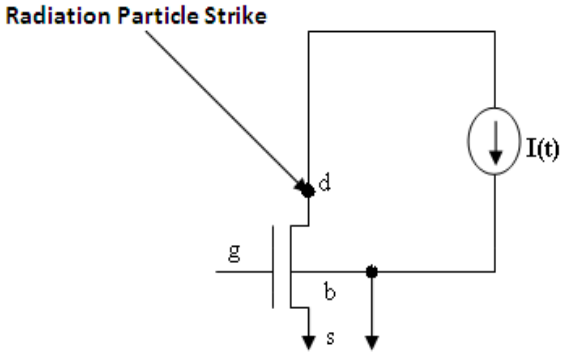


Figure 5: Particles strike modeled by a transient current source

A common approximation to determine the current slope I(t) is the double exponential function in equation [15]. Here τ_α is the collection time-constant of the p-n junction and τ_β denotes the time constant for establishing the electron-hole track. An alternative model is given by formula with parameters Q, t and K, where q is the collectiod charge, t is a pulse shaping parameter and K is a constant [14].

$$I(t) = I_0(\exp\left(-\frac{t}{\tau_\alpha}\right) - \exp\left(-\frac{t}{\tau_\beta}\right)) \quad (3)$$

$$I(t) = \frac{K.Q}{\tau}\sqrt{\frac{t}{\tau}}exp\left(-\frac{t}{\tau}\right) \quad (4)$$

simplification is appropriate for modeling diffusion, but charge collection by drift depends on the electric field strength, and thus on the voltage.

III. Modeling and simulation of SRAM

Using VPULSE input signal source, having value, V1=0V, V2=5V, TD=0, TR=1m, TF=1m, PW=5m, PER=10m, the WORD line is connected to high voltage level, due to this MOS transistor Q5 and Q6 are ON

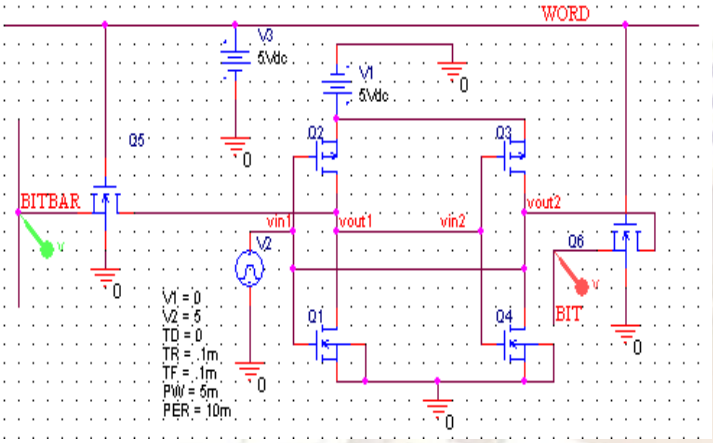


Figure 6: Modeling of 6t SRAM cell in ORCAD PSPICE 16.5

In this figure 6, BIT and BITBAR are complement to each other which is the basic working of the SRAM cell [6,7,8,9,10,11]. The following figure is a simulation waveform (ORCAD PSPICE 16.5) of schematic of 6 transistor SRAM cell

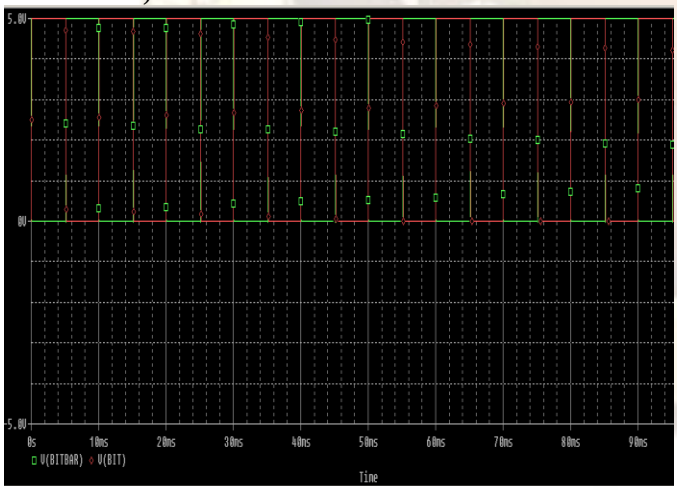


Figure 7: Simulation result of 6t SRAM cell

The figure shows voltage status at the two output level BIT and BITBAR, which is complement to each other (according to the working of SRAM) [9]. The green line show the voltage level of BITBAR and red line show the voltage level of BIT which is complement to each other.

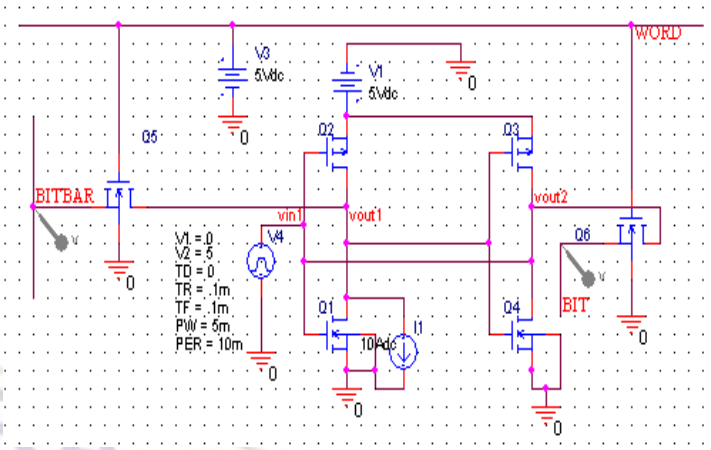


Figure 8: SEU effect on 6t SRAM by injecting current source

In this figure SEU effect is injecting by parallel connection of current source to the NMOS which is OFF due to this the desired output is not available [3].

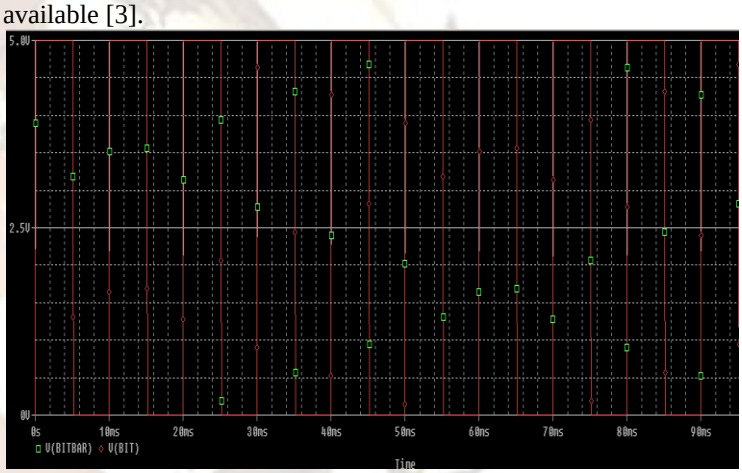


Figure 9: Simulation of figure, injecting SEU effect in SRAM cell

The figure shows that the value of BIT and BITBAR are equal. The green line which show the voltage level of BITBAR are overlap to red line which show the voltage level of BIT.

To remove this SEU effect the radiation hardened circuit of full SRAM is used which is shown below.

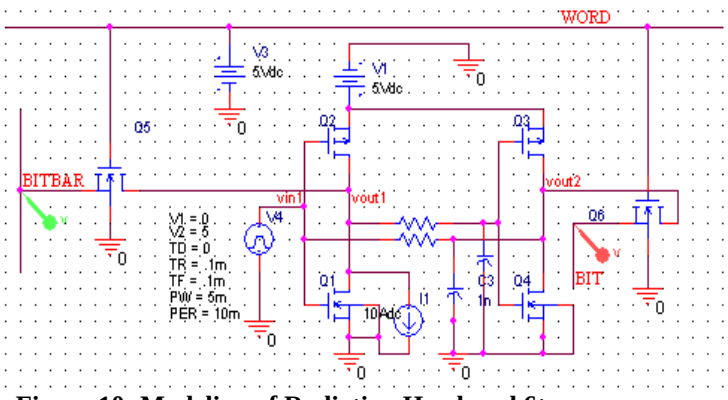


Figure 10: Modeling of Radiation Hardened 6t SRAM cell in ORCAD PSPICE 16.5 [5]

In this circuit current source is still connected in the circuit but some other changes is used to removed the radiation effect which is cause by the injecting current source parallel to the NMOS [3].

The figure shows that, due to the use of radiation hardened circuit , SEU effect is almost removed in SRAM and the circuit resumes its actual behaviour which is reflect in the resultant waveform, in which BITBAR and BIT are complement to each other.

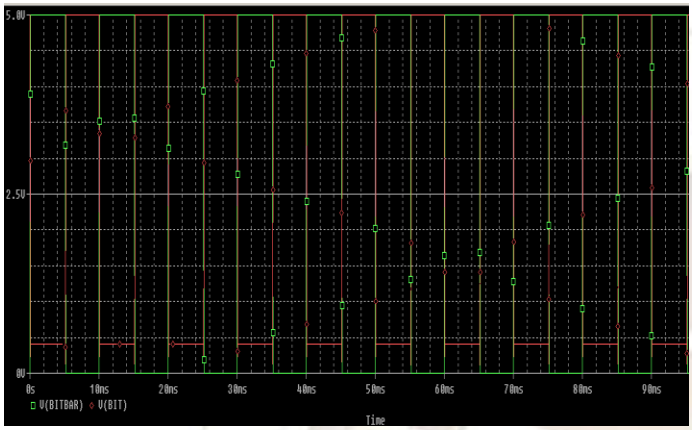


Figure 11: Simulation waveform of SRAM hardened circuit.

IV. Conclusion

In this paper we see how we can induced single event upset in SRAM and how we can remove it using radiation hardened circuit. Radiation hardened circuit is used to protect your digital device from radiation effect. But the radiation hardened circuit is complex so this is the limitation of this project.

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