A. Suresh Kumar, G. Mahanandeswara Gowd / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 3, Issue 4, Jul-Aug 2013, pp.2162-2167

Simple Boost Control of Five-Level Z-Source Diode-Clamped Inverter by Multi-Carrier PWM Methods

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Abstract

In recent years, multilevel inverters have drawn significant attention in research and high power applications such as AC Transmission systems (FACTS), renewable energy resources, power quality devices, etc. Such power converters have been the prime focus of power electronic researches in order to improve their performance, reliability and energy efficient at minimum cost. Among several reported topologies, diode-clamped multilevel inverter is very used. To control these multilevel inverters several carrier –based PWM strategies have been reported. Traditional inverters are known to produce an output voltage that is lower than the DC source voltage. In order to reach boosted voltage with available switching devices Z-source inverters were invented. Multilevel Z-source inverters have been proposed as a solution for HV applications. This type of inverters decreases the Total Harmonic Distortion (THD) and has a good performance for different applications such as Flexible AC Transmission systems, power quality improvement and connecting renewable energy resources to the network. This paper compares several alternative carrier disposition PWM strategies (Phase Disposition (PD) method, Alternative Phase Opposition Disposition (APOD) method) for a five level Z-source diode–clamped inverter. These strategies are simulated in MATLAB/Simulink.The simulation results will illustrate the performance of Phase Disposition (PD) method, Alternative Phase Opposition Disposition (APOD) method.

Keywords- Multicarrier PWM strategies, multilevel inverter, DC-Sources, Z-Source inverter.

I. INTRODUCTION

There exist two traditional converters: voltage source (VSI) and current source (CSI) [1]. Fig.1 shows the traditional single-phase voltage-source converter (abbreviated as V-Source converter) structure. A dc voltage source supported by a relatively large capacitor feeds the main converter circuit, to a single-phase circuit. The dc voltage source can be a battery, fuel-cell stack, diode rectifier, and/or capacitor. Four switches are used in the main circuit; each is traditionally composed of a power transistor and an antiparallel (or freewheeling) diode to provide bidirectional current flow and unidirectional Voltage blocking capability. The V-source converter is widely used.

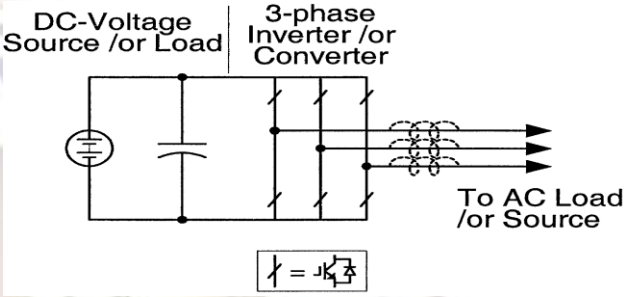

Fig. 1. Traditional V-source converter

It has the following conceptual and theoretical barriers.

- The AC output voltage is limited below and cannot exceed the DC input voltage.
- External equipment is needed to boost up the voltage, which increases the cost and lowers the overall system efficiency.
- There is a possibility for the occurrence of short Through which destroys the device.

II. Z-SOURCE INVERTER

The main objective of static power converters is to produce an AC output waveform from a dc power supply. Impedance source inverter is an inverter which employs a unique impedance network coupled with the inverter main circuit to the power source. This inverter has unique features in terms of voltage (both buck & boost) compared with the traditional inverters. A two port network that consists of a split-inductor and capacitors that are connected in X shape is employed to provide an impedance source (Z-source) coupling the inverter to the dc source, or another converter. The DC source/load can be either a voltage or a current source/load. Therefore, the DC source can be a battery, diode rectifier, thyristor converter, fuel cell, PV cell, an inductor, a capacitor, or a combination of those [1].

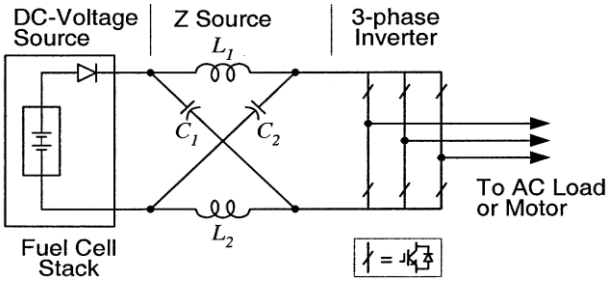

Fig2.ZSI Using the Antiparallel combination of switch and diode.

A. Impedance Network

The Z-source concept can be applied to all DC-to-AC, AC-to-DC, and AC-to-AC and DC-to-DC power conversion. It consists of voltage source from the DC supply, Impedance network, and three phase inverter and with AC motor load**.** AC voltage is rectified to DC voltage by the three phase rectifier. In the rectifier unit consist of six diodes, which are connected in bridge way. This rectified output DC voltage fed to the Impedance source network which consists of two equal inductors (L1, L2) and two equal capacitors (C1, C2).The network inductors are connected in series arms and capacitors are connected in diagonal arms .The impedance network is used to buck or boost the input voltage depends upon the boosting factor. This network also act as a second order filter .This network should require less inductance and smaller in size. Similarly capacitors required less capacitance and smaller in size. This impedance network, constant impedance output voltage is fed to the three phase inverter main circuit. Depending upon the Gating signal, the inverter operates and this output is fed to the 3-phase AC load or AC motor.

B. Equivalent Circuit and Operating Principle

The main feature of the Z-source is implemented by providing gate pulses including the shoot-through pulses. Here how to insert this shoot through state becomes the key point of the control methods. It is obvious that during the shoot-through state, the output terminals of the inverter are shorted and the output voltage to the load is zero. The output voltage of the shoot through state is zero, which is the same as the traditional zero states, therefore the duty ratio of the active states has to be maintained to output a sinusoidal voltage, which means shoot-through only replaces some or all of the traditional zero states. Let us briefly examine the Z-source inverter structure. In Fig. 2, the three-phase Z-source inverter bridge has nine permissible switching states (vectors) unlike the traditional three-phase V-source inverter that has eight. The traditional three-phase V-source inverter has six active vectors when the DC voltage is impressed across the load and two zero vectors when the load terminals are shorted through either the lower or upper three devices, respectively. However, three-phase Z-source inverter bridge has one extra zero state (or vector) when the load terminals are shorted through both the upper and lower devices of any one phase leg (i.e., both devices are gated on), any two phase legs, or all three phase legs. This shoot-through zero state (or vector) is forbidden in the traditional V-source inverter, because it would cause a shoot-through. We call this third zero state (vector) the shoot-through zero state (or vector), which can be generated by seven different ways: shoot through via any one phase leg, combinations of any two phase legs, and all three phase legs. The Z-source network makes the shoot-through zero state possible. This shoot-through zero state provides the unique buck-boost feature to the inverter. The Z-source inverter can be operated in three modes which are explained in below.

i. Open circuit state:

The equivalent circuit of the bridge in this mode is as shown in the fig 3.

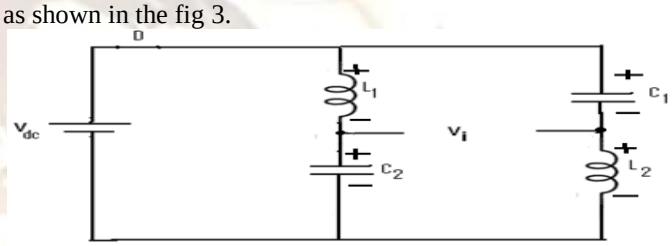

Fig. 3: Equivalent Circuit of the ZSI in one of the Two Traditional Zero States.

The inverter bridge is operating in one of the two traditional zero vectors and shorting through either the upper or lower three device, thus acting as an open circuit.

ii. Shoot through state:

The inverter bridge is operating in one of the seven shoot-through states. The equivalent circuit of the inverter bridge in this mode is as shown in the below figure 4. In this mode, separating the dc link from the ac line. This shoot-through mode to be used in every switching cycle during the traditional zero vector period generated by the PWM control. Depending on how much a voltage boost I needed, the shoot-through interval (T0) or its duty cycle (T0/T) is determined. It can be seen that the shoot-through interval is only a fraction of the switching cycle.

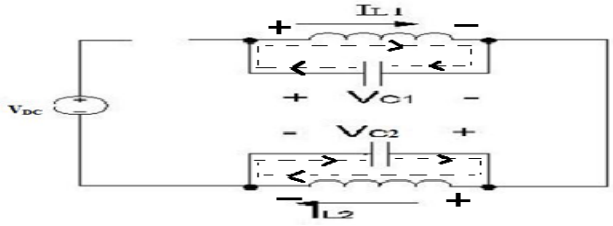

Fig. 4: Equivalent Circuit of the ZSI in the Shoot-Through State.

iii. Active state:

In this mode, the inverter bridge is operating in one of the six traditional active vectors; the equivalent circuit is as shown in figure.

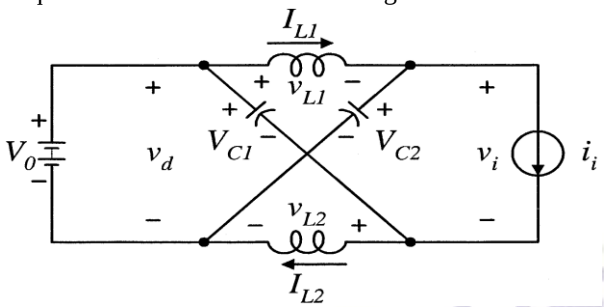

Fig5.Equivalent circuit the ZSI in one of the Six Active States

The inverter bridge acts as a current source viewed from the DC link. Both the inductors have an identical current value because of the circuit symmetry. This unique feature widens the line current conducting intervals, thus reducing harmonic current.

III. EQUATION FOR THE OUTPUT PEAK PHASE VOLTAGE

Ac output voltage: Vac =M*B*(Vdc/2)

Where M=modulation index = (reference voltage/carrier voltage)

B =Boost factor = {1/ (1-2T0/T)} ≥ 1

T0=Shoot through period.

T=Total switching period.

B0=M*B=Buck boost factor.

The output voltage can be stepped up & stepped down by varying the Buck boost factor.

IV. SIMPLE BOOST CONTROL

Actually, this control strategy inserts shoot through in all the PWM traditional zero states during one switching period. This maintains the six active states unchanged as in the traditional carrier based PWM.The implementation of simple boost control method [19] is illustrated in Fig. 6. Two straight lines are employed to realize the shoot through duty ratio (Do). The first one is equal to the speak value of the three-phase sinusoidal reference voltages while the other one is the negative of the first one. When the triangular carrier waveforms is greater than the upper envelope, *Vp*, or lower than the bottom envelope, *Vn*, the circuit turns into shoot-through state. Otherwise it operates just as traditional carrier-based PWM.

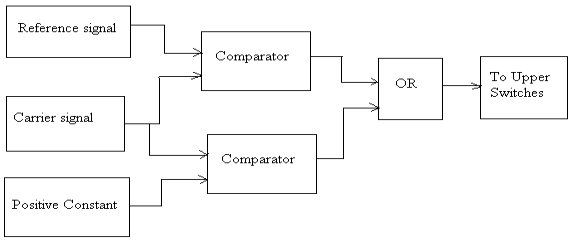

Fig6 (a)

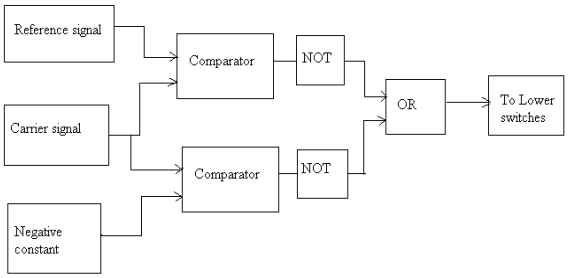

Fig 6(b): Implementation Diagrams of SBC

Shoot-through pulses are inserted into the switching waveforms by logical OR gate. To produce switching pulses, three phase reference wave forms having peak value with modulation index (M) are compared with the same high frequency triangular signal. Comparator compares these two signals and produces pulses (when Vsin>Vtri, on and Vsin<Vtri, off). These pulses are then sent to gates of the power IGBT's through isolation and gate drive circuit. Figure 7 shows the pulse generation of the three phase leg switches (S1, S3 and S5-positive group/upper switches and S2, S4 and S6 negative group/lower switches).This method is much uncomplicated; however, the resulting voltage stress across the device is relatively high because some traditional zero states are not utilized either partially or fully. This characteristic will restrict the obtainable voltage gain because of the limitation of device voltage rating. For a complete switching period, T is total switching period, T0is the zero state time period and Do is the shoot-through duty ratio. In this paper, the control of ZSI is done by this control technique (SBC).

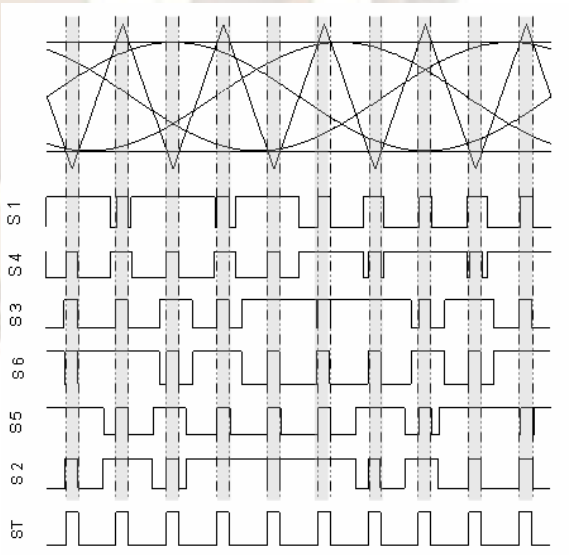

Fig 7: PWM Signals from Simple Boost Control

V. MULTILEVEL INVERTERS

There are several drawbacks of two level inverter in which the switching devices have limited ratings .So that these cannot used effectively in high power and high voltage applications. And also at high switching frequencies these two level inverter has high switching losses that leads to decrease in the efficiency. If we consider the Multilevel Inverters, These are suitable for high voltage and high power applications. Because the switching device voltage stresses are controlled. And increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating. As the number of voltage levels increases the harmonic content of the output voltage waveform decreases significantly. From the figure we can see the main purpose of the capacitor is to split the dc source into equal voltages and they act as energy sources for the inverter .The number of capacitors require for 5-level (m-level) inverter is 5-1=4 i.e. (m-1) . The number of switching devices per leg is 2 (m-1) i.e. 8 for five levels.

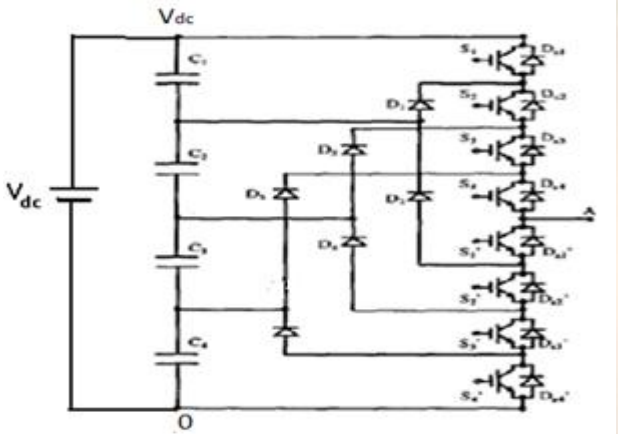

Fig8.Five-level diode clamped inverter.

For understanding the Clamping mechanism i.e. for producing five levels in the output voltage ,the required sequence of switching states are given in the table1.

Diode-Clamped Voltage Level and Their Switching States

Output (V_o)	Switch states							
Levels	S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	0	0	1	1	1	1	0	0
$V_3 = V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2 = V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	0

Table1: Switching states of five level diode-clamped inverter.

A. View of Five-level Z-Source Diode-Clamped Inverter

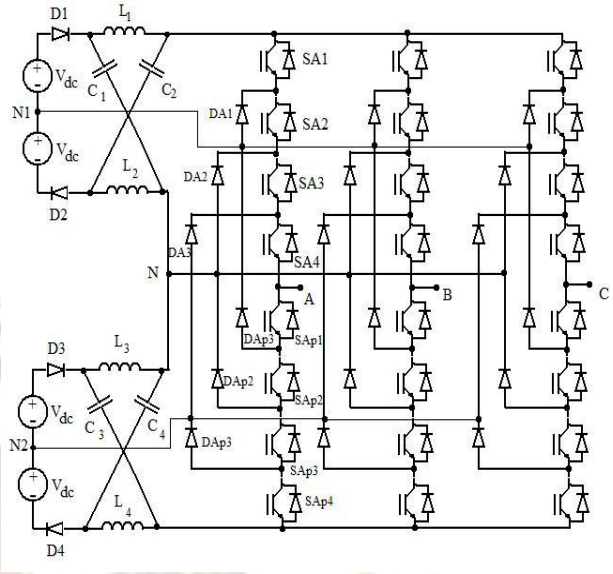

Fig9. Five-level Z-Source Diode-Clamped Inverter

VI. MULTICARRIER PWM STRATEGIES

There are four carrier-based PWM schemes for mentioned topologies.

a) Alternative Phase Opposition Disposition (APOD), where each carrier signal is phase shifted by180 from adjacent carrier;

b) Phase Opposition Disposition (POD), where the carrier signals above the sinusoidal reference zero point are 180 out of phase with those below the zero point;

c) Phase Disposition (PD), where all carrier signals are in phase.

Fig. 10 shows carrier-based PWM strategies. APOD, POD and PD modulations are used to control most of multilevel inverter structures.

There are several methods to control Z-source inverter that can be classified into shoot-through states insertion methods. In the first method, six shoot-through states will be inserted in one switching cycle. The second method two shoot-through states will be directly inserted in one cycle [18].

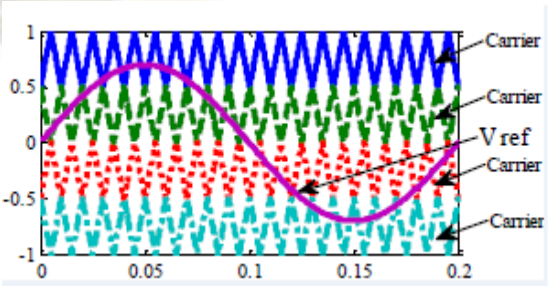

Fig10 (a)

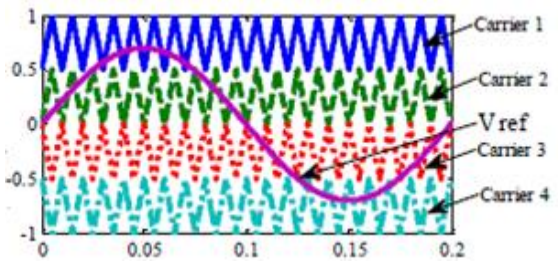

Fig10 (b)

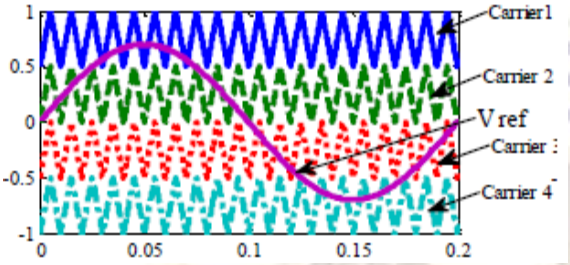

Fig10(c)

Fig.10: CarrierbasedPWMstrategies, (a) APOD modulation, (b) POD modulation and (c) PD modulation.

VII. SIMULATION RESULTS

For comparison, the carrier-based PWM strategies that are Applied to a five-level Z-source inverter. The simulations have been carried out in MATLAB/Simulink. Major system parameters are listed in Table 2.

Table 2 -System parameters

	PARAMETER
Source	$V_{dc} = 40V$
LC Network	$L = 4.3mH$
	$C = 3$ micro F
Inverter	$f_c = 10kHz$
	$f_r = 50Hz$
	$M = 0.8$, K=0.8
	$T_0/T = 0.3$
Load	$L = 1mH$
	$R = 100\,\Omega$

Figs. (11), (12) and (13) show Line-to-Line voltages of five level Z-Source diode clamped inverter.

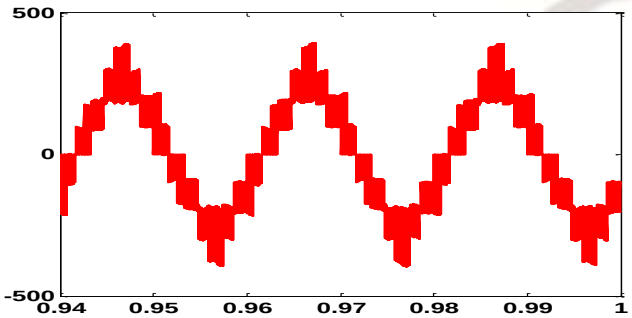

Fig (11)**:** Line to line voltage (APOD modulation)

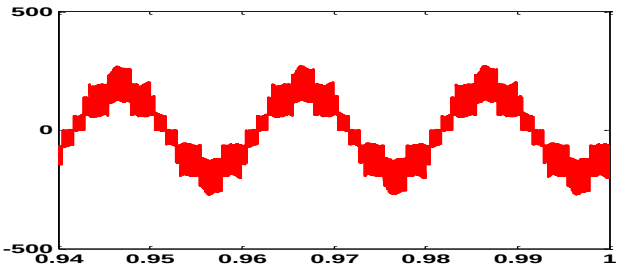

Fig (12)**:** Line to line voltage (POD modulation)

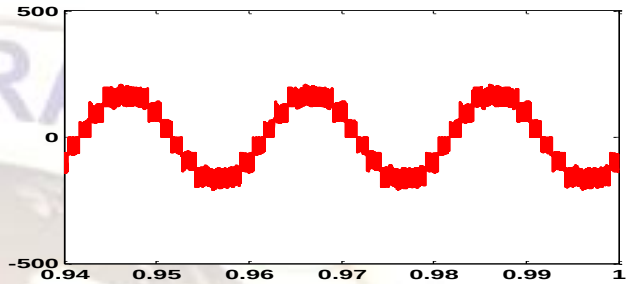

Fig (13)**:** Line to line voltage (PD modulation)

In Table 3, the amplitude and the THD of the line-to-line voltages of three methods are presented.

As given in Table 3, it is clearly deduced that APOD modulation will boost the voltage more than POD and PD modulation in the same condition. Also, Line-to-Line voltage harmonics increase in PD, APOD and POD, respectively. Considering the aforementioned advantages, APOD modulation is a suitable technique to be applied in this type of converters

A. Simulation Diagram:

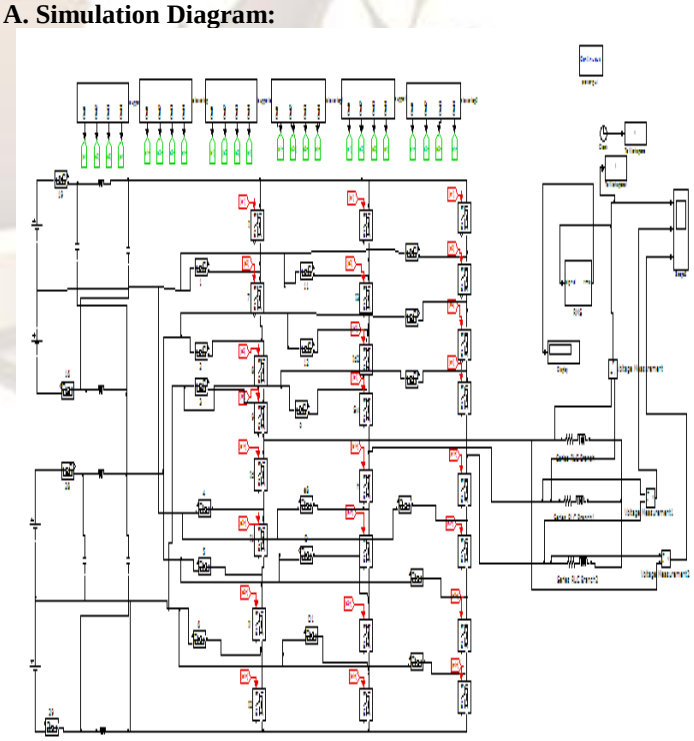

Table3: Simulation results of different methods.

S.NO	PWM Method	Output Voltage(L-L)rms	%THD
1	PD	136.895	21.42%
2	POD	141.697	34.82%
3	APOD	183.41	28.02%

VIII. CONCLUSION

- The lowest %THD happens in Phase disposition method.
- The APOD scheme will boost the voltage more than the POD and PD modulation technique in the same condition.
- The highest %THD happens in POD method.

"The simulation results illustrate that using Phase disposition method decrease the %THD considerably. Also APOD method increases the voltage more than the PD method. Both methods can be used effectively."

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