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Design Of Low Power &Energy Proficient Pulse Triggered Flip-Flops

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ABSTRACT

In this paper, pulse-triggered flip-flop types which are bidirectional elements in sequential logic circuits were designed. Initially, the pulse generation control logic is removed from the critical path to facilitate a faster discharge operation. Following low-power techniques are implemented, such as conditional capture, conditional precharge, conditional discharge, conditional data mapping, clock gating technique and SAL technique. Among all the mentioned techniques, SAL technique is the best one to avoid internal switching activities to reduce power dissipation, and also proposed circuit can be estimated as free of glitches. This paper explores the energy-delay space of widely referred flip-flops in a 180nm CMOS technology.

Keywords: Flip-Flop, Low Power, Pulse triggered, clock gating, SAL technique.

I. INTRODUCTION

The performance of VLSI integrated circuits are strongly influenced by the clock network design and appropriate choice of flip flops (FFs) is of fundamental importance[7]. Flip Flops are extremely important circuit elements in all synchronous VLSI circuits. They are not only responsible for correct timing, functionality and performance of the chip, but also they and other clock distribution networks consume a significant portion of the total power of the circuit. It is estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%-45% of the total system power. Comparing to different elements in VLSI circuits , Flip Flops are the primary source of the power consumption in synchronous system. Moreover , FFs have a large impact on circuit speed the performance of the flip flop is an important element to determine the performance of the whole circuit. Therefore, the studies on flip flop become more and more in recent years[8]. The basic types of flip flop is classified based on clock ,that are S-R flip flop, D flip flop, JK flip flop, T flip flop. Among all the types D flip flop is most widely used because D-type flip flops in ICs have the capability to be forced to the set or reset state(which ignores the D and clock inputs),much like an SR flip flop. Usually, the illegal S=R=1 condition is resolved in D-type flip flops. The advanced flip flop classes are MS (Master-slave),Implicit &Explicit pulsed, DET(Dual-edge triggered),Differential[7]. In these types pulse triggered flip flops (P-FFs) are studied in this paper. The flip flop tree diagram is shown below.

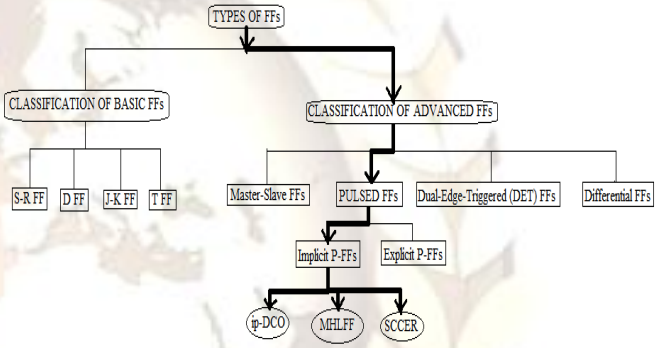

Fig 1: Flip Flop Tree Diagram

II. PULSE TRIGGERED FLIP FLOPS

For higher performance, the pulse triggered flip flops are the fastest alternatives among all the flip flop types[9]. A P-FF consists of a pulse generator for generating strobe signals and latch for data storage. Since triggering pulses generated on the transition edge of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF.

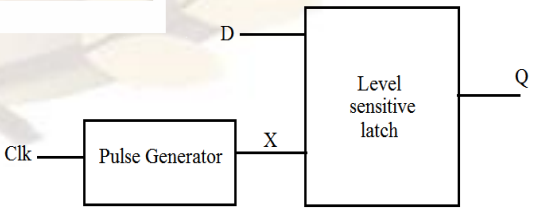

Fig2: Block diagram of Pulse triggered flip flop

The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master-slave configuration , is needed. Depending on the method of pulse generation , P-FF design can be classified as implicit

or explicit . in an implicit type P-FF ,the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit type P-FF, the design of pulse generator and latch are separate[1]. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit type designs , however , face a lengthened discharging path in latch design, which leads to inferior timing characteristics. Explicit type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches. Pulse triggered flip flops reduce the two stages into one stage and are characterized by the soft edge property. Due to these timing issues, P-FFs provide higher performance than their master slave counterparts, and since we are concerned about performance, MS FFs will not be discussed any further in this paper. P-FFs outperform hard-edged FFs, as they provide a soft edge, negative setup time, and small to delays, which help not only in reducing the delay penalty this flip flops incur on cycle time but also help in absorbing the clock skew. Many contemporary microprocessors selectively use Master-Slave and Pulse-triggered flip flops.

III. ANALYSIS OF IMPLICIT TYPE P-FFS

In this paper three types of implicit pulse triggered flip flops are studied. That are ip-DCO(implicit data close to output), MHLFF (modified hybrid latch flip flop) , SCCER (single-ended conditional capture energy recovery).

A. *ip-DCO*

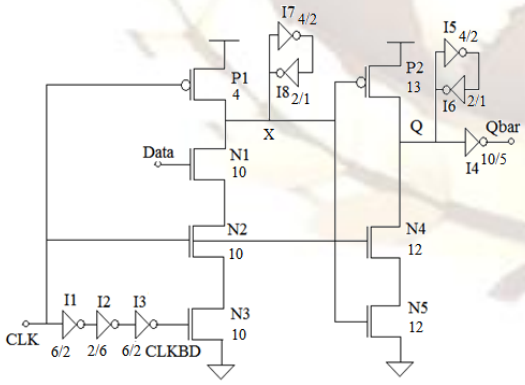

Fig 2(a): P-Ff Design ,Named Ip-Dco[2].

It contains an AND logic-basedpulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3 two practical problems exit in this design. First , during the rising edge, NMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X cause speed and power performance degradation[1].

B. *MHLFF*

By employing a static latch structure presented. Node X is no longer precharged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node X level at high when Q is zero.

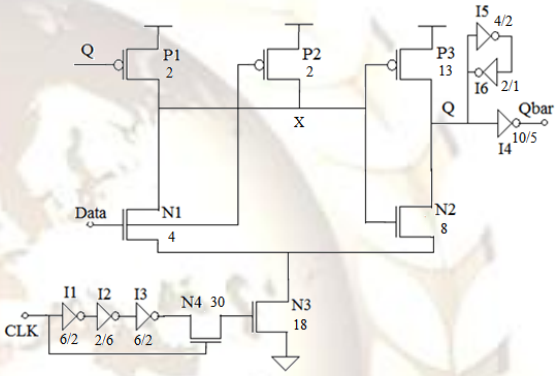

Fig 2(b): Improved P-FF design, named MHLFF [3]

This design eliminates the unnecessary discharging problem at node X. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node X is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node X becomes floating when output Q and input data both equal to "1". Extra DC power emerges if node X is drifted from an intact "1"[1].

C. *SCCER*

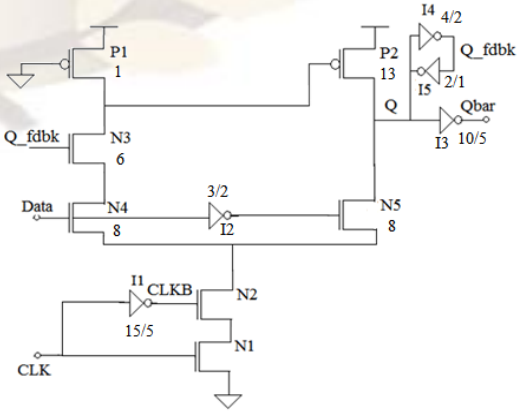

Fig 2(c) shows a refined low power P-FF design , named SCCER[4].

In this design , the keeper logic (back-to-back inverters I7 and I8 in fig 2(a)) is replaced by a weak pull-up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X. The discharge path contains NMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra NMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1"node X is discharged through four transistors in series, i.e ., N1 through N4 while combating with the pull-up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width[1].

IV. ADVANTAGES & DISADVANTAGES OF P-FFs

Study of implicit type P-FF designs , ip-DCO, MHLFF , SCCER are presented in this paper. Besides the speed advantage of P-FFs, it consumes much power compared to the other types of flip flops. P-FF has been considered as popular alternative to the conventional Master-slave based FF in the applications of high speed operations[1]. For this cause leads to achieve low power in high speed region. According to ip-DCO, it is the glitch free circuit and it is the fastest implicit type P-FF designs under analysis but it consumes much power. For improved P-ff design , named MHLFF ,in this the advantage is lower number of transistors & less power consumption because by avoiding unnecessary internal node transition but the delay is increased ip-DCO to MHLFF and having glitches at the output. There by further analysis is done in energy recovery FF that is SCCER, in this much less power consumption is achieved compared to MHLFF but it contains more glitches & delay is further increased from MHLFF to SCCER. Finally, in SCCER consumes less power but delay is increased.

V. TECHNIQUES

To achieve low power in high speed region , the study of different low power techniques are carried out. Such as conditional capture, conditional precharge, conditional discharge, conditional data mapping and clock gating technique. Clock gating is the best one to avoid internal switching activities. The basic principle of energy efficient is to recycle the energy stored in the capacitors by using the LC network. This principle of energy efficient is not applicable to the square wave clock generators. In order to make energy efficient possible we require sinusoidal clock signals and the clock generally has idle states during which it can be turned off else it would continue to run and consume the same amount of power as in the active state. The clock gating is implemented by replacing the inverter with the NAND gate. By applying clock gating technique to SCCER circuit, there is no change at the outputs regarding power dissipation & delay but some glitches are reduced. So, further study low power techniques is done , in that SAL (self adjustable voltage level) technique is efficient one for achieving low power in high speed region.

D. SAL explanation

Self-adjustable voltage level (SAL) technique is the one of low power technique to achieve besides low power and delay in the circuit Where Vdd is the supply voltage and VL is the output voltage of this circuit, which is applied to any load circuit.(In this paper implicit type P-FF designs are the load circuit). During the active mode (when SL=0), this circuit supplies maximum supply voltage to the load circuit through the ON PMOS transistor (P1) so that the load circuit can operate quickly.

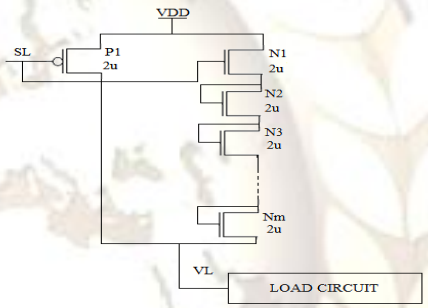

Fig 3: SAL circuit[5]

During the standby mode (when SL=1), it provides slightly lower supply voltage to the load circuit through the weakly ON NMOS transistor (N1, N2, N3..... Nm). So the voltage applied to the load circuit is given by

$$VL = Vdd - Vn$$

Where Vn is the voltage drop of m weakly ON NMOS transistors.The drain to source voltage Vdsn of the OFF NMOS in the standby mode is expressed as

$$Vdsn = VL - Vss = VL$$

Vdsn can be decreased by increasing Vn that is increasing m, the number of NMOS transistors . when Vdsn is decreased, the DIBL (Drain – induced – barrier – lowering) effect is decreased and this in turn increases the threshold voltage Vtn of NMOS transistors. Consequently the sub threshold leakage current of the OFF MOSFETs decreases, so leakage power is minimized while data are retained[5].

VI. Discussion of SAL results

In this paper implicit type pulse triggered flip flop designs are presented. The Proposed designs that are ip-DCO using SAL, MHLFF using SAL,

SCCER using SAL, shows Power improvement than the Existing Pulse Triggered Flip-flop designs that are ip-DCO, MHLFF , SCCER . Present paper analyze the three types of pulse triggered flip flops and comparision is done according to different flip flop parameters, that are Total power dissipation, delay, noise figure & gain. To demonstrate the superiority of the proposed design, simulation results on various P-FF designs were conducted to obtain their performance figures. These designs include the three P-FF designs shown in Fig. 1 (ip-DCO, MHLLF, SCCER). Simulations are performed using 180nm CADENCE tool is used to find the total power dissipation (TPD) of the above analyzed flip flops.

A Transient analysis is carried out assuming typical parameters, with power supply voltage 1.8volts, transient analysis from 0-200ns,the clock period is 20ns,the data period is 30ns and taking the delay time, rise time, fall time is 1nSec. Similarly DC & NOISE analysis are done for identifying the noise figure and gain.

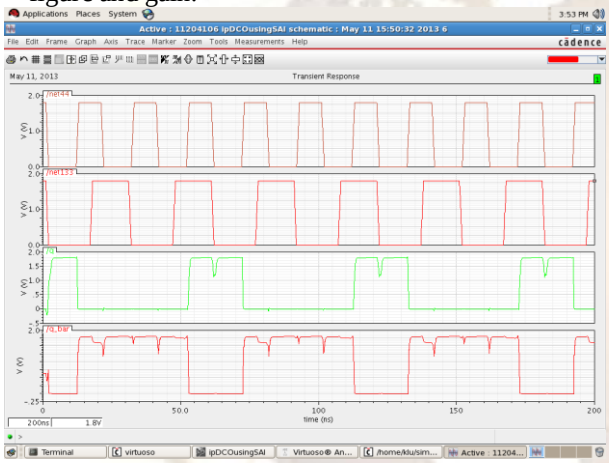

Fig 4.1: Simulation result for ip-DCO using SAL technique.

Fig 4.2: Simulation result for MHLFF using SAL technique.

Fig 4.3: Simulation result for SCCER using SAL technique.

VII. COMPARITION OF TPD, DELAY, NOISE FIGURE & GAIN

PARAMETERS			Before Applying SAL		
			Ip-DCO	MHLFF	SCCER
Total Power Dissipation			1.88852 m	1.37465 m	1.27574 m
Delay			16.37E-9	16.42E-9	34.88E-9
Noise Figure	Freq	Max	285.5	315.3	308.1
		Min	25.82	6.398	6.609
	Volt	Max	25.97	7.873	12.82
		Min	21.26	5.526	9.407
gain	Freq	Max	1.17E-02	2.02E-02	1.07E-01
		Min	1.99E-14	5.92E-12	7.84E-12
	Volt	Max	4.73E-03	2.79E-02	1.50E-02
		Min	8.16E-03	3.33E-02	1.99E-02

TABLE 1: BEFORE APPLYING SAL

PARAMETERS			After Applying SAL		
			Ip-DCO SAL	MHLFF SAL	SCCER SAL
Total Power Dissipation			626.601 n	561.757 p	136.102p
Delay			15.47E-9	35.23E-9	34.42 E-9
Noise Figure	Freq	Max	195.2	194	179.1
		Min	13.28	4.737	1.429
	Volt	Max	13.91	5.323	4.537
		Min	11.75	4.253	3.456
gain	Freq	Max	1.05E-01	1.00E-01	1.31E-01
		Min	9.97E-06	8.93E-05	4.91E-05
	Volt	Max	1.74E-02	5.96E-02	4.53E-02
		Min	2.29E-02	7.20E-02	5.05E-02

TABLE 2: AFTER APPLYING SAL

Before and after applying SAL Technique to the three types of Pulse Triggered Flip Flop designs, there is a tremendous change in the FF parameters like Total Power Dissipation, Delay, Noise Figure and Gain is listed above. In Total Power Dissipation there is an improvement from milli meter- nano meter – pico meter. According to Delay there is 1.31% improvement is obtained. There is 42.01% improvement in the Noise Figure with respect to Frequency and 83.07% improvement in the Noise Figure with respect to Voltage. Coming to the Gain parameter, 91.07% improvement with respect to Frequency and 86.55% improvement with respect to Voltage.

VIII. IMPLEMENTATION

Pulse triggered flip flop has been successfully used on many high performance low power processors. For instance, on INTEL's Pentium processor chips more than 90% of the FF adopts pulse triggered FF architecture. Besides improving system performance, it also reduces power consumption and can resolve incurred cooling and chip packaging issues. Integrated circuit operating frequency and density increases duo to deep submicron technology. Single chip containing many complex functional blocks with interconnects and buses. As complexity of circuit increases noise effect also increases like capacitive or inductive cross talk, transmission line effect etc. One of the common approaches to reduce the noise hazard is to bound the noise. Some deterministic method like BIST will generate the test pattern and detect the faults due to noise. Another approach is to detect the noise is on-line testing method. It will test the function block during operation time it has many advantages over deterministic methods. This method is highly reliable, increased system performance and high degree of noise tolerance. Double sampling data checking technique is the one of the online testing method[6].

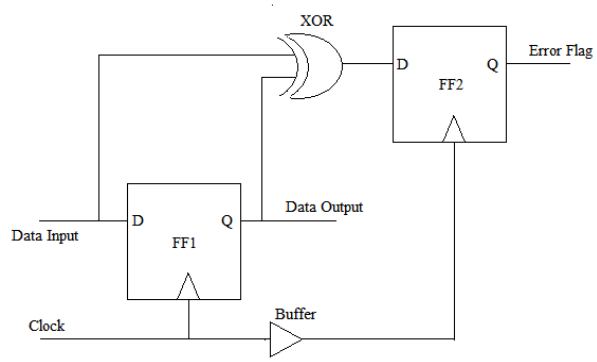

Fig 3.3: Error Detection circuit.

The principle behind this method is input data is sampled by two FF at a time interval dt and consistency is checked from the two latched data's with each other. Consider the noise interval tn is less than dt. One of the FF will be catches the error and sends the error signal, and the rest of the clock cycle will indicate error (i.e difference) is occurred by comparing the two FFs[6].

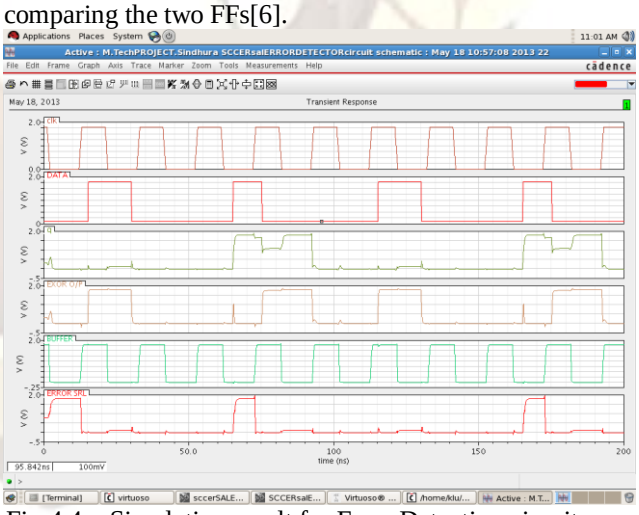

Fig 4.4: Simulation result for Error Detection circuit using SAL technique.

IX. CONCLUSION

One of the main advantages of pulse-triggered Flip- Flops is that they allow time borrowing across cycle boundaries as a result of the zero or even negative setup time. Due to these timing issues, pulse-triggered flip-flops provide higher performance than their master-slave counterparts. In such circuits where the performance and power are

high volatile constraints the devices with better the performance with low power are much essential and this paper achieves the simple P-FF design with reduction in power with optimized delay as that of SCCER FF, but when compared with other methodologies like ip-DCO, MHLFF the power and delay are substantially reduced.

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