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Designing CNTFET and Force Stacking CNTFET Inverter for the Analysis of Average Power and PDP at Different Low Supply Voltage

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ABSTRACT

As technology scales down to 90nm and below, the bulk CMOS technology has approached the scaling limit due to the increased short-channel effects, increased leakage power dissipation, severe process variations, high power density, and so on. To overcome this scaling limit, different types of materials have been experimented. Si-MOSFET-like Carbon nanotube FET (CNFET) devices have been evaluated as one of the promising replacements in the future nanoscale electronics. CNFET has lower short-channel effect and a higher sub-threshold slope than Si-MOSFET .It has been observed that the stacking of two off devices has smaller leakage current than one off device. this paper propose an inverter that uses forced stack technique to reduce average power and PDP. circuit is simulated using HSPICE with Stanford CNFET model at 32nm. The simulation result shows that the proposed forced stack CNTFET inverter reduce average power by 15% when supply voltage is 0.9v ,13.204% when supply voltage is 0.8v and 13.116% when supply voltage is 0.7v.

Keywords -Average Power, CNTFET, Force Stacking, HSPICE, PDP

I. INTRODUCTION

The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Thinner gate oxides have led to an increase in gate leakage current. Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever

increasing share in the processor power consumption. In 65 nm and below technologies, leakage accounts for 30-40% of processor power. According to the International Technology Roadmap for Semiconductors (ITRS) [1], leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. According to Moore's law, the dimensions of individual devices in an integrated circuit have been decreased by a factor of approximately two every two years. This scaling down of devices has been the driving force in technological advances since late 20th century. However, as noted by ITRS 2009 edition, further scaling down has faced serious limits related to fabrication technology and device performances as the critical dimension shrunk down to sub-22 nm range [1]. The limits involve electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping [2]. Carbon nanotubes (CNT) are very promising in respect of overcoming the serious limits faced by the Si CMOS Technology, because of their exceptional structural, electronic, and optical properties [2]. In particular, they exhibit ballistic transport over length scales of several hundred nanometers. Nanotube devices can be integrated with existing silicon-based structures. A CNTFET refers to a FET that uses CNT as the channel instead of bulk silicon in the traditional MOSFET structure.

Inverter is one of the important building block in the digital circuit. SRAM is further building block built from inverter which occupies about 90% of the area of soc in 2013[1].so its important to design low power inverter using CNTFETs.
Authors [5-8] proposed a new SRAM cell cell design using CNTFETs. while there are circuit level solutions to reduce leakage in processors[9-13]. Force stacking technique is used in leakage reduction authors have already published their paper in

IJERA[17].this paper proposes a novel approach for reducing average power in CNTFET based inverter and force stacking CNTFET inverter at low supply voltage.

II. THE CARBON NANOTUBE FET

The operation principle of carbon nanotube field-effect transistor (CNFET) is similar to that of traditional silicon devices. This three (or four) terminal device consists of a semiconduting nanotube, acting as conducting channel, bridging the source and drain contacts. The device is turned on or off electrostatically via the gate. The quasi-1D device structure provides better gate electrostatic control over the channel region than 3D device (e.g. bulk CMOS) and 2D device (e.g. fully depleted SOI) structures [19].

In terms of the device operation mechanism, CNFET can be categorized as either Schottky Barrier (SB) controlled FET (SB-CNFET) or MOSFET-like FET [3,4,20]. The conductivity of SB-CNFET is governed by the majority carriers tunneling through the SBs at the end contacts. The on-current and thereby device performance of SB-CNFET is determined by the contact resistance due to the presence of tunneling barriers at both or one of the source and drain contacts, instead of the channel conductance, as shown by Figure 1.8(a). The SBs at source/drain contacts are due to the Fermi-level alignment at the metal-semiconductor interface. Both the height and the width of the SBs, and therefore the conductivity, are modulated by the gate electrostatically. SB-CNFET shows ambipolar transport behavior [27]. The work function induced barriers at the end contacts can be made to enhance either electron or hole transport. Thus both the device polarity (n-type FET or p-type FET) and the device bias point can be adjusted by choosing the appropriate work function of source/drain contacts [21]. On the other hand, MOSFETlike CNFET exhibits unipolar behavior by suppressing either electron (pFET) or hole (nFET) transport with heavily doped source/drain. The non-tunneling potential barrier in the channel region, and thereby the conductivity, is modulated by the gate-source bias (Figure 1.8(b)).

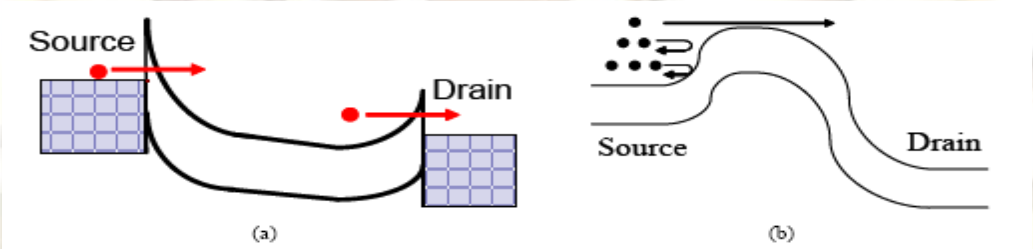


Figure 1.8: The energy band diagram for (a) SB-CNFET, and (b) MOSFET-like CNFET.

The first fabricated CNFET devices with Au or Pt source/drain metal contacts were reported in 1998 [22,23]. The gate dielectric material was a thick SiO2 layer. A highly doped Si back gate was used to control the conductivity. The Al2O3 gate dielectric was introduced to improve the gate controllability over the channel region [24]. The front gate device structure, by placing the gate electrode over the thin gate oxide that covers CNT, was used to further improve the channel electrostatics [25]. Better gate electrostatics was achieved by using high-*k*, e.g. HfO2, gate dielectric material [20,26].

The source/drain contacts using a variety of metals (Ti, Ni, Al, Pd, …) were fabricated to study the effect of the work function difference between the metal contacts and CNT on device conductivity. Ti source/drain metallization was reported to be efficient on reducing the contact resistance [27]. The device fabricated with Pd source/drain metal contact, Al gate electrode, and HfO2 gate dielectric was reported to achieve excellent dc characteristics [3]. Logic circuits with field-effect transistors based on single carbon nanotubes have beendemonstrated in the past few years. In 2001, [28] demonstrated one-, two-, and three CarbonNanotube Field-Effect Transistors transistor circuits that exhibit a range of digital logic operations, including an inverter, a logic NOR, a static random-access memory (SRAM) cell, and an three-stage ac ring oscillator operating at 5 Hz. A five-stage CMOS type nanotube ring oscillator using palladium p-type gates and aluminum n-type gates was reported in 2006 [29]. Owing to the compact device/circuit design, this ring oscillator works at a frequency of 72 MHz. Regarding RF analog application using CNFET, the first demonstration of ac gain in a single-walled carbon nanotube common-source amplifier was reported in 2006 [30]. The low frequency gain was ~ 11.3 dB, and the unity-gain frequency was about 560 kHz which was mostly limited by the parasitic load capacitance. While the CNT synthesis / fabrication technique and the performance of CNFET devices and circuits have been significantly improved since the first fabricated device in 1998, CNFETs is still premature for very large scale integrated (VLSI) circuits design and commercial use. In order for CNFET to develop into a technology, first, we need tools to enable circuit design and performance benchmarking. Efforts have been made in recent years on modeling semiconducting CNFET [31,32,33,34] for digital logic applications and CNT for interconnects [35,36] in order to evaluate the

potential performance at the device level. This thesis will mostly focus on the device applications of CNT. A numerical model was reported in [37] to evaluate the dc current of SB-CNFET. The model reported in [38] predicts the dc performance of short channel SB-CNFET. Though good dc current can be achieved by SB-CNFET with the self-aligned structure [3,37,38], its ac performance is going to be poor due to the proximity of the gate electrode to the source/drain metal. The ambipolar behavior of SBCNFET also makes it undesirable for complementary logic design. Considering both the fabrication feasibility [39] and superior device performance of MOSFET-like CNFET as compared to SB-CNFET, we will focus on MOSFET-like CNFETs. To evaluate the device/circuit performance as well as the performance dependence on device/geometry parameters, the requirements for a good device model include:

(1) Good scalability.
(2) Physics-based, or at least semi-physics based.
(3) Reasonable accuracy for both large signal and small signal analysis.
(4) Acceptable run time.

The reported compact models to date [31,32,33,34] used one or more lumped static gate capacitances and assumed an ideal ballistic transport channel. These simplifications make it questionable when evaluating the transient response and device dynamic performance.

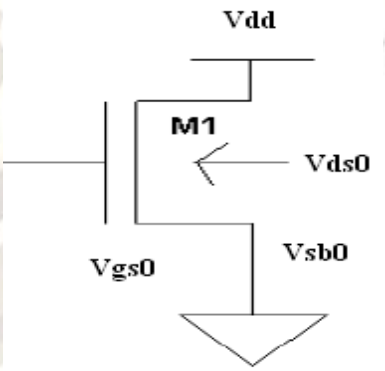
The integral function used in [31,32] requires intensive calculation efforts and thereby makes it difficult to implement in circuit simulators, e.g. HSPICE [40]. The model in [33] improves the run time significantly by using a polynomial fitting approach. This methodology dilutes the physical meaning of the device model and makes evaluating CNFET performance with different device parameters (e.g. CNT chiralities, gate oxide thickness) inconvenient. The reported models to date [31,32,34] used a simple coaxial or planer gate structure that differs from the typical realistic CNFET gate structure that consists of high-*k* gate oxide on top of SiO2 insulating bulk [26]. For a CNFET with multiple parallel CNTs [3], these published models cannot examine the multiple CNT-to-CNT screening effect on both the driving current and the effective gate capacitance [41].

All the reported device models assumed CNFET devices with perfect and ideal CNT channel. Compared to the intrinsic performance of CNFET predicted by theoretical studies [31], the actual device and circuit level performance is mostly limited by various parasitics and process induced imperfections. The device parasitics and/or non-idealities include, but are not limited to: the channel length dependence of current drive, the finite scattering mean free path, the source/drain series resistance, the source/drain contacts (SBs) resistance, the geometry dependence of the gate to channel capacitance, and the interconnect wiring capacitance. To evaluate CNFET device/circuit performance with improved accuracy, a CNFET device model with a more complete circuit-compatible structure and also incorporating the typical device/circuit non-idealities is necessary. A good balance between the simulation run-time and accuracy is desired.

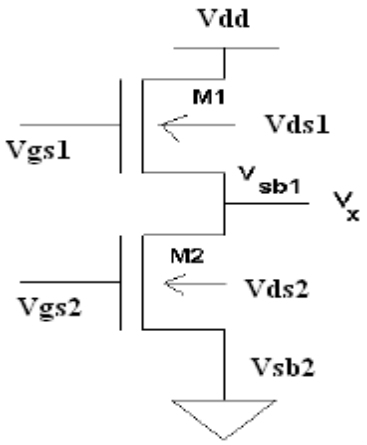
The circuit macro level performance is not only limited by the performance of one single device, but also limited by the device performance variations which are significant for nanometer scale devices [42]. There are a variety of device parameter variations and imperfections caused by today's CNT synthesis/fabrication technique: (1) CNT diameter and chirality control [43]; (2) Doping level control [39]; (3) The probability of a CNT to be metallic [12,44]; (4) Directed-CNT-growth [45,46]. A reasonable question to ask is: considering these imperfections, what can be gained at the circuit-level using CNFET technology compared to cutting-edge Si CMOS? Finally, in order for CNFET to develop into a competitive technology, it should have good scalability, i.e. the performance advantage of CNFET over MOSFET is expected to improve (or at least maintain the same) as the technology node advances.

III. FORCED STACK BAICS

Stacking transistor can reduce sub-threshold leakage [9]. So it is called stacked effect. Where two or more stacked transistor is turned off together, the result can reduce the leakage power. The effect of stacking on reducing leakage can be understood from the Fig. 2.



(a)



(b)

Fig. 2: (a) Single Transistor (b) Forced Stack Transistor

If the input is '0', then both transistor M1 and M2 are turned off. Here Vx is the intermediate node voltage between M1 and M2. Transistor M2 has its internal resistance. Due to this resistance Vx is greater than the ground potential. This positive Vx results in a negative gate-source (Vgs) for the M1 transistor and the negative source-base voltage (Vsb) for M1. Here M1 also has a reduced drain-source voltage (Vds), which lower the drain induced barrier lowering (DIBL) effect. These three effects together reduced the the leakage power. The Figure 3 also illustrates the concept of Stacking effect.

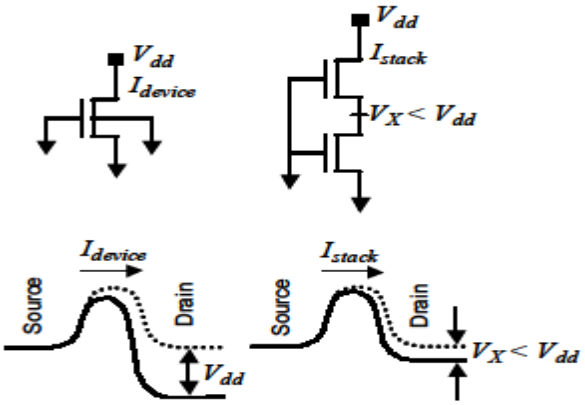


Fig. 3: Leakage current difference between a single OFF device and a stack of two OFF devices.

IV. THE PROPOSED FORCED STACK CNTFET INVERTER

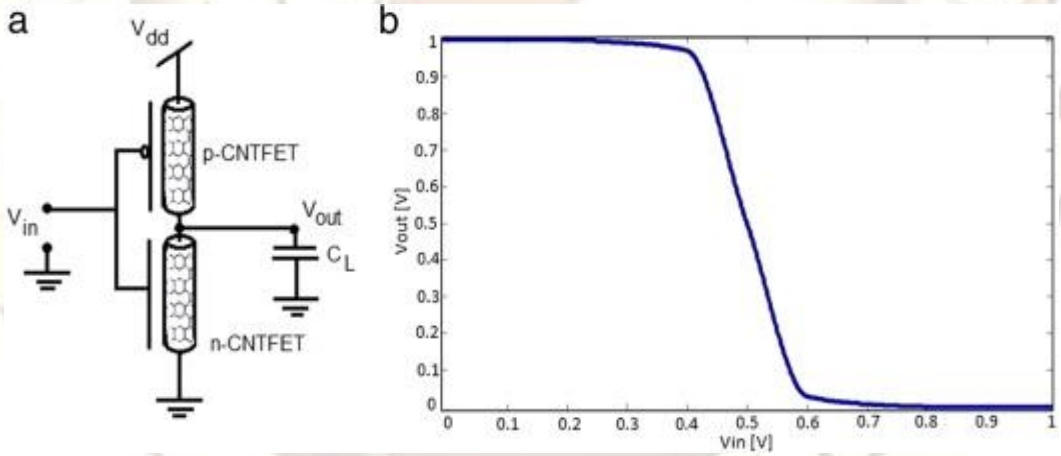


Fig 4 (a) cntfet inverter and (b) cntfet inverter dc characteristics

Fig 4(a) shows the normal cntfet inverter and 4(b) shows the cntfet inverter dc characteristics

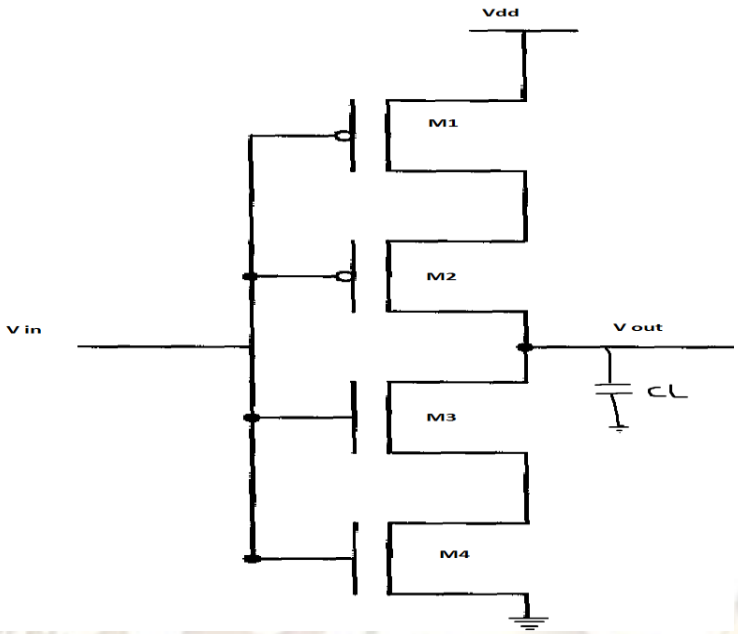


Fig 5 : Forced stacking CNTFET inverter.

Fig. 5 shows a inverter based on CNTFETs using Forced Stack Technique to reduce leakage power. Two pairs of Stack transistors (M1, M2 and M3, M4) are used in the inverter cell. Here M1 and M2 are stacking similarly M3 and M4 are stacking. The effect of stacking the transistor results in the reduction of subthreshold leakage current when two or more transistors are turned off together[17]. But we are lowering the supply voltage of both type of inverter and analyzing the average power and pdp of both cntfet and force stacking cnfet inverter. In this design 1 tube is used for each M1,M2,M3 and M4 force stack cntfet inverter and 1 tube in each cntfet of other cntfet inverter beside forced stacking inverter.

V. SIMULATION RESULTS

The proposed inverter cell based on CNTFETs is designed and simulated using the Synopsis HSPICE. Simulations performed with Stanford CNTFET model at 32nm feature size with supply voltage VDD of 0.9V,0.8 and 0.7 [15]. The following technology parameters are used for simulation of inverter using CNTFET Technology [16]:

- Physical channel length (L_channel) = 32.0nm.
- The length of doped CNT source/drain extension region (L_sd) = 32.0nm.
- Fermi level of the doped S/D tube (Efo) = 0.6 eV.
- The thickness of high-k top gate dielectric material (Tox) = 4.0nm.
- Chirality of tube (m,n) = (19,0).
- CNT Pitch = 10nm.
- Flatband voltage for n-CNTFET and p-CNTFET (Vfbn and Vfbp) = 0.0eV and 0.0eV.
- The mean free path in intrinsic CNT (Lceff) = 200.0nm.
- The mean free path in p+/n+ doped CNT = 15.0nm.
- The work function of Source/Drain metal contact = 4.6eV.
- CNT work function = 4.5eV.

The HSPICE avanwaves is used for displaying and measuring simulation parameters. Average power and PDP of both CNTFET inverter Cell with Forced stack Transistors and CNTFET inverter cell without forced stack Transistors are summarized in Table 1 and Table 2.

CNTFET Forced stacking inverter is better than normal CNTFET inverter without Forced stacking in average power by 15% at 0.9 supply voltage. Similarly At supply voltage 0.8v Force stacking CNTFET inverter average power is 13.204% better than CNTFET inverter without force stacking inverter. At supply voltage 0.7 v Force stacking CNTFET inverter average power is 13.116% better than CNTFET without Force stacking inverter.

CNFET INVERTER WITHOUT FORCE STACKING
TABLE 1

VDD	AVG P.	PDP
0.9 V	3.5542E-05	2.0927E-13
0.8	2.7870E-05	1.5583E-13

0.7	2.1240E-05	1.1622E-13	0.7	1.8454E-05	1.8391E-13
0.6	1.5682E-05	8.5448E-14	0.6	1.3090E-05	1.2094E-13
0.5	1.0694E-05	5.8021E-14	0.5	7.9659E-06	7.1638E-14
0.4	6.2077E-06	3.3506E-14	0.4	3.6719E-06	3.2462E-14
0.3	6.2077E-06	3.3506E-14	0.3	1.4864E-06	1.2908E-14

The wave form of CNTFET inverter with Forced stacking and CNTFET inverter without Forced stacking at different supply voltage are as shown in fig 1,2,3,4,5,and 6.

CNFET INVERTER WITH FORCE STACKING
TABLE 2

VDD	AVG P.	PDP
0.9V	3.0061E-05	3.6991E-13
0.8	2.4190E-05	2.6666E-13

Fig1(a),(b),(c) and (d) : waveform of inverter without force stacking at different supply voltage.

Fig1 (a) waveform of inverter without force stacking at 0.9 supply voltage and input voltage 0.9v.

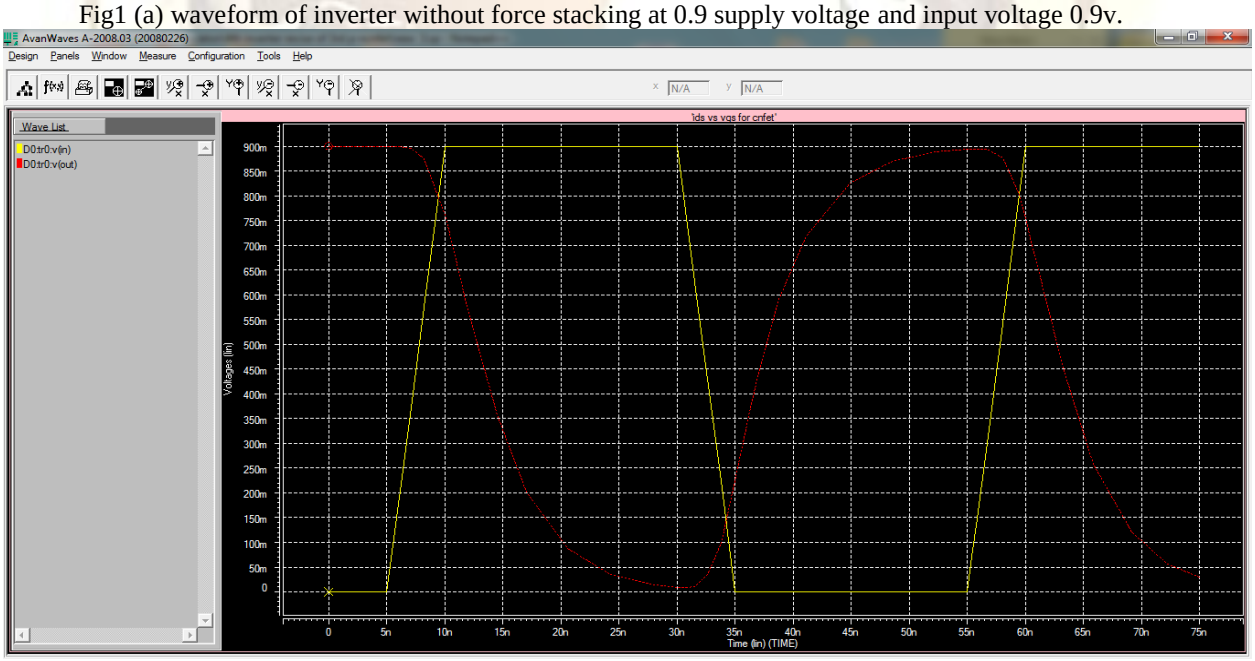


Fig1 (b) waveform of inverter without force stacking at 0.8 supply voltage and input voltage 0.9v.

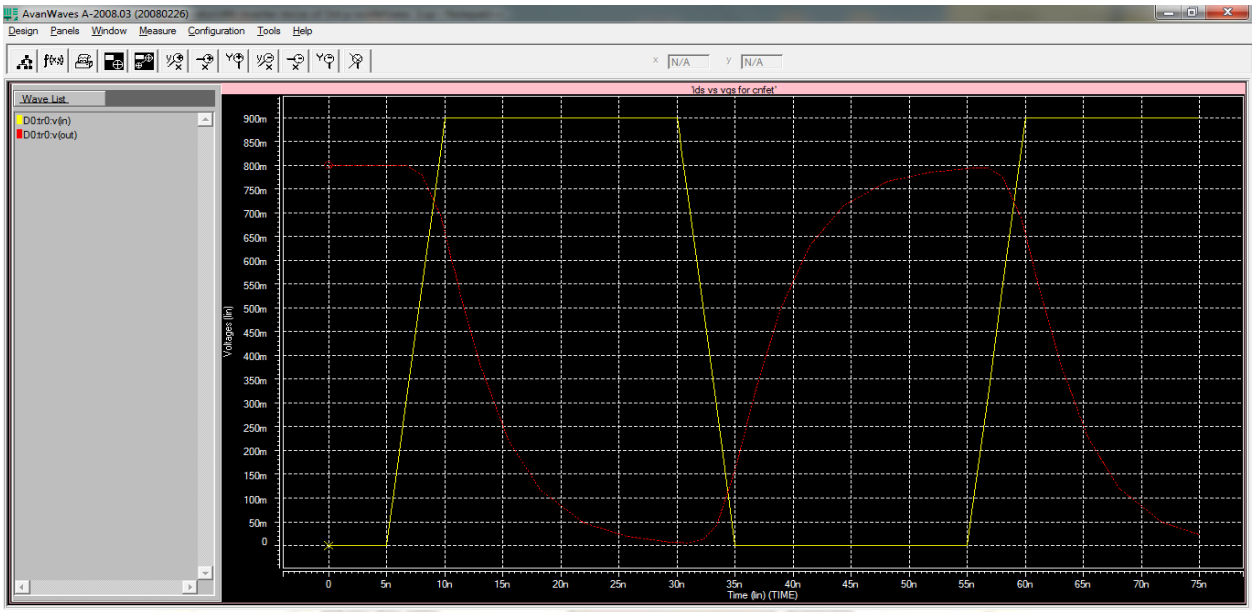


Fig1 (c) waveform of inverter without force stacking at 0.7 supply voltage and input voltage 0.9v.

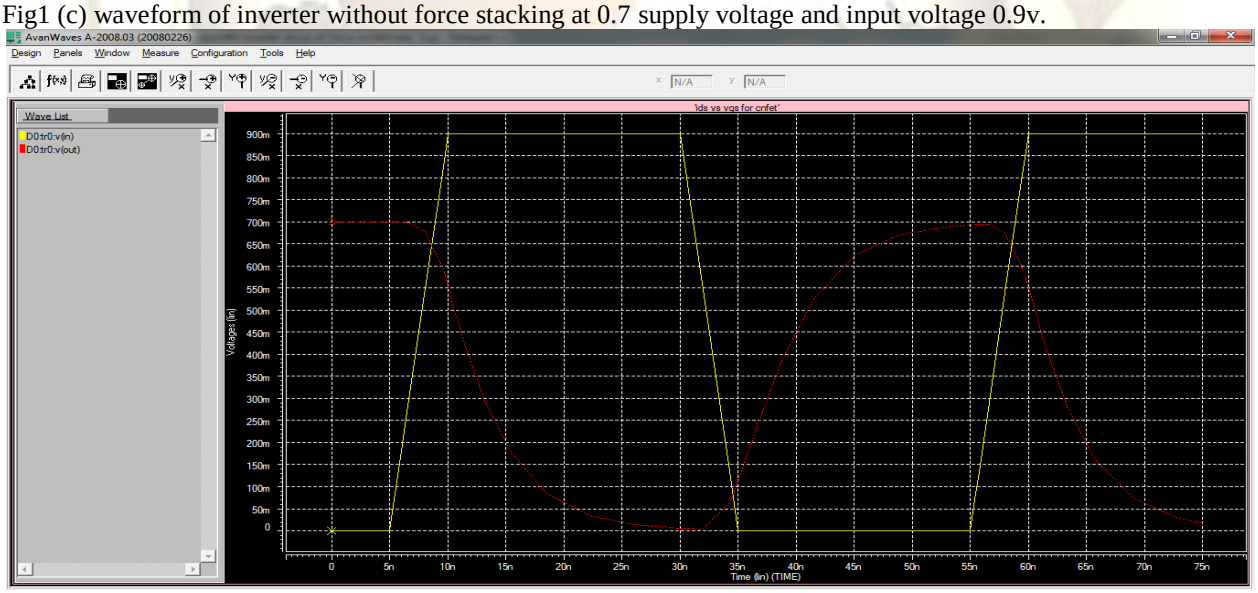


Fig1 (d) waveform of inverter without force stacking at 0.6 supply voltage and input voltage 0.9v.

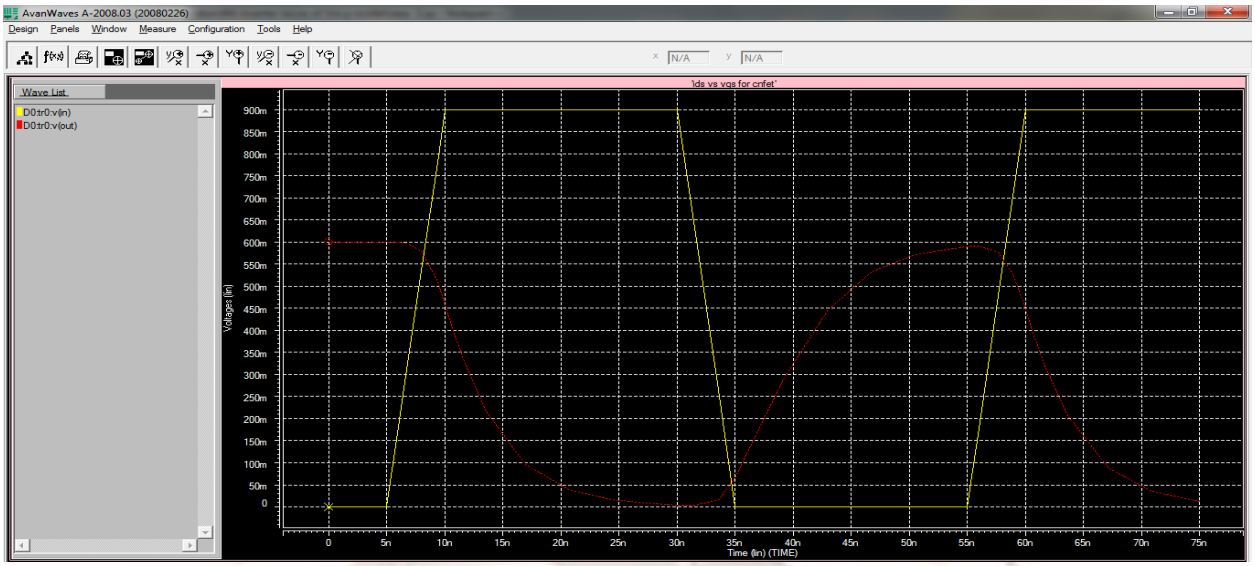


Fig2 (a),(b),(c) and (d) : waveform of inverter without force stacking at different supply voltage.

Fig2 (a) waveform of inverter with force stacking at 0.9 supply voltage and input voltage 0.9v.

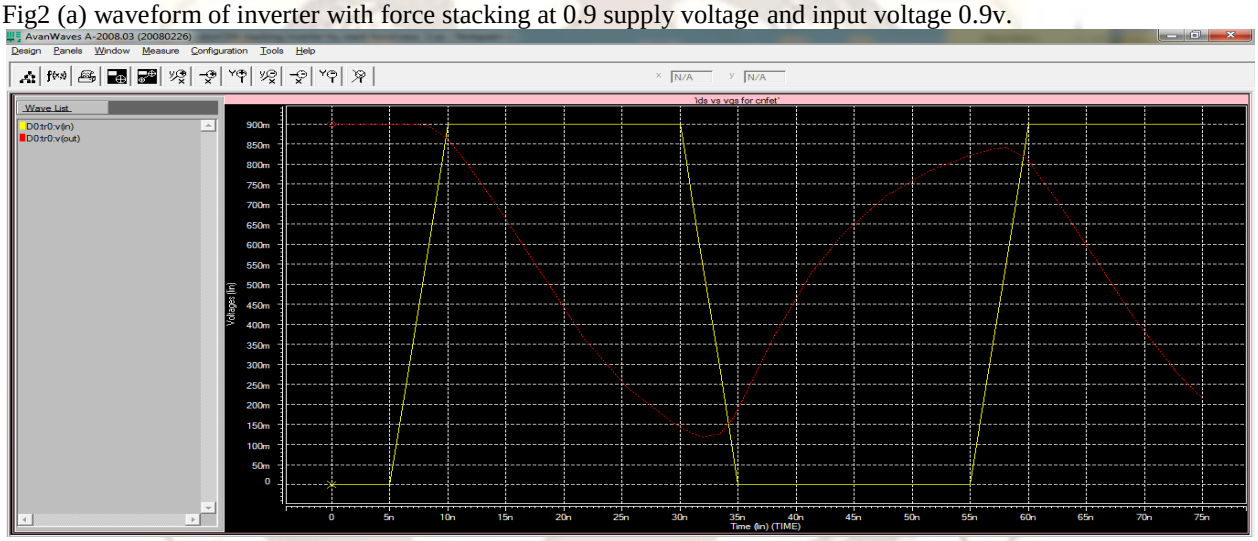


Fig2 (b) waveform of inverter with force stacking at 0.8 supply voltage and input voltage 0.9v.

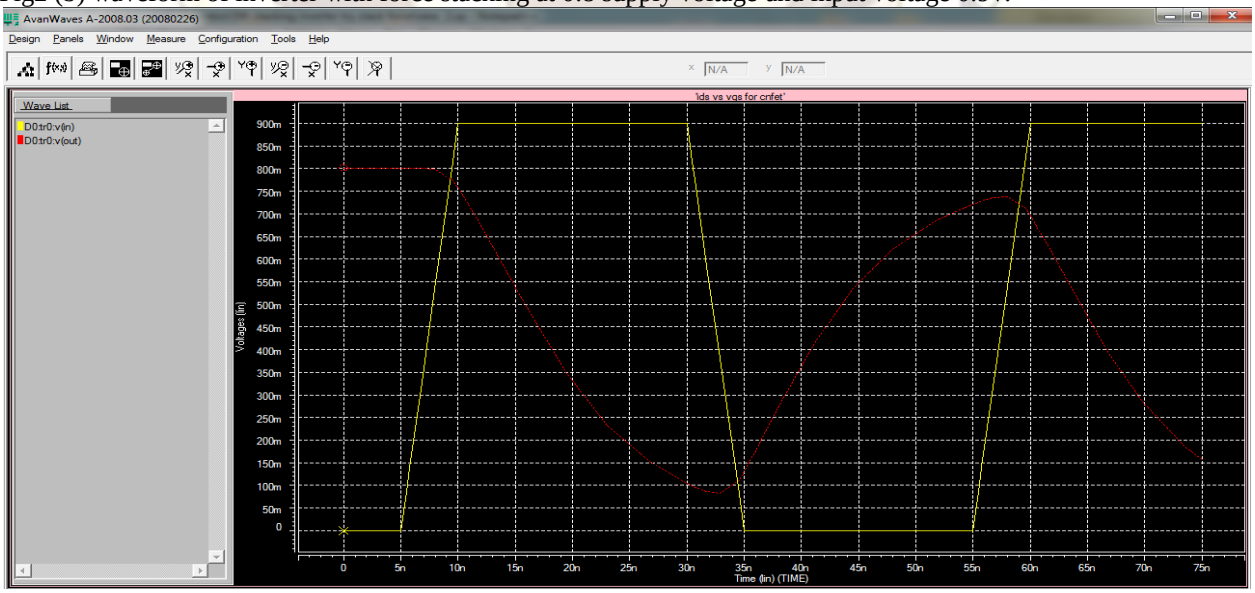


Fig2 (c) waveform of inverter with force stacking at 0.7 supply voltage and input voltage 0.9v.

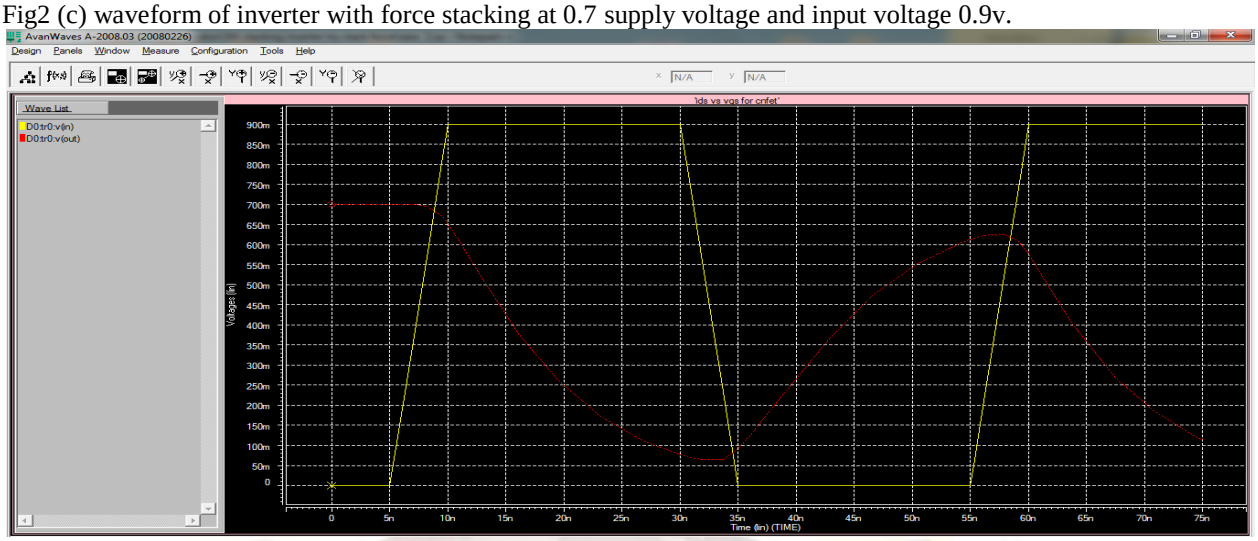
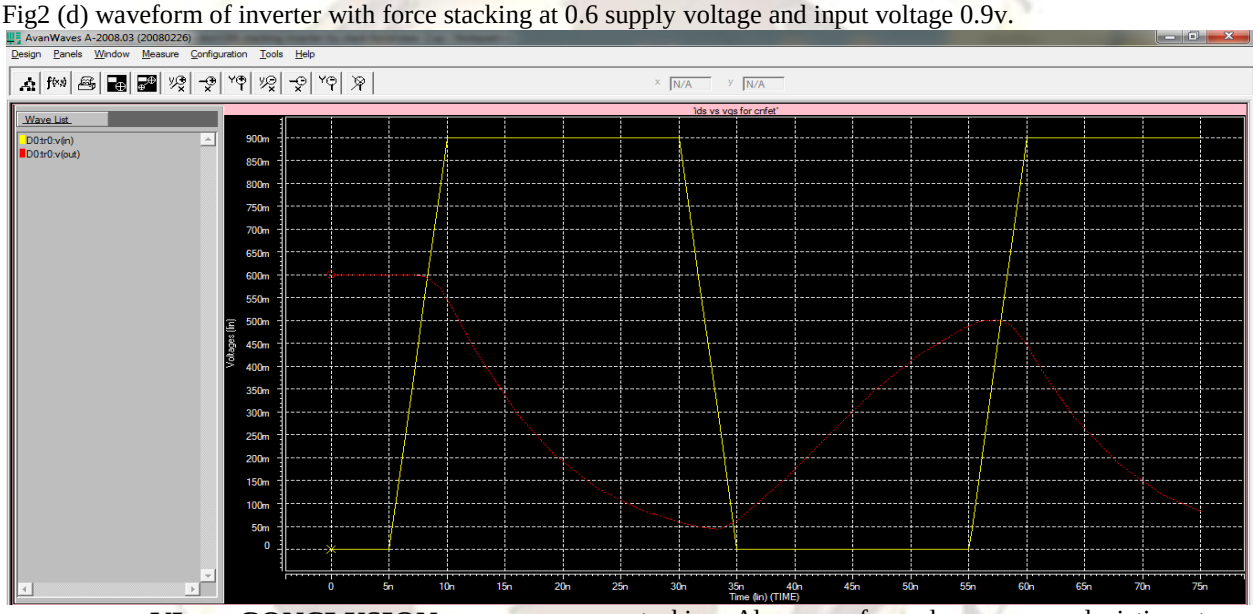


Fig2 (d) waveform of inverter with force stacking at 0.6 supply voltage and input voltage 0.9v.



VI. CONCLUSION

Carbon nanotube electronics remains a very promising route to solve future down-scaling problems of conventional silicon technology. In this paper a CNTFET inverter using Forced Stack technique and without force stack technique is designed and simulated using HSPICE with Stanford CNFET Model at 32nm Technology at low supply voltage. The results shows that this proposed Forced Stack CNTFET SRAM cell reduces average power and PDP to the significant effect compared to CNTFET inverter without force stack technique. Table 1 and Table 2 shows that average power and PDP reduce while lowering the supply voltage in CNTFET inverter without force stacking , compare to force stacking technique inverter average power and PDP is reduce much lower while lowering the supply voltage. This data shows that force stack technique inverter proposed design is better in average power and PDP than CNTFET inverter without forced stacking. Also wave form shows no any deviation at different supply voltage.

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