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MODELING OF SINGLE-PHASE TO THREE-PHASE DRIVE SYSTEM USING TWO PARALLEL CONVERTERS ON INPUT SIDE

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Abstract

The objective is to supply a three phase motors from a single phase AC mains. It is common to have only a single phase power grid in residential, commercial, manufacturing and mainly in rural areas, while adjustable speed drives may require a three phase power grid. Hence we need to convert from single phase to three phase supply to operate the drive system. Parallel converters can be used to improve the power capability, reliability, efficiency and redundancy. Parallel converter techniques can be employed to improve the performance of active power filters, uninterruptable power supplies, fault tolerance of doubly fed induction generators and three phase drives. When an isolation transformer is not used, the reduction of circulating currents among different converter stages is an important objective in the system design. This work proposes a single phase to three phase drive system composed of two parallel single phase rectifiers, an induction motor and three phase inverter. The proposed system permits to reduce the rectifier switch currents, the total harmonic distortion (THD) of the grid current with same switching frequency and to increase the fault tolerance characteristics. Even with the increase in the number switches, the total energy loss of the proposed system is lower than that of conventional system. The model of the system will be derived. A suitable control strategy and pulse width modulation technique (PWM) will be developed. The complete comparison between the proposed and standard configurations will be carried out in this work. Simulation of this project will be carried out by using MATLAB/ Simulink.

Index Terms— Ac-dc-ac power converter, 3-phase Ac motor drive, parallel *converter*.

I. INTRODUCTION

A wide variety of commercial and industrial electrical equipment requires three-phase power. Electric utilities do not install three-phase power as a matter of course because it cost significantly more than single-phase installation. Hence we need to conversion from single-phase to three-phase. Parallel converters have been used to improve the power capability, reliability, efficiency, and redundancy. Usually the operation of converters in parallel requires a transformer for isolation. However, weight, size, and cost associated with the transformer may make such a solution undesirable [1]. When an isolation transformer is not used, the reduction of circulating currents among different converter stages is an important objective in the system design [2]–[7].

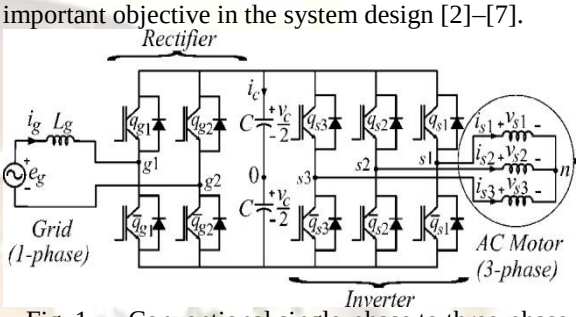

Fig. 1. Conventional single-phase to three-phase drive system.

Several solutions have been proposed when the objective is to supply three-phase motors from single-phase ac mains [8]–[16]. It is quite common to have only a single-phase power grid in residential, commercial, manufacturing, and mainly in rural areas, while the adjustable speed drives may request a three-phase power grid. Single-phase to three-phase ac–dc–ac conversion usually employs a full-bridge topology, which implies in ten power switches, as shown in Fig.1. This converter is denoted here as conventional topology. In this paper, a single-phase to three-phase drive system composed of two parallel single-phase rectifiers and a three-phase inverter is proposed, as shown in Fig. 2.

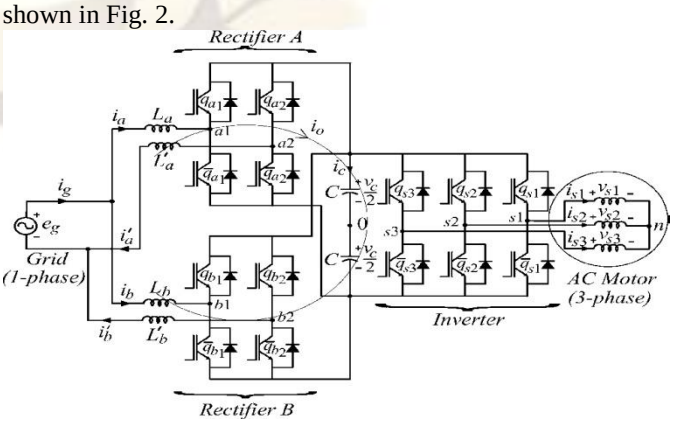

Fig.2. Proposed single-phase to three-phase drive system.

The proposed system is conceived to operate where the single-phase utility grid is the unique option available. Compared to the conventional topology, the proposed system permits: to reduce the rectifier switch currents; the total harmonic distortion (*THD*) of the grid cur-rent with same switching frequency or the switching frequency with same *THD* of the grid current; and to increase the fault tolerance characteristics. In addition, the losses of the proposed system may be lower than that of the conventional counterpart. The aforementioned benefits justify the initial investment of the proposed system, due to the increase of number of switches.

II. PWM METHOD

Considering that v_a^*,v_b^* and v_o^* denote the reference voltages determined by the current controllers. i,e,

$$v_a^* = v_{a10}^* - v_{a20}^* \quad (1)$$

$$v_b^* = v_{b10}^* - v_{b20}^* \quad (2)$$

$$v_o^* = v_{a10}^* + v_{a20}^* - v_{b10}^* - v_{b20}^* \quad (3)$$

The gating signals are directly calculated from the reference pole voltages v_{a10}^*, v_{a20}^*, v_{b10}^* and v_{b20}^*.

Introducing an auxiliary variable $v_x^* = v_{a20}^*$ and solving this system of equations,

$$V_{a10}^* = v_a^* + v_x^* \quad (4)$$

$$V_{a20}^* = v_x^* \quad (5)$$

$$V_{b10}^* = (v_a^*/2) + (v_b^*/2) - (v_o^*/2) + v_x^* \quad (6)$$

$$V_{b20}^* = (v_a^*/2) - (v_b^*/2) - (v_o^*/2) + v_x^* \quad (7)$$

From these equations, it can be seen that, besides v_a^* , v_b^* and v_o^*, the pole voltages depend on also of v_x^* . The limit values of the variable v_x^* can be calculated by taking into account the maximum $v_c^*/2$ and minimum $-v_c^*/2$ value of the pole voltages

$$V_{xmax}^* = (v_c^*/2) - v_{max}^* \quad (8)$$

$$V_{xmin}^* = (-v_c^*/2) - v_{min}^* \quad (9)$$

Introducing a parameter μ ($0 \le \mu \le 1$), the variable v_x^* can be written as,

$$V_x^* = \mu V_{xmax}^* + (1- \mu)V_{xmin}^* \quad (10)$$

Once v_x^* is choosen, pole voltages v_{a10}^*, v_{a20}^*, v_{b10}^* and v_{b20}^*.are defined from (4) to (7).The parameter μ changes the place of the voltage pulses related to v_a and v_b. And also μ influences the harmonic distortion of the voltages generated by the rectifier.

III. SYSTEM DESIGN

To avoid the circulating current, the following three approaches are used commonly

1) Isolation. In this approach, the overall parallel system is bulky and costly because of additional power supplies or the ac line-frequency transformer.

2) High impedance. They cannot prevent a low-frequency circulating current.

3) Synchronized control. This approach is not suitable for modular converter design. When more converters are in parallel, the system becomes very complicated to design and control.

In this proposed method the system is designed to reduce the circulating current (i_o).

From fig.2 . the following equations can be derived for the front end rectifier

$$V_{a10} - V_{a20} = e_g - (r_a+l_ap)\, i_a - (r'_a+l'_ap)\, i'_a \quad (11)$$

$$V_{b10} - V_{b20} = e_g - (r_b+l_bp)\, i_b - (r'_b+l'_bp)\, i'_b \quad (12)$$

$$V_{a10} - V_{b10} = (r_a+l_ap)\, i_a - (r_b+l_bp)\, i_b \quad (13)$$

$$V_{a20} - V_{b20} = (r'_a+l'_ap)\, i'_a - (r'_b+l'_bp)\, i'_b \quad (14)$$

$$i_g = i_a + i_b = i'_a + i'_b \quad (15)$$

where $p = d/dt$ and symbols like r and l represent the resistances and inductances of the input inductors.The circulating current i_o can be defined from i_a and i'_a or i_b and i'_b i.e.

$$i_o = i_a - i'_a = - i_b + i'_b \quad (16)$$

By solving the above equations ,

$$V_a = e_g - [r_a + r'_a + (l_a+l'_a)p]\, i_a + (r'_a+ l'_ap) \quad (17)$$

$$V_b = e_g - [r_b + r'_b + (l_b+l'_b)p]\, i_b + (r'_b+ l'_bp)\, i_o \quad (18)$$

$$V_o = - [\, r'_a + r'_b + (l'_a + l'_b)p]\, i_o - [r_a - r'_a + (l_a - l'_a)p]\, i_a + [r_b - r'_b + (l_b - l'_b)p]\, i_b \quad (19)$$

where

$$V_a = V_{a10} - V_{a20} \quad (20)$$

$$V_b = V_{b10} - V_{b20} \quad (21)$$

$$V_o = V_{a10} + V_{a20} - V_{b10} - V_{b20} \quad (22)$$

In order to both facilitate the control and share equally current, voltage, power between the rectifiers, the four inductors should be equal . i.e. $r'_g = r_a = r'_a = r_b = r'_b$ and $l'_g = l_a = l'_a = l_b = l'_b$.In this case the model (17)-(19) can be simplified to the model given by

$$V_a + V_o/2 = e_g - 2(r'_g+l'_gp)\, i_a \quad (23)$$

$$V_b - V_o/2 = e_g - 2(r'_g+l'_gp)\, i_b \quad (24)$$

$$V_o = -2(r'_g+l'_gp)\, i_o \quad (25)$$

$$V_{ab} = (V_a + V_b)/2 = e_g - (r'_g+l'_gp)\, i_a \quad (26)$$

$$V_a - V_o/2 = e_g - 2(r'_g+l'_gp)\, i'_a \quad (27)$$

$$V_b + V_o/2 = e_g - 2(r'_g+l'_gp)\, i'_b \quad (28)$$

In this ideal case, the circulating current can be reduced to zero imposing

$$V_o = V_{a10} + V_{a20} - Vb10 - V_{b20} = 0 \quad (29)$$

When $i_a = 0$ then $i_a = i'_a$ and $i_b = i'_b$ and the system model (17)-(19) reduced to

$$V_a = e_g - 2(r'_g+l'_gp)\, i_a \quad (30)$$

$$V_b = e_g - 2(r'_g+l'_gp)\, i_b \quad (31)$$

IV. SYSTEM CONTROL

The gating signals are obtained by comparing pole voltages with one (v_{t1}), two (v_{t1} and v_{t2}) or more high-frequency triangular carrier signals [17]–[20]. In the case of double-carrier approach, the phase shift of the two triangular carrier signals (v_{t1} and v_{t2}) is 180^0. The parameter μ changes the place of the voltage pulses related to v_a and v_b . When $v_x^* = v_x^*{}_{min}$ ($\mu = 0$) or $v_x^* = v_x^*{}_{max}$ ($\mu = 1$) are selected, the pulses are placed in the begin or in the end of half period (T_s) of

the triangular carrier signal.

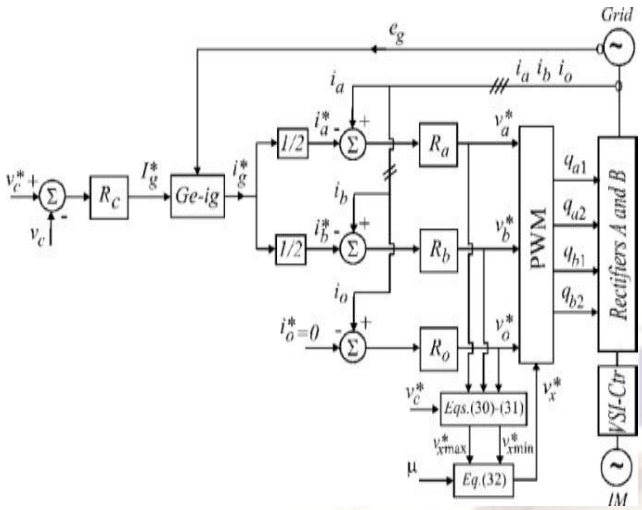

Fig. 3. Control block diagram.

The control block diagram of Fig. 2, highlighting the control of the rectifier. To control the dc-link voltage and to guarantee the grid power factor close to one. Additionally, the circulating current i_o in the rectifier of the proposed system needs to be controlled.

In this way, the dc-link voltage v_c is adjusted to its reference value v_c^* using the controller R_c , which is a standard PI type controller. This controller provides the amplitude of the reference grid current I_g^*. To control power factor and harmonics in the grid side, the instantaneous reference current I_g^* must be synchronized with voltage e_g , as given in the voltage-oriented control (VOC) for three-phase system. This is obtained via blocks *Ge-ig*, based on a PLL scheme. The reference currents $i_a^*$and i_b^* are obtained by making $i_a^* = i_b^* = I_g^* /2$, which means that each rectifier receives half of the grid current. The control of the rectifier currents is implemented using the controllers indicated by blocks R_a and R_b . These current controllers define the input reference voltages $v_a^*$and v_b^*.

The homopolar current is measured (i_o) and compared to its reference ($i_o^* = 0$). The error is the input of PI controller R_o , that determines the voltage v_o^*. The motor there-phase voltages are supplied from the inverter (VSI). Block VSI-Ctr indicates the inverter and its control. The control system is composed of the PWM command and a torque/flux control strategy (e.g., field-oriented control or volts/hertz control).

V. COMPARISION OF THD'S

Topology (PWM)	THD_p/THD_c
Proposed (S-Ca μ = 0.5)	0.035
Proposed (D-Ca μ = 0.5)	0.041
Proposed (D-Ca μ = 0)	0.012

The dc-link capacitor current behavior is examined in this section. The proposed converter using double-carrier with $\mu = 0$ provides the best reduction of the high frequency harmonics. The highest reduction of *THD* is obtained for the converter using double-carrier with $\mu = 0$ and the *THD* obtained for $\mu = 1$ is equal to that for $\mu = 0$.

By observing the above table we can say that the proposed method has lesser THD, when compared to conventional one .And also from the above table it is said that the THD of proposed one is lesser at double carrier μ=0,when compared to single carrier μ=0.5 and double carrier μ=0.5.

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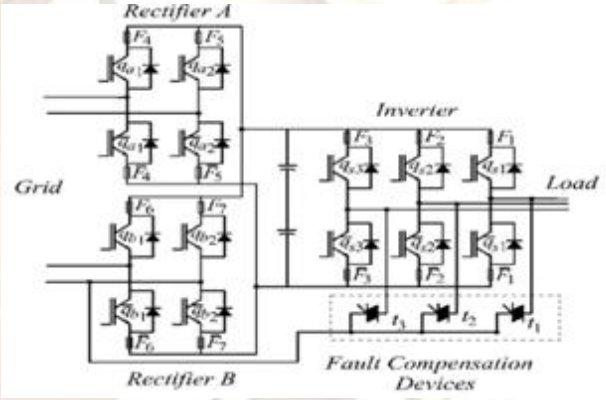
VI. COMPENSATION OF FAULT

Fig. 4. Proposed configuration highlighting devices of



fault tolerant system

The fault compensation is achieved by reconfiguring the power converter topology with the help of isolating devices (fast active fuses—F_j , j = 1, . . . , 7) and connecting devices (back-to-back connected SCRs—t_1 , t_2 , t_3), as observed in Fig. 4 and discussed in [21]–[24]. These devices are used to redefine the post-fault converter topology, which allows continuous operation of the drive after isolation of the faulty power switches in the converter. Fig. 5 presents the block diagram of the fault diagnosis system. In this figure, the block fault identification system (FIS) detects and locates the faulty switches, defining the leg to be isolated. This control system is based on the analysis of the pole voltage error.

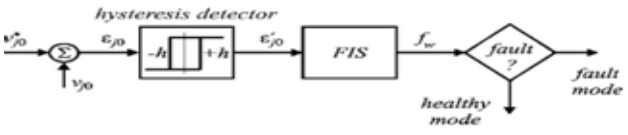


Fig.5. Block diagram of the fault diagnosis system.

The proposed system can provide compensation for open-circuit and short-circuit failures occurring in the rectifier or inverter converter devices
The fault detection and identification is carried out in four steps:

1) measurement of pole voltages ($v_{j\,0}$);
2) computation of the voltage error $\varepsilon_{j\,0}$ by comparison of reference voltages and measurements affected in Step 1);
3) determination as to whether these errors correspond or not to a faulty condition; this can be implemented by the hysteresis detector shown in Fig. 5;
4) Identification of the faulty switches by using $\varepsilon^{3}_{j\,0}$

This way, four possibilities of configurations have been con-sidered in terms of faults:

1) pre-fault ("healthy") operation [see Fig. 6(a)];
2) post-fault operation with fault at the rectifier B [see Fig. 6(b)];
3) post-fault operation with fault at the rectifier A [see Fig. 6(c)];
4)
4) post-fault operation with fault at the inverter [see Fig. 6(d)].
5)

When the fault occurrence is detected and identified by the control system, the proposed system is reconfigured and becomes similar to that in Fig. 1.

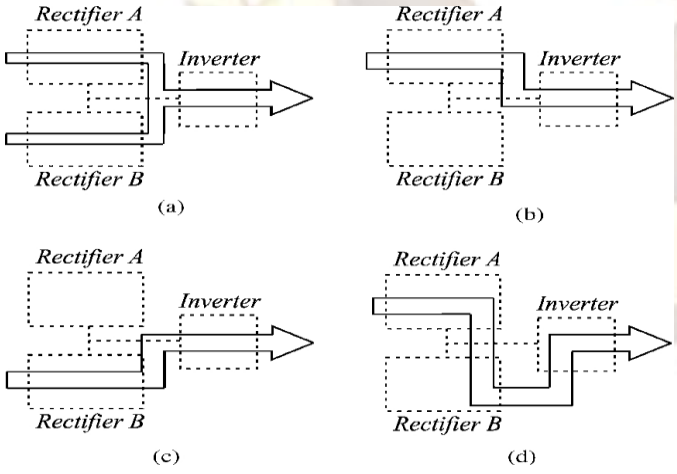


Fig. 6. Possibilities of configurations in terms of fault occurrence. (a) Pre-fault system. (b) Post-fault system with fault at the rectifier B. (c) Post-fault system with fault at the rectifier A. (d) Post-fault system with fault at the inverter.

VII. EFFICIENCY TABLE

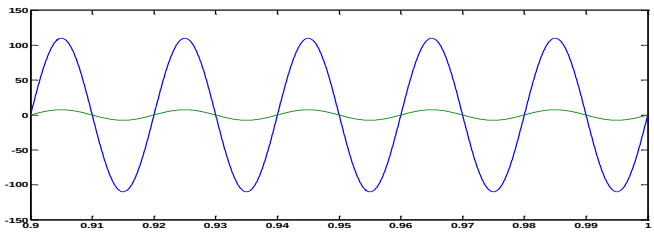
η_p/η_c -1			
Frequency/Inductor	S-Ca μ = 0.5	D-Ca μ = 0.5	D-Ca μ = 0
5 kHz/ ($L'_g = L_g$)	-0.75 %	-0.29 %	1.61 %

By observing the above table we can conclude that the efficiency of proposed system has better at D-Ca μ = 0 as compared with the conventional system at the same operating conditions.
The initial investment of the proposed system is higher than that of the standard one, since the number of switches and de-vices such as fuses and triacs is highest. But, considering the scenario when faults may occur, the drive operation needs to be stopped for a nonprogrammer maintenance schedule. The cost of this schedule can be high and this justifies the high initial investment inherent of fault-tolerant motor drive systems. On the other hand, the initial investment can be justified if the *THD* of the conventional system is a a critical factor.

VIII. SIMULATION RESULTS

The steady-state simulation results are shown in Fig. 7. The waveforms in this figure are: (a) voltage and current of the grid, (b) dc-link voltage, (c) currents of rectifier A and circulating current, (d) currents of rectifiers A and B, and (e) load line voltage. Note that, with the proposed configuration, all control demanded for single-phase to three-phase converter has been established. the proposed configuration provides current reduction in the rectifier side (half of the current of the standard topology) [see Fig. 7(d)], which can provide loss reduction. Also, the control guarantees the circulating current close to zero [see Fig. 7(c)].

The same set of simulation results was obtained for transient in the
machine voltages, as observed in Fig. 8
Simulation results presented in Fig. 9 show the behavior of variables of the proposed system when fault is detected in rectifier B. In this case, after fault detection given by the control system, the rectifier B has been isolated and the total flux of energy flows through rectifier A.



(a)

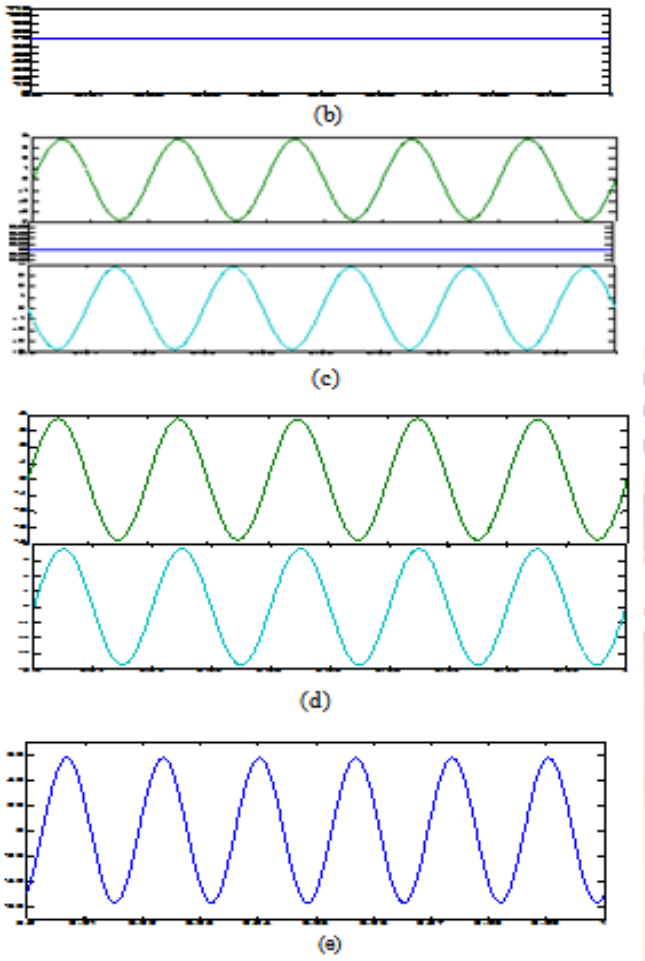


Fig. 7. Steady-state simulation results. (a) Grid voltage (e_g) and gird current (i_g). (b) Capacitor voltage (v_c). (c) Currents of rectifier A (i_a and i^*_a) and circulating current (i_o). (d) Currents of rectifiers A (i_a) and B (i_b). (e) Line voltage of the load ($v_{s\,2\,3}$).

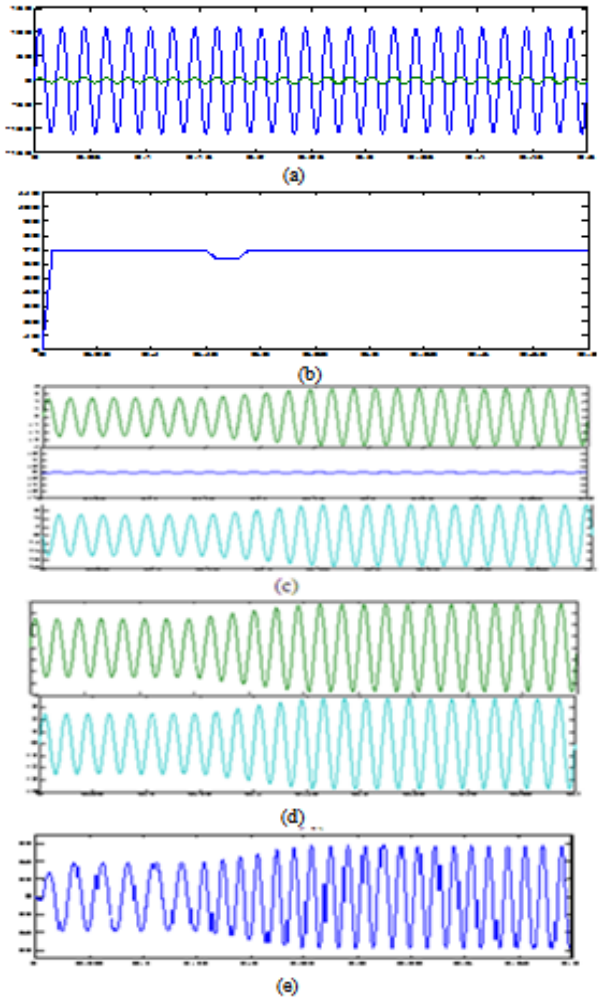
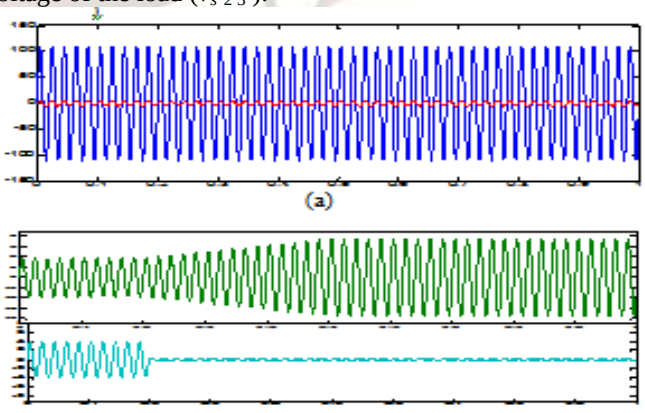


Fig. 8. Simulation results for a volts/hertz transient applied to the three-phase motor. (a) Grid voltage (e_g) and gird current (i_g). (b) Capacitor volt-age (v_c). (c) Currents of rectifier A (i_a and i^*_a) and circulating current (i_o).
(d) Currents of rectifiers A (i_a) and B (i_b). (e) Line voltage of the load ($v_{s\,2\,3}$).



(b)

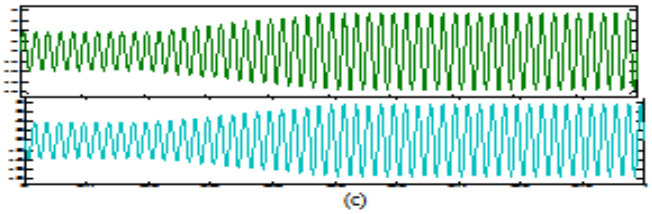


Fig. 9. Simulation results of the proposed configuration when a fault is identified at the rectifier B. (a) Grid voltage (e_g) and grid current (i_g).(b) Currents of rectifiers A (i_a) and B (i_b). (c) Currents of rectifier A (i_a and i^*_a).

IX. CONCLUSION

The system combines two parallel rectifiers without the use of transformers. The system model and the control strategy, including the PWM technique, have been developed.

The complete comparison between the proposed and standard configurations has been carried out in this work. Compared to the conventional topology, the proposed system permits to reduce the rectifier switch currents, the *THD* of the grid current and to increase the fault tolerance characteristics.
The simulation results have shown that the system is con-trolled properly, even with transient and occurrence of faults

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BIOGRAPHIES

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