Muniraja Thoti, Jagadeeshwar Reddy M / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 3, Issue 4, Jul-Aug 2013, pp.1627-1631

# Design Of Low Power Bcd Adder Using 14-T Full Adder

**Muniraja Thoti[1], Jagadeeshwar Reddy M[2]**
[1]M.TECH in DSCE BIT-INSTITUE OF TECHNOLOGY HINDUPUR, India
[2]M.TECH in VLSI DESIGN &EMBEDDED SYSTEM, ASSISTANT PROFESSOR BIT-INSTITUTE OF TECHNOLOGY HINDUPUR, India

***Abstract***

**Nowadays, Decimal arithmetic is increasing in recent years, hence growth in decimal data processing systems like in all commercial, financial and internet based applications. Power reduction is one among the parameter plays a vital role in VLSI industry. Hence, In this paper, a BCD adder is reconfigured in order to reduce the power. This work concentrates on14-T(Transistors) full adder circuits is used in BCD adder .This work evaluates the performances of power and delay of BCD adder compared with conventional BCD adder using 50nm technology.**

**KEYWORDS:** Low power, BCD adder, 14-T full adder, decimal arithmetic.

## I. INTRODUCTION

VLSI designers have used speed as the performance metric. High gains, in terms of performance and silicon area, have been made for digital processors, microprocessors, DSPs (Digital Signal Processors), ASICs (Application Specific ICs), etc. In general, small area and high performance are two conflicting constraints. The power consumed for any given function in CMOS circuit must be reduced for either of the two different reasons: One of these reasons is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power dissipation is worthwhile as long as it doesn't degrade overall circuit performance. The other reason is to save energy in battery operated instruments same as electronic watches where average power is in microwatts. In CMOS circuits, the power consumption is proportional to switching activity, capacitive loading and the square of the supply voltage. Circuit complexity has always been the on the top of various design factors being considered in that it relates directly to the silicon die size and indirectly to the power consumption. The emphasis on power or energy consumption, however, has drawn even bigger attention these years with the prevailing of battery operated mobile device. Speed performance remains as the ultimate concern for those applications with critical computing demands. In practice, it is unlikely to accomplish a design excels in all these design aspects. Most of the time, a design tradeoff must be made to balance the performance in terms of power, delay and so on. As a result, many compound performance indexes such as power delay product, area delay product or energy consumption per specific task were revised for performance evaluation. Subject to the design specifications, circuits are optimized in terms of these compound performance indexes. As the process technology evolves into the era of deep submicron, emerging design concerns such as leakage power consumptions and low *Vdd* operations surface and bring up new paradigms for conventional circuit designs. It is therefore worth of re-examining the designs of these basic digital processing units and developing new circuit level designs subject to various performance indexes.

For full adder design, static-CMOS is the most conventional one. It can support low voltage, low power-delay-product (PDP) operation but requires as many as 28 transistors. Dynamic circuits can reduce the transistor count but the incurred power consumption, including that of the clock tree, is usually high. Complementary pass transistor logic (CPL) based design is another high performance design alternative but not a power efficient one, either. Various low transistor count designs have been developed in the hope of low power operation as well. In transmission gate plus inverter based full adder designs were presented using 20 - 16 transistors, respectively. In pass transistor logic based XOR/XNOR circuits were used and the full adder designs consist of only 14/16 transistors. In a pass transistor based new Static Energy-Recovery Full *(SERF*) adder with only 10 transistors was presented. Low transistor count designs, however, often lead to degraded output signals and deteriorates the speed performance dramatically. The phenomenon is even prominent in n-bit cascaded operations due to Elmore effect. Therefore, how to achieve speed performance and power efficiency while maintaining the low circuit complexity are still challenging design issues for full adder designs.

Binary coded decimal (BCD) is encoding method for the decimal numbers in which each digit can be represented in its own binary format. Decimal fractions are pervasive in human endeavors, yet most cannot be represented by binary fractions.

### *A. **verview of BCD adder***

BCD is a decimal representation of a number directly coded in binary, digit by digit. For example the number 9527, which is equal to (1001 0101 0010 0111)BCD. It can be seen that each digit of the decimal number is coded in binary and then concatenated, to form the BCD representation of the decimal number.

To use this representation all the arithmetic and logical operations need to be defined. As the decimal number system contains 10 digits at least 4 bits are needed to represent a BCD digit.

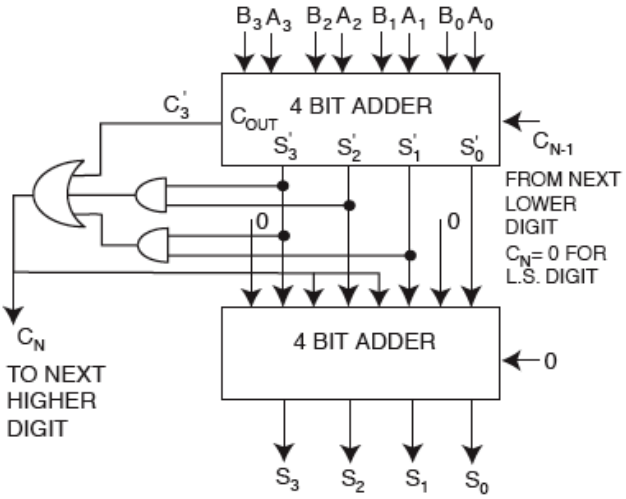


Fig 1. Overview of 4- bit BCD adder

To implement a 4-bit BCD adder we need two 4-bit full adders, one to add two 4-bit BCD numbers and the other full adder 2's complement of the results greater than 9 to the result if carry is generated. Also we need 2 AND gates and one OR gate to generate carry signal.

### *B. Conventional power gated BCD adder design*

In the power gating, sleep transistors are used as switches to shut off power to parts of a design in standby mode. The header switch is implemented by PMOS to control Vdd supply. PMOS transistor is less leaky than NMOS transistor of the same size. The disadvantage of the header switch is that PMOS has lower drive current than NMOS of a same size. As a result, a header switch implementation usually consumes more area than a footer switch implementation. The footer switch is implemented by NMOS transistor to control VSS supply. The advantage of footer switch is the high drive and hence smaller area. However, NMOS is leakier than PMOS and sleep transistor become more sensitive to ground noise. Among the leakage reduction techniques, the power gating technique has become one of the most effective methods. With the circuit density being increased at nanoscale, the scheduling of the sleep transistors plays a vital role in reducing the leakage power of the circuit. Sleep transistor is shown in the fig 2

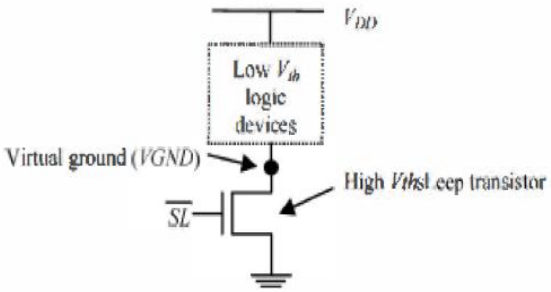


Fig 2. A power gating structure

In clock gated power gating structure, an internal clock signal is used to excite the sleep transistors in the BCD circuit. The clock frequency is partially dependent on the average delay which occurs within the circuit. The clock speed is predetermined based on the propagation speed of intermediate results between logic clusters in the circuit. Low Vth devices are replaced with BCD adder circuit. Due to applying the clock signal to the circuit consumes extra power. If the number of stages increases the power consumption and area will get increased.

Instead, we are going to use less transistor count full adder circuits. Generally 28 transistors are used while designing the full adder circuit in order to generate sum and carry for one bit addition. The following section explains different low complexity and low power transistor based full adder circuit designs.

## II. FULL ADDER DESIGNS

The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The driving capability of a full adder is very important, because, full adders are mostly used in cascade configuration, where the output of one provides the input for other. If the full adders lack driving capability then it requires additional buffer, which consequently increases the power dissipation. In the last decade, the full adder has gone through substantial improvement in power consumption, speed and size, but at the cost of weak driving capability and reduced voltage swing. However, reduced voltage swing has the advantage of lower power consumption.

### *C. Design of 8T Full Adder*

The basic of 8T full adder consists of 3 modules, 2 XOR elements and a Carry section as shown in figure below. The Sum output is obtained by two XOR blocks in succession. For the carry section we use GDI based 2T-MUX and (A XOR B)as the selection signal. The Sum and the Cout module need 6 and 2 transistors respectively. The transistor level implementation of the eight transistor full adder is shown in Fig. 3. It is obvious from the figure that both Sum and Cout has a maximum delay of 2T.

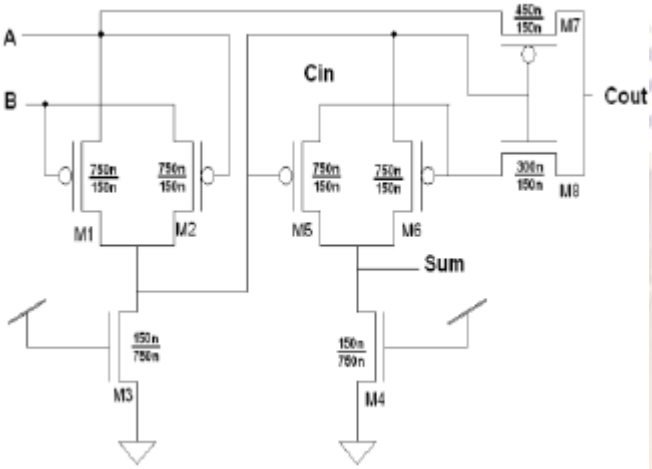


Fig 3. 8T full adder circuit

But while simulating the above 8T full adder circuit, the output results are clamped at the voltage, i.e., the voltage swing is more at its output.. Higher power consumption due to short circuit current. It is clearly shown in the below simulation results. Fig 4 gives iput waveform for all following full adder designs.

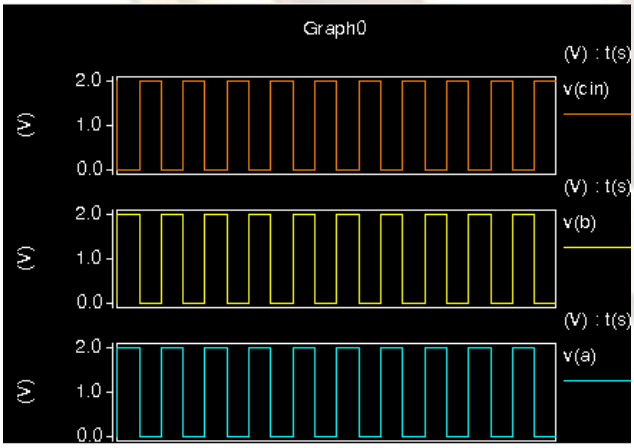


Fig 4. Input waveforms for the full adder designs.

The output waveform for 8T based full adder is shown below,

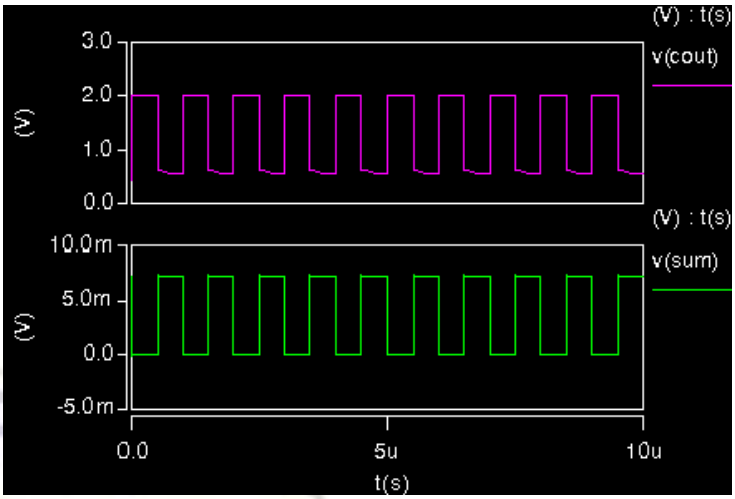


Fig 5. 8T full adder output waveform

From the above output waveform its clearly noted that sum output is exactly very less voltage swing. But at the carry output i.e cout has high voltage swing at its output nearly 0.4v has been clamped.

Hence this adder cannot be used in the BCD adder because its driving capability is very poor.Next we are design the 10 T(Transistor) based full adder design.

### *D. Design of 10T Full Adder*

The design, denoted as SERF (static energy recovery full adder), emphasizes the low power consumption. As shown in Fig. 6, it uses two 4-transistor XNOR circuits. The design is claimed to be extremely low power because it doesn't contain direct path to the ground and it can re-apply the load charge to the control gate (energy recovery).

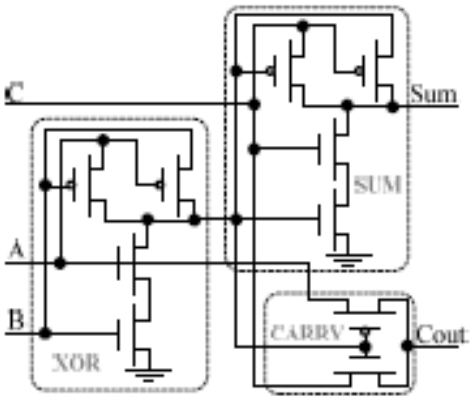


Fig 6. 10T full adder circuit

The circuit produces full-swing at the output nodes. But it fails to provide so for the internal nodes. As the power consumption by the circuit reduces the circuit becomes slower. Also it cannot be cascaded at low power supply due to multiple threshold

problems. It is noted from the below simulation results for the same above input waveform.

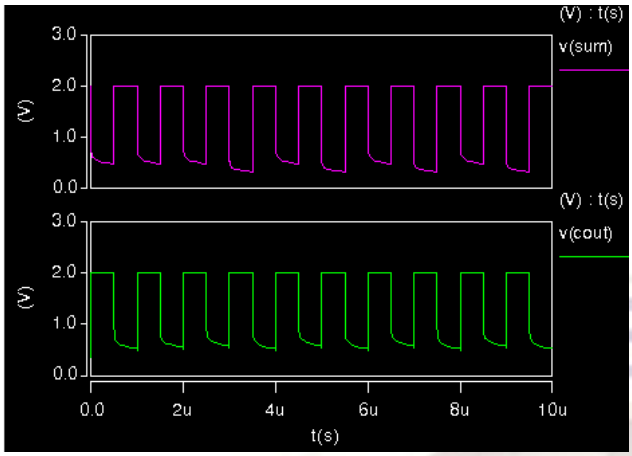


Fig 7. 10T full adder output waveform.

Here bothe sum and cout values has voltage swing at its output and it also less driving capability . Hence, we cannot use this 10 T full adder circuit in BCD adder application.Therefore we are going to design the full adder by using 14 Transistors.

### *E. Design of 14T Full Adder*

This circuit has 4 transistor XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously to generate sum and cout. The signals cin and □□□□ are multiplexed which can controlled either by (a b) or (a ⊗ b). Similarly the cout can be calculated by multiplexing a and cin controlled by (a b).It is the fastest adder among above adders. The circuit is shown in the fig 8

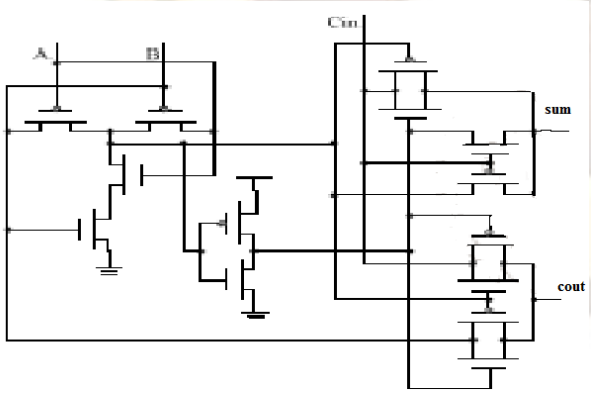


Fig 8. 14 T full adder circuit

The 14T adder with 14 transistors consumes considerably less power in the order of microwatts and has higher speed. The simulated results are shown below in the figure 9 with respect to input waveform fig 4. Here the exact results have came without any voltage swing.

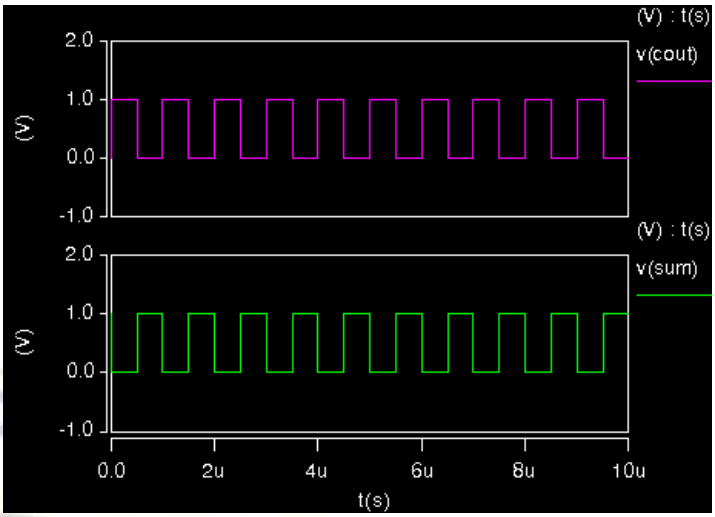


Fig 8. 14 T Full adder output waveform.

Hence this adder circuit is perfectly suitable to implement the 4 –bit BCD adder .

## III. PROPOSED 4-BIT BCD ADDER

Now we are going to use 14 T based full adder circuit in BCD adder circuit and to build the block diagram of proposed BCD adder with low power consumption which is shown in the fig 9 below

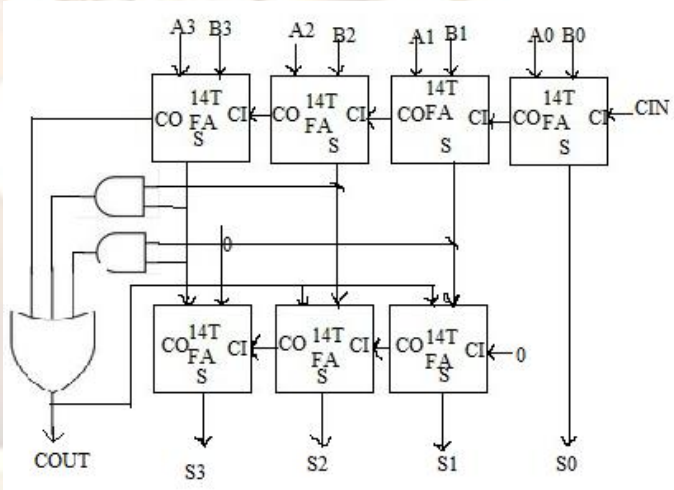


Fig 9 Proposed 4-bit BCD adder block diagram

## IV. SIMULATION RESULTS

Thus, the above mentioned 4 bit proposed BCD adder circuit are designed in 50 nanometer technology and simulated by using HSPICE tool and the results are shown below. The inputs are set as A input set as 1001 and B input set as 1001 and cin i.e. carry input set as 0,the corresponding output SUM should be 1000 and carry out COUT should be 1.

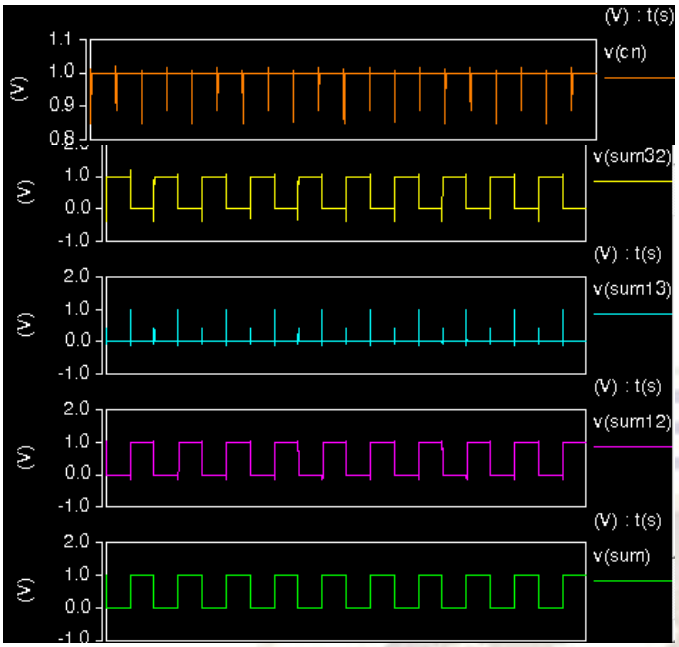

Fig 10. Output waveform for 4 bit BCD adder

The results are verified with respect to output waveform of 4 –bit BCD adder , which is exactly mathced with the expected output.

## V. PERFORMANCE ANALYSIS

### F. *Power analysis*

The performance analysis of this work mainly concentrates on power and delay. The power consumed by this 4 –bit BCD adder is only 0.03µW,which is greatly reduced with respect to conventional one and also clock power gated BCD adder it is clearly given in the bar graph.

The bar graph mentioned below is the average power consumed and compared between the conventional BCD adder, clock power gated BCD adder and proposed 4- bit BCD adder.

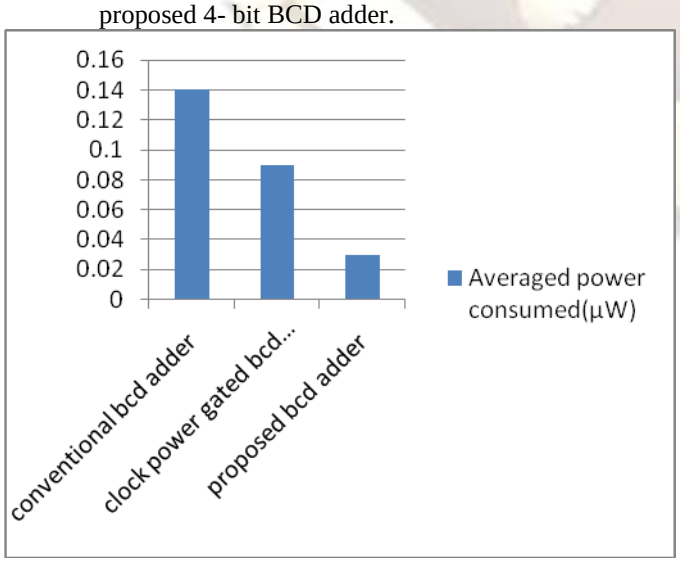

Fig 11.Average power consumption

### G. *Delay analysis*

The delay analysis is performed to calculate the delay arising across the circuits designed above. Delay has been reduced upto 8ps.The table 1 describes the power delay and power delay product is compared with other two BCD adder circuits.

| S.no | Circuit | Delay(in ps) | Power delay product(in µj) |
|---|---|---|---|
| 1 | Conventional BCD adder | 82.5 | 11.8 |
| 2 | Clock power gated BCD adder | 72.36 | 6.138 |
| 3 | Proposed BCD adder | 8 | 0.24 |

TABLE 1: Delay comparison between the adders.

From the above tabular column of delay analysis clearly shown that our proposed BCD adder has less delay than other adder circuits.

## VI. CONCLUSION

The main scenario of this work is to reduce power consumption in BCD adder using 50nm scale cmos technology and simulated by HSPICE tool. Clock gating method in power gating design, which provides additional control over the excitation process of sleep transistor. Thus we achieved by means 14-Transistors full adder is used without any usage of power gating techniques. There is a vast difference between this too. It is finally found that performance has greatly improved i.e. power and delay reduction.

## REFERENCES

[1] Jin-Fa Lin, Yin-Tsung Hwang, Ming-Hwa Sheu and Cheng-Che Ho " A novel high speed and energy efficient 10-transistor full adder design," *IEEE Transactions on Circuits and Systems I*, vol54, pp.1050-1059, May. 2007. SCI,EI

[2] Jin-Fa Lin , Yin-Tsung Hwang and Ming-Hwa Sheu "Low-power and low-complexity full adder design for wireless base band applications" , *IEEE International Symposium on Circuit and System*, pp. 2337-2341, Jun. 2006.

[3] P. M. Lee, C. H. Hsu, and Y. H. Hung, "Novel 10-T full adders realized by GDI structure" IEEE International Symposium on Integrated Circuits (ISIC-2007).

[4] M.Moaiyeri, R. Faghih Mirzaee, K.Navi, "Two New Low Power and High Performance Full Adders", Journal of Computers, Vol. 4, No. 2, February 2009.

[5] Rabaey J.M., A. Chandrakasan, B.Nikolic, "Digital Integrated Circuits, A Design" 2nd 2002, prentice Hall, Englewood Cliffs,NJ.