Power Aware BIST for Digital IC's

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ABSTRACT

Testing of digital VLSI circuits encounters many challenges as a result of rapidly growing semiconductor manufacturing technologies along with unexampled levels of design complexity and the gigahertz range of operating frequencies. These challenges include keeping the average and peak power dissipation and test application time within acceptable limits. This paper proposes a new output sequence of an LFSR to design a low-power test-pattern-generator for built-in self-test (BIST) to achieve reduction in the overall switching activity in the circuit-under-test (CUT). Conventional and low power test patterns are applied on an industry standard ISCAS-85 c432 27-channel interrupt controller circuit and total power consumption is measured. The obtained results show up to 18% power reduction for the proposed design. Fault simulation tool is used to estimate the number of test vectors required for high fault coverage of the interrupt controller. It generates 261 test vectors for the conventional TPG and 678 test vectors for the low power TPG, thus indicating 160% increase in test vectors. The results obtained show a significant increase in test application time for low power TPG.

Keywords **-** CUT, LP-TPG, Fault Coverage, Test Cycles, Test Vectors.

I. Introduction

In recent years, circuit size has increased due to scaling down of technology. Controlling power dissipation in these large circuits during test sessions is one of the major concerns in VLSI testing. In general power dissipation of a system in test mode is higher than the normal mode. The power consumption of the chip during manufacturing test can be significantly higher than the power consumption of the chip in its target system. This increase in the power consumption can be attributed primarily to on-chip extremely random test pattern generation. This extra power can cause problems such as instantaneous power surge that causes circuit damage, formation of hot spots, difficulty in performance verification and reduction of system lifetime and product yield [8].

The reason behind the high power dissipation during test is because unlike normal mode operation of the system correlation between consecutive test patterns does not exist in test mode. This is particularly true in case of Built-In-Self-Test (BIST), a popular DFT methodology. To increase the correlation between consecutive vectors during testing, several techniques have been proposed for creating low transition density in the pattern sets and thus control the power dissipation. However, this in turn increases the test application time as the test has to run for longer test sessions to reach sufficient fault coverage. Increase in test time is undesirable as testing cost of a chip is directly related to the time it takes to test the chip.

This paper presents a new low power pattern generation technique. Conventional and low power test patterns are applied on an industry standard ISCAS-85 c432 27-channel interrupt controller circuit and power consumption is measured along with analysis of number of test patterns and test time required to achieve targeted fault coverage.

II. Built in self test (BIST)

As the complexity of modern chips increases, external testing with Automatic Test Equipment (ATE) becomes extremely expensive. Instead, built-in self-test (BIST) is becoming more common in the testing of digital VLSI circuits since it overcomes the problems of external testing using ATE. BIST test patterns are generated internally using some some parts of the circuit, also the responses are analyzed using other parts of the circuit. When the circuit is in test mode, test patterns generators (TPG's) generate patterns that are applied to the CUT, while the signature analyzer (SA) evaluates the CUT responses. One of the most common TPG is the (linear feedback shift register) LFSR [6]. LFSR's are used as TPG's for BIST circuits because, with little overhead in hardware area, a normal register can be configured to work as a test generator, and with an appropriate choice of the location of the XOR gates, the LFSR can generate all possible output test vectors (with the exception of the 0s-vector, since this will lock the LFSR). The pseudorandom properties of LFSR's lead to high fault coverage when a set of test vectors is applied to the CUT compared with the fault coverage obtained using normal counters as TPG's. Logic built-in self-test (LBIST) is well known as one of the technologies to reduce test data volume. In general, LBIST uses pseudorandom pattern generator (PRPG) with high switching activity. Therefore LBIST makes high power consumption during scan shift operation. As

the results, it increases test time (costs) because test engineer has to slow down shift speed to solve power issue [4].

III. Automatic Test Pattern Generation (ATPG)

The automatic test pattern generator (ATPG) is software dedicated to the generation of test vectors that are used to detect the modeled faults in a CUT. Since in many cases the generated vectors do not achieve 100% fault coverage, the ATPG gives statistics about the FC achieved, the percentage of redundant faults, and the aborted faults which will therefore not be detected) for these test vectors.

ATPG tools can be divided into two types: combinational ATPG and sequential ATPG. The combinational ATPG is dedicated to generating test sets for combinational circuits, or scan-based sequential circuits where all of the state elements can be accessed directly through the scan-chain. In this paper the ATPG can generate test vectors that achieve high fault coverage. Most of the combinational ATPG's depends on random and deterministic phases in the generation of test vectors. In the random phase, the ATPG applies pseudo-random vectors to inputs of the CUT and then performs fault simulation to check the fault coverage and the faults remaining undetected. Normally, most of the faults are detected in this phase. In the deterministic phase, the ATPG generates test vectors for specific faults (that are hard to detect by pseudorandom means) and normally uses algorithms such as the path sensitization method for this purpose.

The sequential ATPG, which is dedicated to the generation of test vectors for sequential circuits, is more complicated as a result of the timing signals and memory elements present in the circuit. In general, two test vectors are needed to test a fault (or group of faults). The first test vector is used to initialise the memory elements to a specified state, and then the next is used to detect the presence of the fault(s). One of the aims of design for testability techniques is to reduce the complexity of test generation for sequential circuits. One common technique to achieve this is to change the sequential circuit to a scan-based circuit.

The aim of this paper is to reduce the test power in a combinational benchmark circuit by applying LP-TPG vectors and conventional test vectors to inputs of the CUT.

IV. Low Power Test Pattern Generation

With the development of portable devices and wireless communication systems, design for low power has become an important issue. Minimising power dissipation in VLSI circuits increases the battery lifetime and the reliability of the circuit. In general, the power dissipation of complementary metal oxide semiconductors (CMOS) circuits can be divided into two main categories: static power and dynamic power [1].

Static power is the power dissipated by a gate when it is not switching. A significant fraction of static power is caused by the reduced threshold voltage used in modern CMOS technology that prevents the gate from completely turning off, thus causing source to drain leakage. All the components of static power dissipation have a minor contribution to the total power dissipation, and can be minimised for well-designed circuits.

On the other hand, dynamic power dissipation, which is the dominant source of power dissipation in CMOS circuits, occurs while the circuit is switching. The circuit is active when the applied voltage to an input of a cell changes, resulting in a logic transition in one or more outputs of the circuit at transistor level [3 9]. Hence, charging discharging of the load capacitances of transistors is the main source of dynamic power dissipation.

One way to improve the correlation between the bits of the successive vectors is to avoid frequent transitioning of the logic levels of the primary inputs [7]. The new approach entails inserting 3 intermediate vectors between every two successive vectors. The total number of signal transitions between these 5 vectors is equal to the total number of signal transitions between the 2 successive vectors generated using the conventional approach. This reduction of signal transition activity in the primary inputs reduces the switching activity inside the design under test and therefore results in reduced power consumption by the device under test [3 9]. The technique of inserting 3 intermediate vectors is achieved by modifying the conventional LFSR circuit with two additional levels of logic between the conventional flip-flop outputs and the low power outputs. The first level of hierarchy from the top down includes logic circuit design for propagating either the present or the next state of the flip-flops to the second level of hierarchy. The second level of hierarchy is a multiplexer function that provides for selecting between the two states (present or next) to be propagated to the outputs as low power output. The outputs of the flip-flops are loaded with the seed vector and the feedback taps are selected pertinent to the characteristic polynomial which represents linear feedback shift register. Only two inputs pins, test enable and clock are required to activate the generation of the pattern as well as simulation of the design circuit. It is also noted that the intermediate vectors in addition to aiding in reducing the number of transitions can also assist significantly in detecting faults just as good as the conventional LFSR patterns [7].

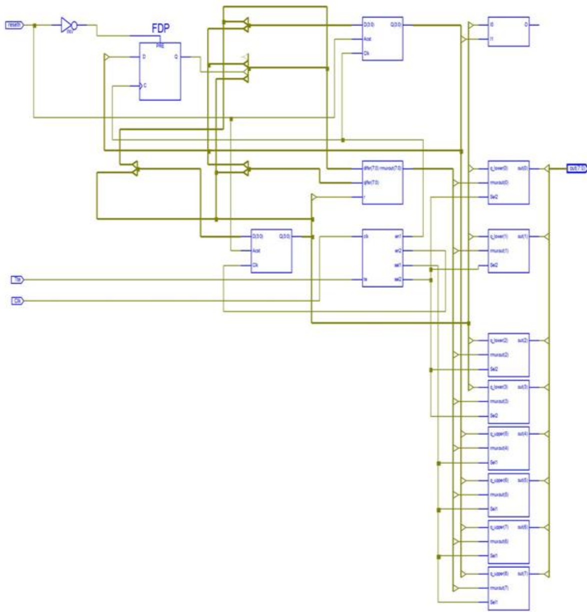

figure 1 schematic for low power test pattern generator

V. Algorithm To Generate Low Power TPG

A low power test pattern generation technique for 9-bit linear feedback shift register with the initial output states (0100 1011) as shown in Fig. 1. The feedback taps are designed for maximal length linear feedback shift register generating all 0's and all 1's as well.

The first step is to generate T1, the first vector by enabling (clocking) the first 4-bits of the LP-TPG and disabling (not clocking) the last 4 bits. This shifts the first 4 bits to the right by one bit. The feedback bits of the LP-TPG are the outputs of the 8th and the 1st flip-flop. The output of the 8th flip-flop is 1 and the output of the 1st flip-flop is 0. The xor of the 8th flip-flop (1) and the 1st flip-flop(0) is input to the first D flip-flop. The new pattern in the first four bits of the LP-TPG is 1010. The middle register is clocked along with the first 4 bits of the LP-TPG. So the input of the middle flip-flop is the output of the 4th flip-flop which in this case is 0. Since prior to the first clock, the input to the middle register was the seed value of the 4th flip-flop at the output of the 4th flip-flop which is 0. Thus after the first clock this value(0) will now appear at the output of the middle flip-flop. In other words the value of the 4th output is stored in this register and is used in the next few steps.

The first 4 shifted bits of the LP-TPG and the last 4 un-shifted bits (i.e. the seed value) are propagated as T1 (1010 1011) to the final outputs.

Next few steps involve generating the 3 intermediate patterns from T1. These patterns are defined as Ta, Tb and Tc.

Ta is generated by maintaining the first four bits of the LP-TPG (disabling the clock) outputs i.e. from T1 as the final first four low power outputs 1010. Note that the clock to the last four bits of the LP-TPG is also disabled. The last four bits however are the outputs from the injector circuits. The injector circuit compares the next value (at the input of the D-flip-flop) with the current value (at the output of the D-flip-flop). According to T1, the outputs (current values) of the last 4 bits of the LP-TPG are 1011. The next values are the values at the inputs of the D-flip-flops which in this case are 0101. Compare the current values (1011) bit by bit with the next values (0101). If the values bit by bit are not the same then use the random generator feedback R (1) as the bit value. If however both values bit by bit are the same then propagate that bit value to output as opposed to the R bit. This bit by bit comparison gives us the last four bits of Ta to be 1111. Therefore Ta = 1010 1111.

Next step is to generate Tb. Shift the last 4 flip-flops to the right one bit but maintain the first 4 flip-flops. The clock to the first 4 bits and the middle flip-flop is disabled. The clock to the last 4 bits is enabled. Propagate the outputs of the flip-flops of the entire LP-TPG as opposed to the outputs of the injection circuit to the outputs (low power). The injection circuits are disabled. As in Ta, maintain the first four LP-TPG outputs (1010) as the low power outputs. Again from Ta, the inputs of the last four D flip-flops from the previous step (generating Ta) are 0101. Also note that the output of the middle register is 0 from the previous step, therefore the input of the 5th flip-flop is a 0. The outputs of the last 4 flip-flops are 0101 resulting in Tb = 1010 0101.

The 3rd intermediate vector Tc is generated by disabling the clock to the entire LP-TPG. Propagate the first 4 outputs from the injection circuit as the first 4 low power outputs and maintain the last 4 low power outputs the same as Tb. Generating injection circuit outputs for Tc is conceptually the same as in generating Ta. Current values (at the outputs of the flip-flops) of the first four flip-flops are compared with the next values (at the inputs of the flip-flops) of the flip-flops.

The feedback from the 8th flip-flop is 1 (from Tb). Therefore the logical feed forward value of R is 1. The feedback value from the first flip-flop is also 1 as per the current values above. The exclusive-or of two 1's is a 0, so the input to the 1st flip-flop is a 0 which is also the next state of the 1st flip-flop. Hence the next values are 0 for the 1st flip-flop and 101 for the 2nd, 3rd and 4th flip-flop respectively. The next values are 0101. The first four outputs from the injection circuit are 1111. The last four outputs are the same as Tb which are 0101 resulting in the 3rd and final intermediate vector Tc = 1111 0101.

Generating T2 is quite similar to generating T1. As in Tc the outputs of the last four LP-TPG flip-

flops are 0101, the outputs of the first 4 flip-flops of the LP-TPG are the current values which are 1010. Therefore the seed vector for generating T2 is 1010 0101.Shift the first four bits of the LP-TPG and the middle flip-flop, disable the last four flip-flops and propagate the outputs of the entire LP-TPG to the final low power outputs. The output of the 8th flip-flop from Tc is 1 and the output of the 1st flip-flop from Tc is also 1, the exclusive or of them is 0. This results in the input to the 1st flip-flop as a 0, the inputs to the 2nd, 3rd , 4th and the middle flip-flops as 1010. These are also the current values from the previous step (Tc). Shifting the first four flip-flops of the LP-TPG to the right by one bit results in 0101 as the outputs of the first four flip-flops. Therefore T2 generated is 0101 0101.

VI. Benchmark Circuit

ISCAS -85 c432 is a 27-channel interrupt controller. It has 3 interrupt request buses A, B and C, each having 9 bits or channels, and one channel-enable bus E as shown in Fig. 2. Priority: A[i] > B[j] > C[k], for any i, j, k .Within each bus, a channel with a higher index has priority over one with a lower index For ex: if E[i] = 0, then the A[i], B[i], and C[i] inputs are disregarded. The seven outputs PA, PB, PC and Chan[3:0] specify which channels have acknowledged interrupt requests. Only the channel of highest priority in the requesting bus of highest priority is acknowledged.

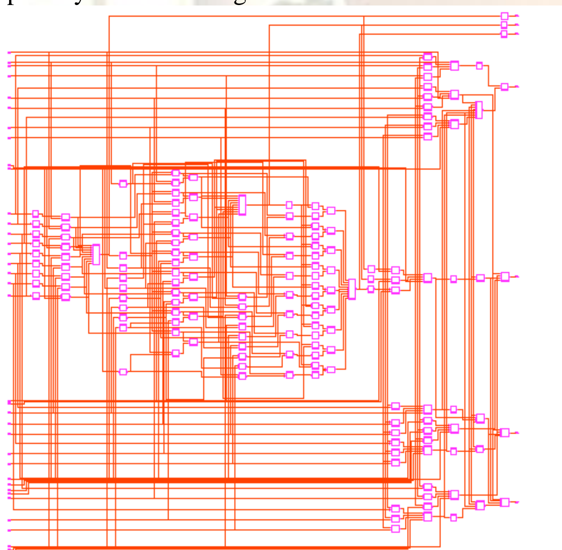

figure 2 c432 benchmark circuit

As shown in Fig. 3, two test pattern generators: conventional TPG and LP-TPG are applied to inputs of c432 (CUT) to estimate power consumption, area, total number of faults in CUT, fault coverage, number of test vectors and number of test cycles required to achieve maximum fault coverage. The results are shown in Table1.

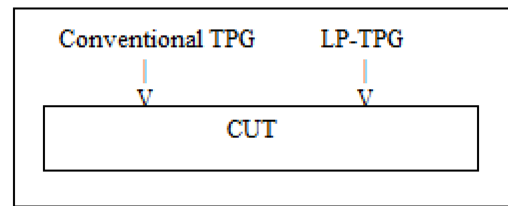

figure 3 block diagram

The LP-TPG when given as inputs to the CUT i.e c432 combinational circuit, improves the correlation between the signals of the successive vectors resulting in reduced transitions of the primary inputs hence reducing switching activity inside the circuit under test [3 9]. The methodology used in estimating the power consumption of the device under test includes the generation of the 36-bit low power pattern, synthesizing the c432 circuit using generic libraries, running the 36-bit pattern on the c432 circuit and computing the power consumption using a power estimation tool. The schematics for 36-bit inputs to CUT is shown in Fig. 4 for both cases, left is conventional TPG and right is LP-TPG. Fault simulation tool is used to estimate the number of test vectors required for high fault coverage of the interrupt controller. The tool generated 261 test vectors for the conventional TPG and 678 test vectors for the low power TPG, thus indicating 160% increase in test vectors. The results also shows a considerable increase in test application time for low power TPG

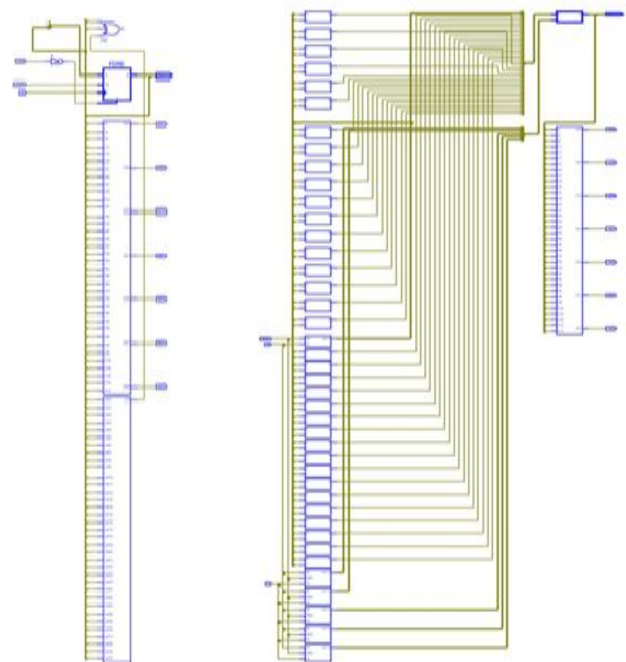

figure 4 schematics for conv TPG (left) and LP-TPG (right)

VII. Fault Modeling and Fault Coverage

A fault model can be defined as a description of the behaviour of, and assumptions about, how components (nodes, gates…etc.) in a faulty circuit behave. In this way, a high percentage of the faults that may occur in a circuit can be modeled. One of the most popular and common fault models at the logic level of abstraction is the stuck-at-fault model. It makes the assumption that a node under consideration is permanently connected to ground , called stuck-at-0 (s-a-0), or permanently connected to Vdd, called stuck-at-1 (s-a-1). This fault model is considered to be most common model in logic circuits and is used throughout this research.

A commonly used metric to represent the percentage of faults detected using a fault model is the fault coverage (FC). The FC can be represented as in equation (1).

$$FC = \frac{DF}{TF} \quad (1)$$

Where DF represents the number of detected faults, TF represents the total number of faults in the CUT.

Fault simulation tool provides the following measures of circuit under test:
Test coverage = detected faults / detectable faults
Fault coverage = detected faults / all faults
ATPG effectiveness = ATPG-resolvable faults/ all faults

Table 1
Test Generation by Fault Simulation

Circuit Name	Conventional TPG with c432	LP-TPG with c432
Total Faults	**2084**	**5106**
Total Power Consumption	102 mW	87 mW
Total Area of DUT	3053	9554
Fault Coverage	99.28 %	93.42 %
Test Coverage	99.71 %	95.76 %
ATPG Effectiveness	99.06 %	99.71 %
Number of Test Vectors	261	678
Number of Test Cycles	9957	80123

Test coverage is defined as the percentage of detected faults out of detectable faults, Fault coverage is defined as the percentage of detected faults out of all faults and ATPG effectiveness is defined as the percentage of ATPG-resolvable faults out of the total faults. The results obtained for both conventional and low power test pattern generator as inputs to c432 benchmark circuit are shown in Table 1.

In this paper, the maximum fault coverage obtained by conventional LFSR is 99.28% for 1195 total number of faults whereas for low power TPG the fault coverage obtained is 93.42% for 3259 total number of faults in CUT

In order to determine the fault coverage for a specified set of test vectors applied to a CUT, fault simulation is carried out. Simulation result in Fig. 5 shows test vectors represented by registers out [35:0], clock, reset, enable and 7 outputs of CUT.

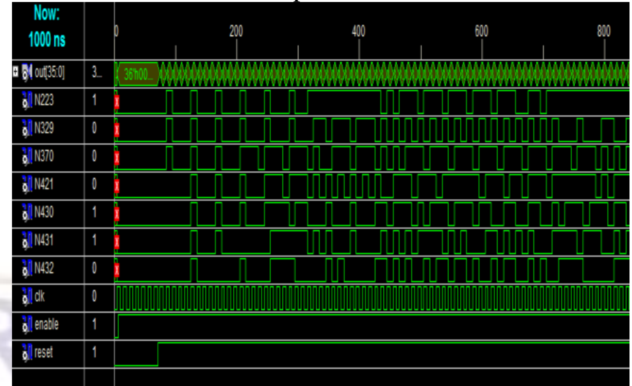

figure 5: simulation result for lp-tpg with cut

For each fault expected in the CUT (excluding redundant faults), the output produced when a test vector is applied to a faulty circuit differs from the output produced in a fault-free circuit. Thus, fault simulation produces a list of detected faults for each test vector [2]. As indicated by Fig. 6, in case of low power TPG, there is a significant increase by 160% in number of test vectors required to achieve high fault coverage as compared to conventional test vectors.

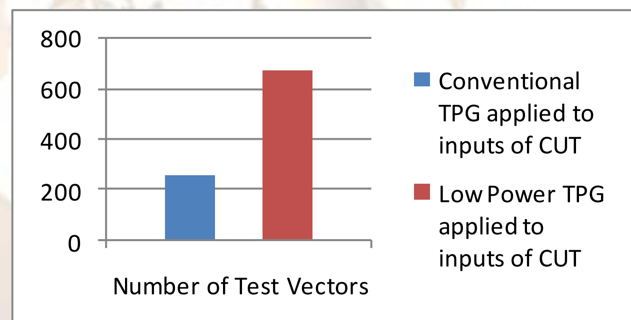

figure 6 number of test vectors

The automatic test pattern generator (ATPG) is software dedicated to the generation of test vectors that are used to detect the modelled faults in a CUT. Since in many cases the generated vectors do not achieve 100% fault coverage, the ATPG gives statistics about the FC achieved, the percentage of redundant faults, and the aborted faults (which will therefore not be detected) for these test vectors.

Testing for high fault coverage has a direct and important relationship with low power testing; the conventional approach to testing, in order to increase the reliability of the system, the test should run till a high fault coverage is achieved. This normally needs very long sequence of test vectors for most circuits. Hence, a long time is needed. Since the total power consumed in the CUT during test is a function of time, conventional approach to testing, without improvement techniques, consumes high

energy, which in turn decreases the battery lifetime [1]. The main reason why the conventional way of testing requires a long test length is that the fault coverage is limited by the presence of random-pattern resistant faults when a pseudorandom TPG is used. The results as indicated by the test cycles in Fig. 7 shows a significant increase in test application time for low power TPG applied as inputs to CUT as compared to conventional TPG.

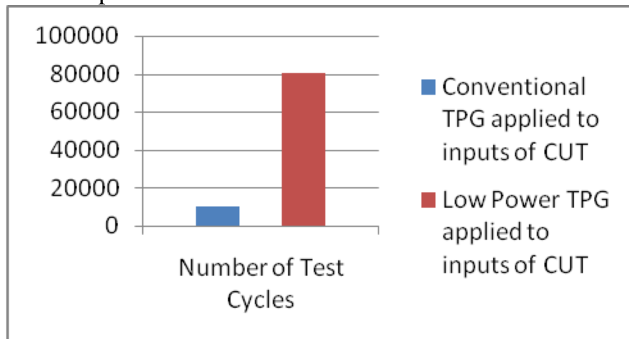

figure 7 number of test cycles

VIII. Conclusion

The LP-TPG improves the correlation between the signals of the successive vectors resulting in reduced transitions of the primary inputs hence reducing switching activity inside the circuit under test [3 9]. The methodology used in estimating the power consumption of the device under test includes the generation of the 36-bit low power pattern, synthesizing the c432 circuit using generic libraries, running the 36-bit pattern on the c432 circuit and computing the power consumption using a power estimation tool. Fault simulation tool is used to estimate the number of test vectors required for high fault coverage of the interrupt controller. In this paper, the maximum fault coverage obtained by conventional LFSR is 99.28% for 1195 total number of faults whereas for low power TPG the fault coverage obtained is 93.42% for 3259 total number of faults in CUT. The tool generated 261 test vectors for the conventional TPG and 678 test vectors for the low power TPG, thus indicating 160% increase in test vectors. The results as indicated by the test cycles in Table 1 shows a considerable increase in test application time for low power TPG applied to CUT.

REFERENCES

[1] Ajit Pal, Santanu Chattopadhyay, Synthesis and Testing for Low Power, Tutorial T7-A, 2009 22nd *International Conference on VLSI Design*

[2] Seongmoon Wang, Srimat T. Chakradhar, A Scalable Scan-Path Test Point Insertion Technique to Enhance Delay Fault Coverage for Standard Scan Designs, *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 8, August 2006

[3] Dr.K.Gunavathi, Mr. K.Paramasivam, Ms.P.Subashini Lavanya, M.Umamageswaran,, A Novel BIST TPG for Testing of VLSI Circuits, *First International Conference on Industrial and Information Systems, ICIIS* 2006, 8 - 11 August 2006, Sri Lanka

[4] Jun Matsushima, Yoichi Maeda, Masahiro Takakura, CooLBIST An Effective Approach of Test Power Reduction for LBIST, *17th Asian Test Symposium.*

[5] Siddharth Seth, Gaurav Sahni, Weighted Pseudo-Random Test Pattern Generation, Indian Institute of Technology Kharagpur

[6] Lung-Jen Lee1, Wang-Dauh Tseng, Rung-Bin Lin, Chi-Wei Yu, Deterministic Built-in Self-Test Using Multiple Linear Feedback Shift Registers for Low-Power Scan Testing, *2009 Asian Test Symposium*.

[7] Seongmoon Wang, Sandeep K. Gupta,, An Automatic Test Pattern Generator for Minimizing Switching Activity During Scan Testing Activity, *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 21, No. 8, August 2002.

[8] Patrick Girard, Low Power Testing of VLSI Circuits: Problems and Solutions

[9] Yi Wang, "Research and Design of Low Power Consumption Testing Generator for Integrated Circuits", *Third International Conference on Information and Computing, 2010.*