Efficiency of Adiabatic Logic for Low-Power VLSI Using Cascaded ECRL And PFAL Inverter

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Abstract
The energy stored at the output can be retrieved by the reversing the current source direction discharging process instead of dissipation in NMOS network. Hence adiabatic switching offers the less energy dissipation in PMOS network and reuse the stored energy in the output capacitance by reversing the current source direction. There are the many adiabatic logic design technique are given in Literature but here two of them are chosen ECRL and PFAL, which shows the good improvement in energy dissipation and are mostly used as reference in new logic families for less energy dissipation reduction of area & power factors the simulations were done using micro wind & DSCH results.

Index Terms— Adiabatic switching, energy dissipation, power clock, equivalent model.

I.   INTRODUCTION

The main objective of this thesis is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth With the scaling down of the technologies. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level. Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. Then, to limit the power dissipation, Alternative solutions at each level of abstraction are proposed. The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this thesis work, a new CMOS logic family called ADIABATIC LOGIC, based on the adiabatic switching principle is presented.

The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation.

The Adiabatic switching technique can achieve very low power Dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.
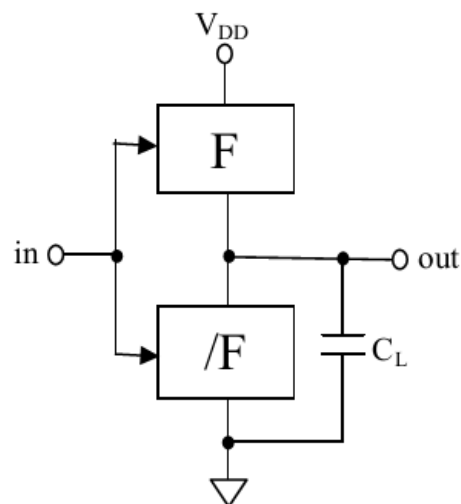

Fig1: Conventional CMOS logic circuit with pull-up (F) and pull-down (/F) networks.

This thesis work demonstrates the low power dissipation of Adiabatic Logic by presenting the results of designing various design/ cell units employing Adiabatic Logic circuit techniques. A family of full-custom conventional CMOS Logic and an Adiabatic Logic units for example, an inverter, a two-neither input NAND gate, a two-input NOR gate, a two-input XOR gate, a two-to-one multiplexer and a one-bit Full Adder were designed in Mentor Graphics IC Design Architect using standard TSMC 0.35 µm technology, laid out in Microwind IC Station.

All the circuit simulations has been done using various schematics of the structures and post-layout simulations are also being done after they all have been laid-out by considering all the basic design rules and by running the LVS program. Finally, the analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done to show the amount of power dissipated by the two logic families.

Adiabatic logic circuits reduce the energy dissipation during switching process, and reuse the some of energy by recycling from the load capacitance. For recycling, the adiabatic circuits use the constant

current source power supply and for reduce dissipation it uses the trapezoidal or sinusoidal power supply voltage.

II.   DISSIPATION MECHANISMS IN ADIABATIC LOGIC CIRCUITS

Fig.2 shows, the equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Here R is on resistance of the PMOS network, CLis the load capacitance.
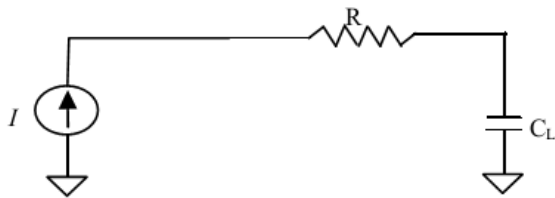
Energy dissipation in resistance R is

Fig.2 Equivalent model during charging process in adiabatic circuits.

$$E_{diss} = I^2.R.T = \left(\frac{C_L V_{DD}}{T}\right)^2 .R.T = \left(\frac{RC_L}{T}\right).C_L V_{DD}^2$$

Since Ediss depends upon R, so by reducing the on resistance of PMOS network the energy dissipation can be minimized. The on resistance of the MOSFET is given by the first order approximation is [3-5],

$$R = \left[\mu C_{OX} \frac{W}{L}(V_{GS} - V_{th})\right]^{-1}$$

Where µ is the mobility, Cox is the specific oxide capacitance, Vgs is the gate source voltage, W is the withal is the length and Vth is the threshold voltage. Ediss also depends upon the charging time T, If T>> 2RC then energy dissipation will be smaller than the conventional CMOS. The energy stored at output can be retrieved by the reversing the current source direction during discharging process instead of dissipation in NMOS network. Hence adiabatic switching technique offers the less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source direction [1, 2].

III.   ADIABATIC LOGIC GATE

In the following, we will examine simple circuit configurations which can be used for adiabatic switching. Figure 3.2 shows a general circuit topology for the conventional CMOS gates and adiabatic counterparts. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up and the pull-down networks must be replaced with complementary transmission-gate (T-gate) networks. The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network

implementing the pull-down function drives the complementary output node. Note that all the inputs should also be available   in complementary form. Both the networks in the adiabatic logic circuit are used to charge-up as well as charge-down the output capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a pulsed-power supply with the ramped voltage output.
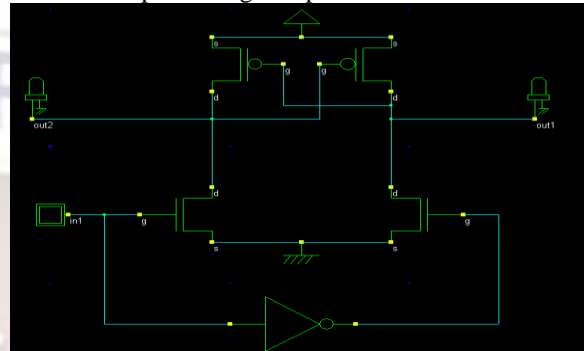

Fig3: :Adiabatic Logic Gate

IV.   ADIABATIC LOGIC TYPES

Practical adiabatic families can be classified as either PARTIALLY ADIABATIC or FULLY ADIABATIC. In a PARTIALLY ADIABATIC CIRCUIT, some charge is allowed to be transferred to the ground, while in a FULLY ADIABATIC CIRCUIT, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization.

A) ECERL-Efficient Charge Recovery Logic:

Efficient Charge – Recovery Logic (ECRL) proposed by Moon and Jeong [13], shown in Figure, uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling. It consists of two cross-coupled transistors M1 and M2 and two NMOS transistors in the An AC power supply pwr is used for ECRL gates, so as to recover and reuse the supplied energy. Both out and /out are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. A more detailed description of ECRL can be found in . Full output swing is obtained because of the cross-coupled PMOS transistors in both precharge and recovers phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches.
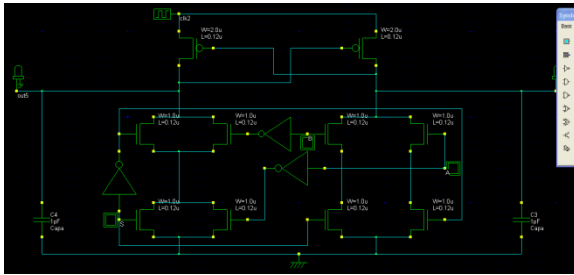
Fig4: ECRL circuit diagram

B) Positive Feedback Adiabatic Logic:

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 5. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS M1-M2 and two NMOS M3-M4, that avoids a logic level degradation on the output nodes out and /out. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETS, rather than by only two PMOSFETs as in ECRL logic, and that the functional blocks are in parallel with the transmission PMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The energy dissipation by the CMOS Logic family and Adiabatic PFAL Logic family can be seen as in Figure 5
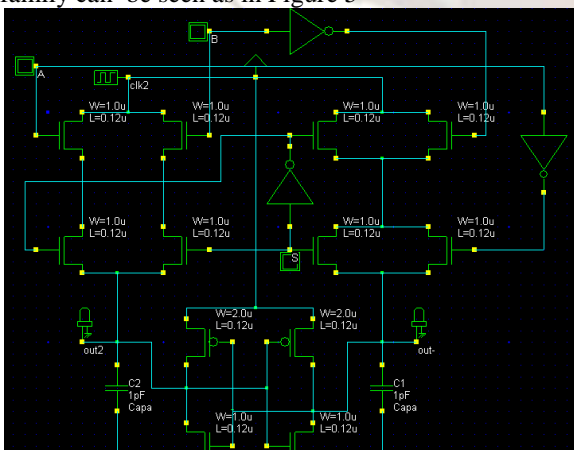

Fig5: PFAL circuit diagram

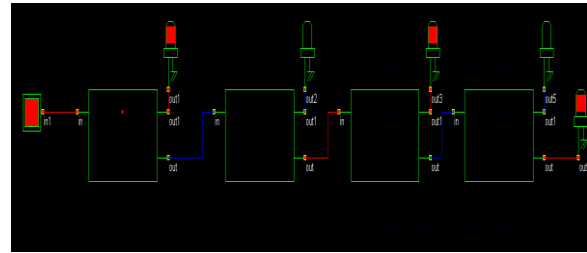**V.   V.PROPOSED DESIGN**

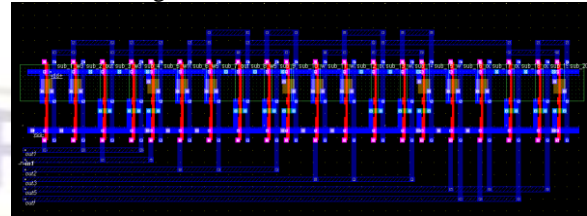
Fig6: Cascaded Of The Inveter

Fig7:layouts of the cascaded inveter

The above circuit shows the out of the cascaded inverter using adiabatic logic

VI.   CONCLUSION

With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems. With the help of adiabatic logic, the energy savings of upto 76 % to 90 % can be reached. Circuit simulations show that the adiabatic design units can save energy by a factor of 10 at 50 MHz logically equivalent conventional CMOS implementation and about 2 at 250 MHz, as compared.

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