Gayathri M G / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 3, Issue 4, Jul-Aug 2013, pp.1074-1076

Design of All Digital Phase Locked Loop in VHDL

Gayathri M G*
* (MTech. VLSI Design, Amrita School Of Engineering, Amrita University, Amritapuri)

ABSTRACT

Phase locked loop is a closed-loop feedback control system that maintains a generated signal in a fixed phase relationship to a reference signal. Advances in telecommunication, wireless & wire line, and intelligent network concepts are posing greater demand towards design of faster and efficient PLLs. Design of an all-digital PLL helps to control the jitter involved in the operation of PLLs to a greater extent that is troubling the current communication industry. This paper mainly deals with design of an all-digital PLL in VHDL using Xilinx.

Keywords-Borrow, Carry, Digital Controlled Oscillator, Edge Triggered Mechanism, K Counter Loop Filter

I. Introduction

A design of an All-Digital Phase Locked Loop (ADPLL) using an accumulator type DCO is proposed in order to generate desired frequency signals with better control of jitter

II. Phase Frequency Detector

The EXOR mechanism offers a simple yet reliable method of phase detection. One main drawback of this mechanism is its lack of sensitivity to edges. It's a flat triggered mechanism. To eliminate this drawback the edge triggered mechanism comes into picture. The edge triggered D flip flop mechanism is the most popular and effective one. It is sensitive to the edges and hence instantaneous corrective action can be achieved. The incoming reference signal acts as one input and the output of the Digital Controlled Oscillator (feedback of the PLL) acts as the other input. This edge triggering mechanism has been used in the design of the current Jitter bounded ADPLL.

Using shown edge triggering mechanism a logical extension can be done to the simple D flip-flop such that it is sensitive to the edges and the clock can be eliminated [2]. As shown in the figure, the reference signal and the output signal of the DCO are binary-valued signals.

They are used to set or reset an edge triggered D flip-flop. The time period in which the Q outputs of the flip-flops is logic 1 is proportional to the phase error θ_e. The output of the PFD depends on both the phase and frequency of the inputs. So this type of phase detector is also termed a sequential phase detector. It compares the leading edges of 'ref' and 'div' (ref is the input signal to PFD, div is considered as the feedback signal from the output of DCO to PFD). A div rising edge cannot be present without a ref rising edge. If the rising edge of the ref leads the div rising edge, the 'Up' output of the phase detector goes high while the 'Down' output remains low. This causes the div frequency to increase and makes the edges move closer. If the div signal leads the ref, 'Up' remains low while the 'Down' goes high and this causes the div frequency to decrease. Thus we get find the phase difference between ref and div at the output of the PFD. The output of the "Up" and "Down" of the PFD are both low when the circuit is locked. It will cause the output of the filter be at a constant value. These UP and DOWN (error) signals are fed to a loop filter.

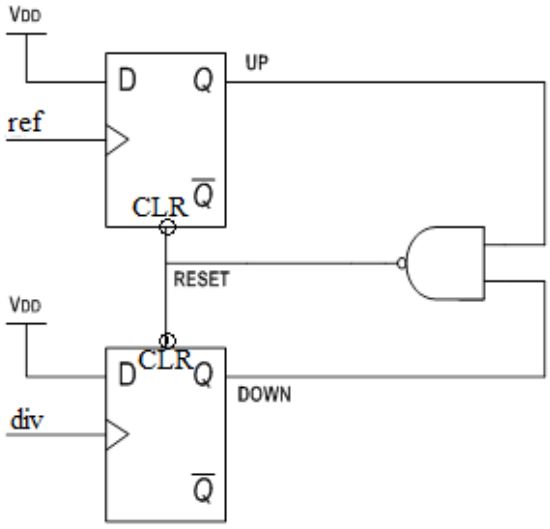

Fig.1. Phase Frequency Detector

III. Loop Filter

The second component in our DPLL is the loop filter. The digital filter is not always present in phase locked loops. But in higher order loops where applications such as servo control, Telecommunications are involved the digital loop filter is necessary. One of the most important digital loop filters is the K counter loop filter [3].

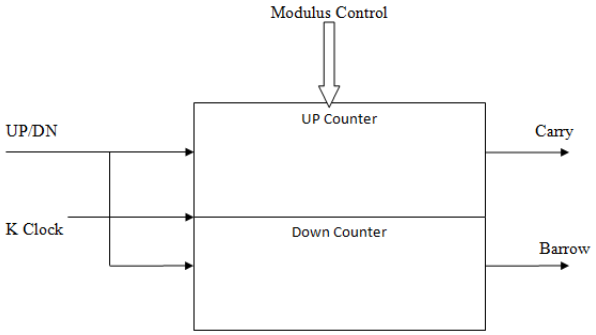

Fig.2. K Counter Loop Filter

The K counter consists of two independent counters, which are usually referred to as "UP-counter" and "DOWN-counter". In reality, however, both counters are always counting upward. K is the modulus of both counters; that is, the contents of both counters are in a range from 0 . . . K-1. K can be controlled by the K modulus control input and is always an integer power of 2. The operation of the K counter is controlled by the DOWN/UP signal. If this signal is high, the "DOWN-counter" is active, while the contents of the UP-counter stay frozen. In the opposite case, the "UP-counter" counts up but the DOWN-counter stay frozen.

Both counters recycle to 0 when the contents exceed K-1. The most significant bit of the "UP-counter" is used as a "carry" output, and the most significant bit of the "DOWN-counter" is used as a "borrow" output. Consequently, the carry is high when the content of the UP-counter is equal to or more than K/2. In analogy, the borrow output gets high when the content of the DOWN-counter is equal to or more than K/2. The positive-going edges of the carry and borrow signals are used to control the frequency of a digitally controlled oscillator.

IV. Digital Controlled Oscillator

The basic block diagram of DCO is given below. It consist of a basic toggle flip flop .It has three input pins and one output pin .first one is the ID clock .second one is the carry input which come from the loop filter section and this signal goes high when the input signal is leading the DCO output. third input is the borrow signal which comes from the loop filter and goes high when the input signal lags the DCO output. the output pin is the IDOUT which is obtained by the NORing operation of T flip flop output with IDclock.

If No BORROW or CARRY pulses: The toggle flip flop switches on every positive edge of the ID clock if no CARRY or BORROW pulses are present. If CARRY input applied when the toggle flip-flop is in the low state: When the toggle flip flop goes high on the next positive edge of the ID clock but stays low foe the next two clock intervals the ID out is advanced by one ID clock period. CARRY input applied hen the toggle flip flop is in high state: The toggle flip flop is set for the next two clock intervals. Because the CARRY can only be processed when the toggle flip flop is in the high state, the maximum frequency of the IDout signal is reached when the toggle flip flop follows the pattern of "high-low-low-high-low-low".

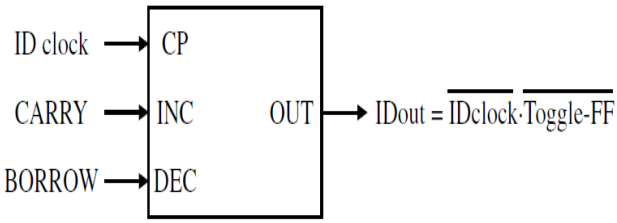

Fig.3. Digital Controlled Oscillator

So from the operation of all component it can be verify that the ADPLL goes to lock after a few cycles. If the input signal is leading the DCO output DCO is adjusted so that some pulses are advanced and the makes the DCO to lead the same amount as that by input signal. If input signal is lagging the DCO output also make to lag by delaying the pulses.

V. Simulation Results

5.1 Phase Frequency Detector Outputs

The output of the PFD when ref signal rising edge leads div signal rising edge and vice versa is shown in the Fig 4 and Fig 5 respectively.

Fig.4. When ref rising edge leads div rising edge

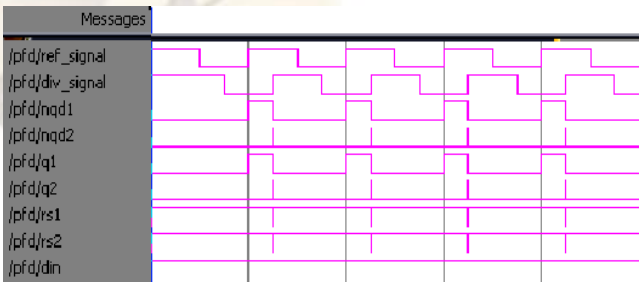

Fig.5.When ref rising edge div rising edge

5.2 K Counter Loop Filter Outputs

The output of the K Counter Loop Filter when ref signal rising edge leads div signal rising edge and vice versa is shown in the Fig 6 and Fig 7 respectively.

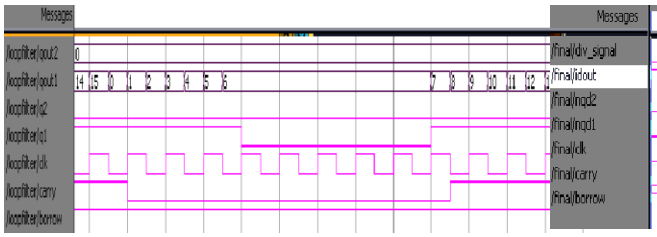

Fig.6.When ref rising edge leads div rising edge

Fig.7.When ref rising edge lags div rising edge

5.3 DCO Output

The output of the digital controlled oscillator is shown in the Fig 8.

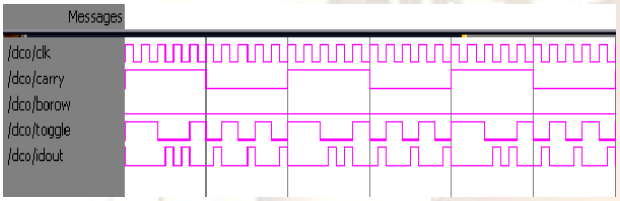

Fig.8.DCO Output

5.4 Overall PLL Outputs

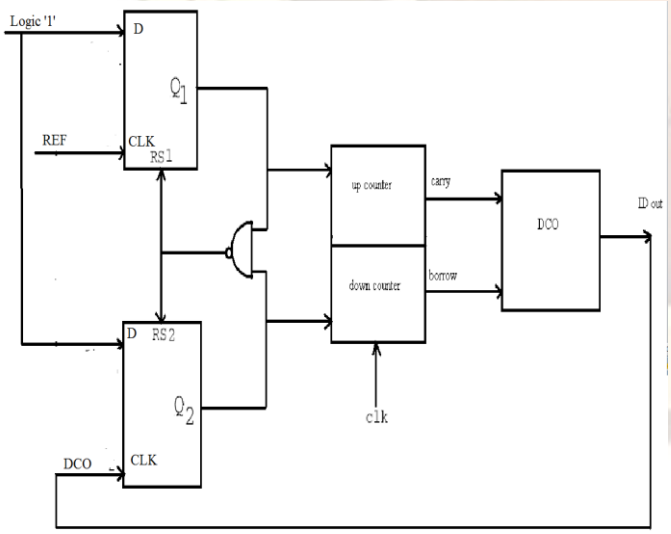

Fig.9.Overall PLL

Fig.10.Overall PLL Output

VI. Conclusion

The ADPLL is entirely built from logic circuits, avoids many drawbacks of DPLL, which is still a semi analog circuit and suffers from problems related to component variations, drifts and aging. That is why ADPLL now replaces the classical DPLL in many applications especially in the field of digital communication.

REFERENCES

[1] Jayaram Bhaskar, *VHDL Primer* (P T R Prentice Hall Englewood Cliffs, New Jersey 07632, 1991).

[2] Behzad Razavi, "*Design of Analog CMOS Integrated Circuits",* (Tata-McGraw Hill 2002)

[3] Ronald E Best *Phase Locked Loops Design, Simulation And Applications* (McGraw-Hill, New York).