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VLSI Implementation of Fractional-N Phase Locked Loop Frequency Synthesizer

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ABSTRACT

Power is the amount to function or generating or shelling out energy. This means that, it is a way of measuring how fast a function can be carried out. It means it is an important parameter. So to have less power consumption, this work is implemented using VLSI technology. This paper presents the design and simulation of VLSI based low power fractional- N Phase locked loop frequency synthesizer. This phase locked loop is designed using VLSI technology, which in turn offers high speed performance at low power. For improving the performance of fractional-N phase locked loop, Loop filter and sigma-delta modulator are the most important components. The loop filter bandwidth limits the speed of switching time between the synthesized frequencies. The periodic operation of dual modulus divider introduces phase noise in the PLL. To eliminate this phase noise, the digital sigma-delta modulator is used which generates a random integer number with an average equal to desired fractional ratio and pushes the spurious contents to higher frequencies. Noise shaping concentrates the quantization noise produced at the PFD output into the higher frequencies where it is removed by the low-pass filter.

Keywords*:* Sigma-Delta modulator; Phase Noise, Phase Locked Loop; Fractional-N Frequency Synthesizer

I. INTRODUCTION

A phase locked loop (PLL) can be divided into two architectures, an integer-N PLL and a fractional-N PLL. The fractional-N PLL solves the trade-off issue between channel spacing and loop bandwidth found in the integer-N PLL, offering a lower phase noise, higher frequency resolution and a larger loop bandwidth. The output frequency of the fractional-N PLL is fout = (N.α)* Fref , where N is an integer, and α is the fractional part. A dual modulus divider is used to average many integer divider cycles over time to obtain the desired fractional division ratio. The main problem of this method is that by using the dual modulus divider periodically generates a spurious tones that is called fractional spur. The best method to remove the fractional spurs is using a Sigma-Delta Modulation technique. Basic PLL is a feedback system composed of three elements: a phase detector, a loop filter and a voltage controlled oscillator (VCO) as shown in figure 1.1

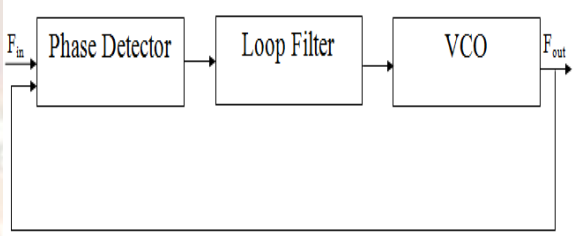

Figure 1.1. : Block diagram of PLL

A phase detector or phase comparator is a frequency mixer, analog multiplier or logic circuit that generates a voltage signal which represents the difference in phase between two signal inputs. The phase detector output voltage proportional to the phase difference between the VCO's output signal and the reference. The phase detector output produces a regular square oscillation when the clock input and signal input have one quarter of period shift or 90^0 (π /2). For another angles, the output is not regular. The phase error voltage controls the VCO's frequency after being filtered by the loop filter. The filter used in PLL is used to transform the phase difference into an analog control voltage which is same as the average output of phase detector. The filter converts rapid variations of the phase detector output into a slow varying signal, which will later control the voltage controlled oscillator.

The most important part of PLL is VCO which is used to generate clock in phase locked loop circuits. This unit consumes the most of the power in the system in addition to operating at highest frequency means the VCO is for reducing power consumption.

Design and analysis of a low power fractional-N phased-locked loop is basically implemented by modifying conventional Phased-locked loop circuit which is designed using 45nm VLSI technology.

The proposed PLL shown in figure 1.2 consist of Low pass filter, charge pump, voltage controlled oscillator and sigma delta modulator. The input of sigma-delta modulator is the desired fractional division number (α), where the output consists of a DC component y[n] that is proportional to the input (α) plus the quantization noise introduced due to using integer divider instead of ideal fractional divider. The frequency divider divides the output frequency of the VCO by N_{int} +y[n], where N_{int} is an integer value and y[n] is the output sequence of the modulator.

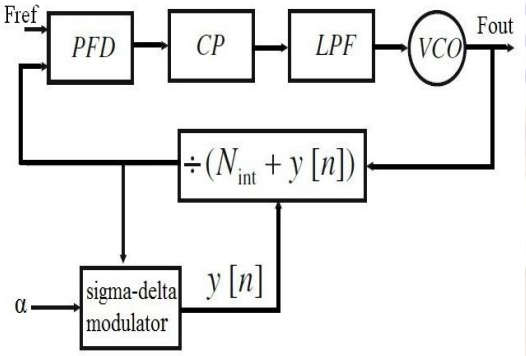

Figure 1.2: Block Diagram of PLL using sigma-delta fractional –N PLL frequency synthesizer

II. IMPLIMENTATION OF PLL USING 45 nm VLSI TECHNOLOGY

2.1 Design of Phase Detector Using 45nm VLSI Technology

The phase detector of the PLL is nothing but the XOR gate. Its output produces a regular square oscillation when the clock input and signal input have one quarter of period shift (90^0 or π /2). For another angles, the output is not more regular. When the two signals being compared are completely in-phase, the XOR gate's output will have a constant level of zero The XOR detector compares well to the analog mixer in that it locks near a 90° phase difference and has a square-wave output at twice the reference frequency. CMOS Circuit of XOR gate shown in figure 2.1. Layout of phase detector using 45nm VLSI technology and Voltage verses time response of phase detector shown in figure 2.2 and 2.3 respectively.

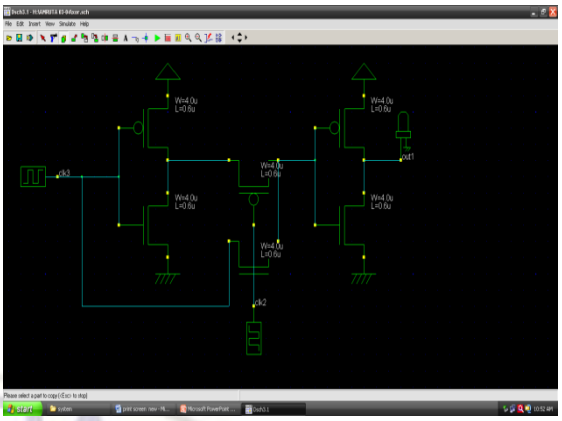

Figure 2.1: CMOS Circuit of XOR gate

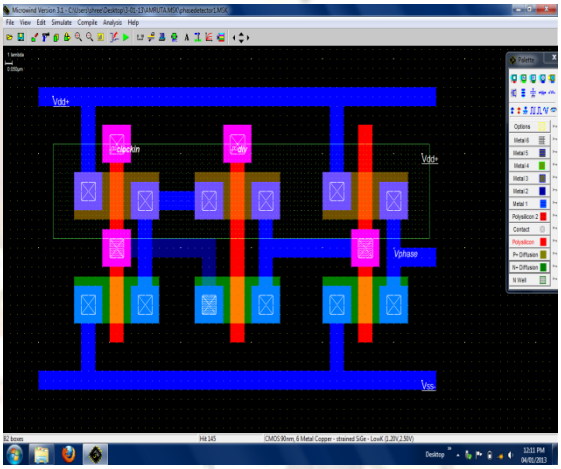

Figure 2.2: Layout of phase detector using 45nm VLSI technology

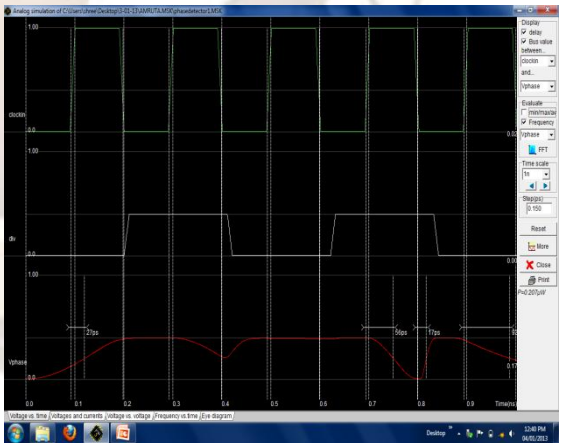

Figure 2.3: Voltage verses time response of phase detector

2.2: Design of Low Pass Filter Using 45nm VLSI Technology

Loop filter is used to filter out the unwanted spur and also suppress noise of the control line for VCO. The filter may simply be a large capacitor C charged and discharged through the Ron resistance of the switch. The Ron.C delay creates a low-pass filter. CMOS circuit of phase detector with filter and its layout shown in figure 2.4 and 2.5 respectively.

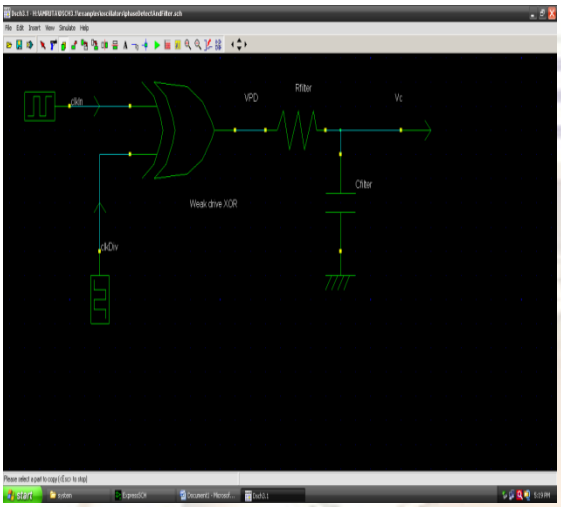

Figure 2.4: CMOS circuit of phase detector with filter

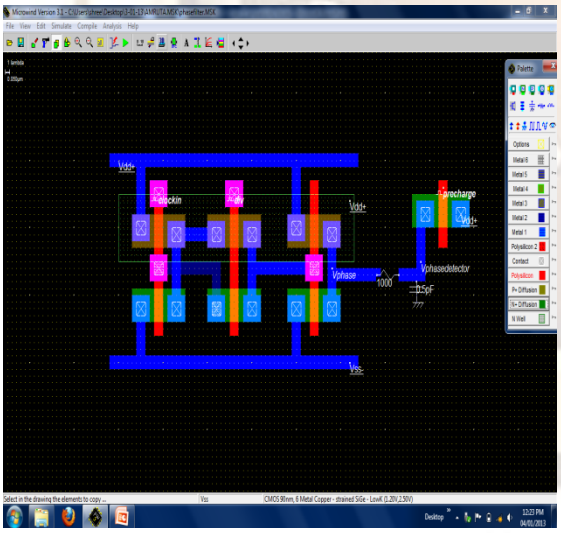

Figure 2.5: Layout of phase detector with filter

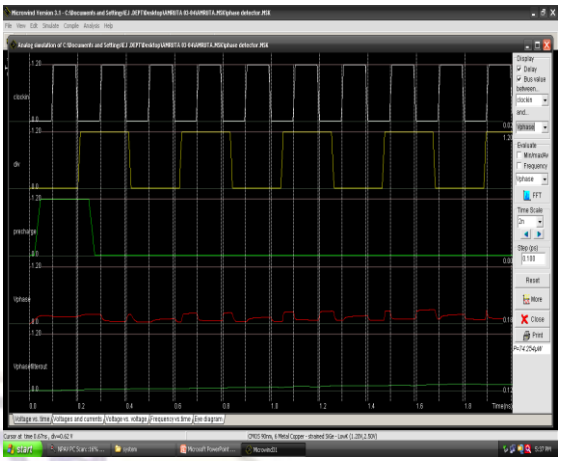

Figure 2.6: Voltage versus time output

2.3: Design of Voltage Controlled Oscillator (VCO) Using 45nm VLSI Technology

A Voltage-Controlled Oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by a dc voltage.

The VCO is commonly used to generate clock in phase locked loop circuit. Based on the control voltage, the VCO oscillates at a higher or lower frequency which affects the phase and frequency of the feedback clock. The output of phase detector is provided to the low pass filter and used as a control signal to drive a VCO. In this phase locked loop, the conventional VCO is replaced by high performance VCO. The high performance VCO provides very good linearity. The principle of this high performance VCO is a delay cell with linear delay dependence on the control voltage. The delay cell consists of a pull-down n-channel MOS, controlled by vplage and a p-channel MOS in series. The delay dependence on vcontrol is almost linear for the fall edge. Figure 2.7 shows the layout of VCO and figure 2.8 shows voltage versus time output of VCO.

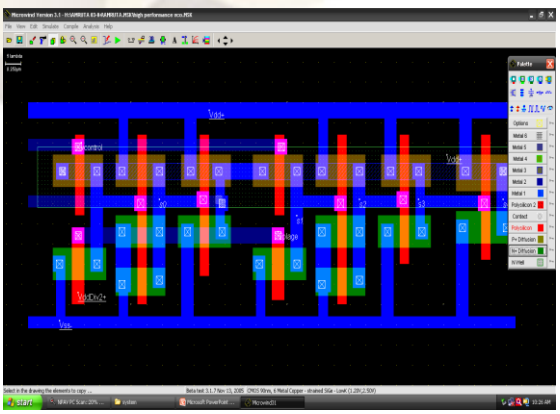

Figure 2.7: Layout of VCO

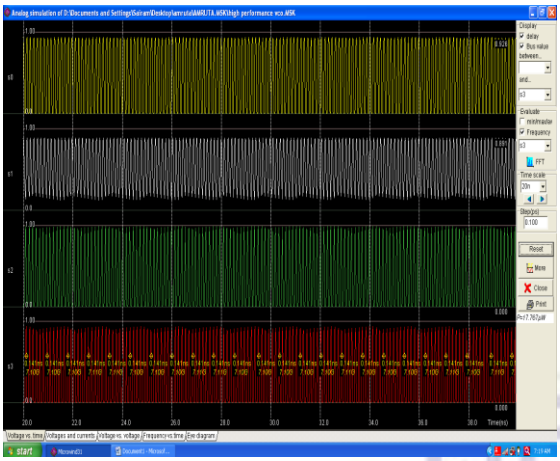

Figure 2.8: Voltage versus time output of VCO

2.4: Design of sigma-delta modulator using 45nm VLSI technology

Delta-sigma or sigma-delta modulation is a method for encoding higher-resolution digital signals into lower-resolution digital signals or analog signals into digital signals. The conversion is done using error feedback, where the difference between the two signals is measured and used to improve the conversion. In this work sigma-delta modulator is designed using 45nm VLSI technology with microwind 3.1 software. The input of sigma-delta modulator is the desired fractional division number (α), where the output consists of a DC component y[n] that is proportional to the input (α), plus the quantization noise introduced due to use of integer divider instead of ideal fractional divider. The frequency divider divides the output frequency of the VCO by N_{int}+y[n], where N_{int} is an integer value and y[n] is the output sequence of the modulator. Figure 2.9 and 2.10 shows CMOS circuit of Comparator and OTA respectively. Supply voltage VDD required is 1 volt. Figure 2.11 and 2.12 respectively shows VLSI implementation of CMOS Comparator and OTA.

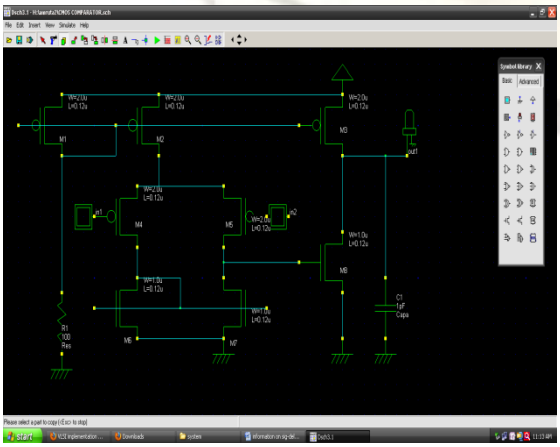

Figure 2.9 : CMOS comparator

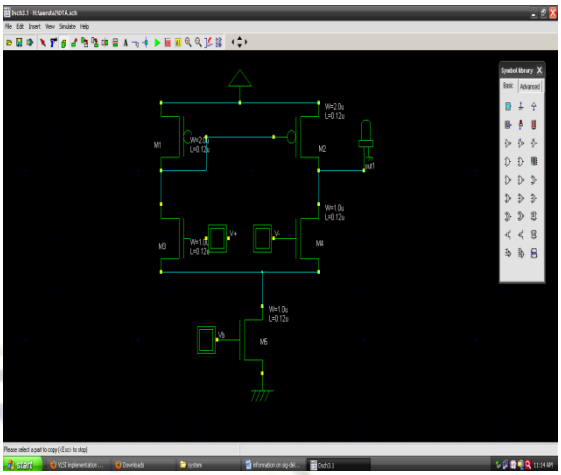

Figure 2.10 : CMOS circuit of operational transconductance amplifier

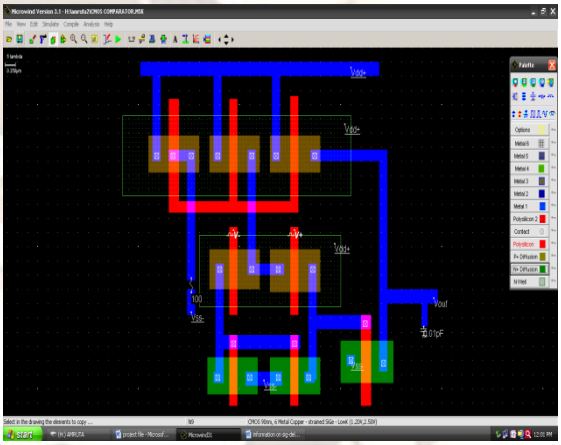

Figure 2.11 : Layout of CMOS comparator

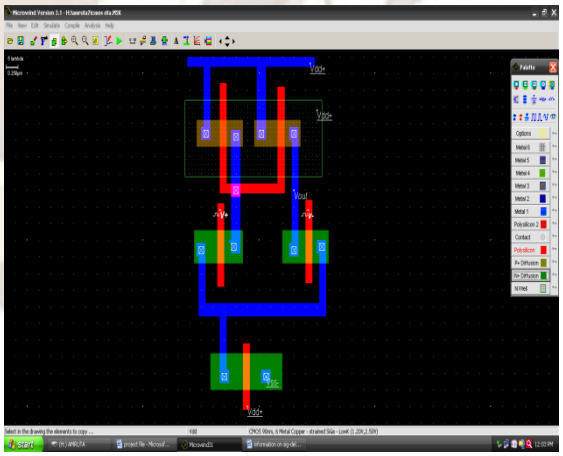

Figure 2.12 : Layout of Operational transconductance amplifier

2.5: Implementation of fractional-N PLL using 45nm VLSI technology

There are a variety of frequency synthesis techniques, phase locked loop (PLL) represents the dominant method in the wireless communications industry. Current PLL ICs are highly integrated digital and mixed signal circuits that operate on low supply voltages and consume very low power. These ICs require only an external crystal (Xtal) reference, voltage controlled oscillators (VCO) and minimal external passive components to generate the wide range of frequencies needed in a modern communications transceiver. Figure 2.13 shows the optimum, high efficient chip design of low power fractional-N PLL frequency synthesizer using sigma delta modulator using 45nm VLSI technology. This layout design is implemented using NMOS along with PMOS BSIM4 transistors with optimum dimensions of transistors and metal connections according to the Lambda based rules of microwind 3.1 software. For the proposed PLL, power supply VDD of 1 volt is used. Figure 2.14 shows the voltage versus time response of fractional-N PLL. Figure 2.15 is the frequency versus time response of PLL which shows that PLL is locked on 2.50 GHz frequency.

Table 2.1 Parametric summary of proposed PLL

SR. NO.	PARAMETERS	VALUE
1	VDD(V)	1.0 Volt
2	VDD DIV/2	0.5 Volt
3	Ioff N (nA/µm)	5-100 (nA/µm)
4	Ioff P (nA/µm)	5-100(nA/µm)
5	Gate dielectric	HfO_2
6	Input frequency	2.1GHz
7	Output frequency	2.50 GHz
8	No. of NMOS and PMOS transistors	23NMOS, 23PMOS
9	Power required	53.239 µwatt

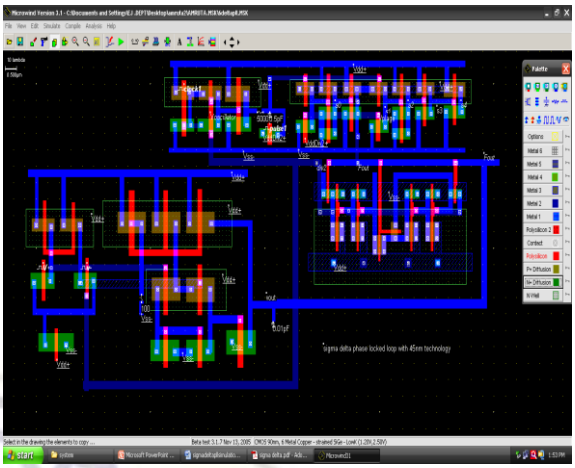

Figure 2.13: The optimum, high efficient layout design of low power fractional-N PLL with sigma delta modulator using 45nm VLSI technology

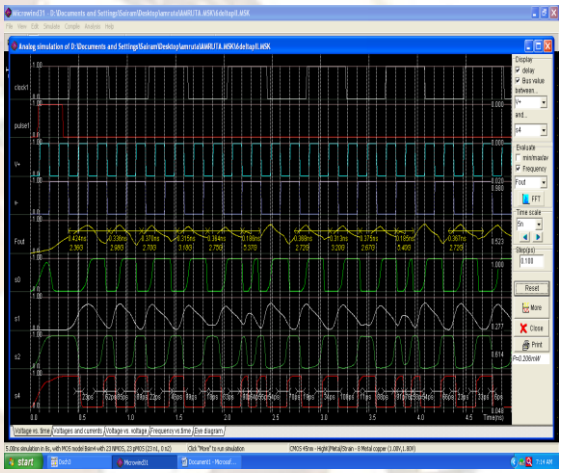

Figure 2.14: Voltage verses time output

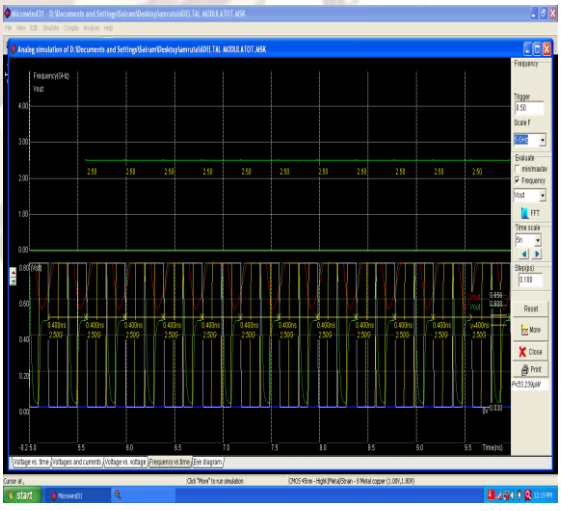

Figure 2.15: Frequency verses time output

III. CONCLUSION

In the real world today VLSI/CMOS is in very much in demand, from the careful study of this work, it is observed that very few researchers have done a work on designing PLL with CMOS/VLSI technology. The layout architecture of proposed fractional-N PLL is designed in a very compact and optimized way using Lamda rules with microwind 3.1 VLSI Backend software and no design rule errors were found. This layout design is implemented using 23 NMOS along with 23 PMOS BSIM4 transistors.

From the parametric analysis of design tool, the output frequency found to be 2.50 GHz and the power dissipation measured by V_{DD} at 1Volt is found 53.239µwatt, which shows that power consumption is very low.

In this way high efficient, low power, optimum area chip is designed for fractional-N phase locked loop frequency synthesizer for Bluetooth.

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