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Efficient Power and Area Reduction Codec for Error Detection Scheme Using Enhanced Clock Gating Technique

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Abstract

This paper presents the use of Berger code for concurrent error detection in asynchronous or synchronous communications. Berger-invert code is a coding scheme proposed to protect communication channels against asymmetric errors and to decrease power consumption. Area and power are main key components playing vital role in designing many circuits. By introducing clock gating technique and gated driver in to Bus Inverter Berger Codec, power and area are reducing respectively. Berger codes detect any number of unidirectional errors with less power and low density.

Keywords: Berger code, bus–invert unidirectional error detection, Gated driver tree, Clock gating technique, Asymmetric channels

I. Introduction

In telecommunication, a Berger code is a unidirectional error detecting code that can detect all unidirectional errors. Unidirectional errors are the errors that only flip ones into zeros or zeros into ones which occurs in asymmetric channels. Consistent wires and the interconnected circuitry are responsible for a more portion of the energy consumption of an integrated circuit, which can reach up to 50%[3].The possibility of increasing the bandwidth of inter connections is limited by the noise induced by simultaneous switching. Several techniques that could be applied at various levels have been suggested to reduce noise and wire power consumption in interconnections. Those that concern the research presented here include bus-invert(BI) coding used for low power [1],[2] or noise reduction[5]; low-weight coding used for noise reduction or for low power; and reduction of voltage swing of the signal on the wire[5].

Improvement in power reduction techniques involves a reduced noise margin[5], which results in increased error rates. Reducing transistor sizes and decreasing power supply voltages result in increasing reliability problems.BI-Coding [2] is used to reduce power consumption, by reducing number of transitions. Berger-Invert code is a combination of low weight Bus-Invert coding and error detecting Berger codes. This BGI code not only protects data transmitted over asymmetric channels but also to reduce the error rate and power consumption at the same time.

II. Existing BGI Code and Codec

The Berger codes [7] are separable codes capable of detecting asymmetric errors. A Berger code word of length n bits has I information bits and K check bits $C = (c_{k-1}, \ldots . c_1 c_0)$ where $K = (\log_2 I + 1)$. Berger code [7] has two different encoding schemes. (i) the check part of the B0-type encoding scheme is $W_0(D)$. It is the binary representation of the number of 0's in the information part, and (ii) the check part of the B1-type encoding scheme is $\overline{W(D)}$.It is the bit-by-bit complemented (1's complement) number of 1's in the information part. These two encoding schemes are equivalent and optimal and detect all asymmetric and unidirectional errors.BGI codec is as shown in figure below. First a counter of 1's introduced which counts the number of 1's in data, $W(D)$ .Number of zeros, $W_0(D)$ can be easily obtained using a counter of 1's by taking advantage of the properties of the 2's complement arithmetic of K-bit integer $\because W(D) + W_0(D) = I$.From this relation we get $W_0(D)$ in terms of $W(D)$ as $W_0(D)=I-W(D)=[I+\overline{W(D)}+1] \bmod 2^K$

The mod 2^K operation is used in order to discard carry out bit. Using these two ,W(D) and $W_0(D)$ BI signal is generated.

$$BI = \begin{cases} 0, \text{if } W(D) \le I/2 \\ 1, \quad \text{otherwise} \end{cases}$$

BGI check part C is generated as follows

$$C = \begin{cases} \overline{W(D)} \bmod 2^{K'} & if\ BI = 0 \\ W(D) + const \bmod 2^{K'} & if\ BI = 1 \end{cases}$$

Where $K' = K - 1$ and $const = 2^K - I - 2$

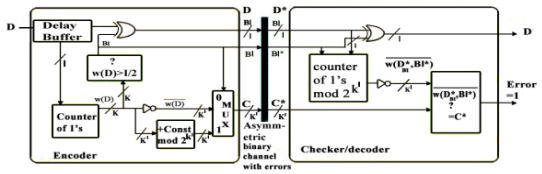

Fig.1: "Proposed BGI codec for any value of I"

III. Proposed BGI Codec with Modified Buffer

In the proposed BGI codec, several power reduction techniques are adopted in modified buffer. Mainly, these circuit techniques are designed with a view to optimizing the power and area in a codec. This modified buffer in a Berger-invert codec gives a new design of encoding/decoding circuitry (a codec). This approach reduces the codec area and power consumption. Coming to the power and area in memory organization, portable multimedia and communication devices have experienced explosive growth in recent times. Longer battery life is one of the crucial factors in the widespread success of these products. As such, low-power circuit design for multimedia and wireless communication applications has become very important. In many such products, delay buffers (line buffers, delay lines) make up a significant portion of their circuits

3.1 Modified Delay Buffer

The Existing delay buffer takes up a large portion of the circuit layout that includes input mux, memory blocks, ring counter and output demux. These elements consume more power and area. If the power consumption of the delay buffer could be reduced significantly, the overall power consumption of the circuit could be reduced significantly. The proposed delay buffer uses several new techniques to reduce its power consumption. Since delay buffers are accessed sequentially, it adopts a ring-counter addressing scheme. In the ring counter, double-edge-triggered (DET) flip-flops are utilized to reduce the operating frequency by half and the C-element gated-clock strategy is proposed. A novel gated-clock-driver tree is then applied to further reduce the activity along the clock distribution network. Moreover, the gated-driver-tree idea is also employed in the input and output ports of the memory block to decrease their loading, thus saving even more power and area. The block diagram of delay Buffer in proposed technique is as shown in fig. given below.

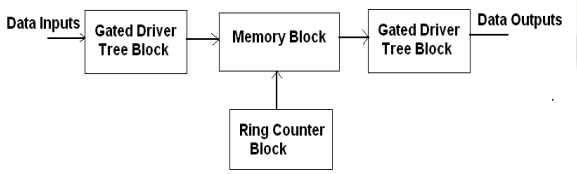

Fig. 2: "Delay Buffer present technique"

3.1.1 Gated driver tree Technique

The basic structure of gated driver tree is given in following block diagram.

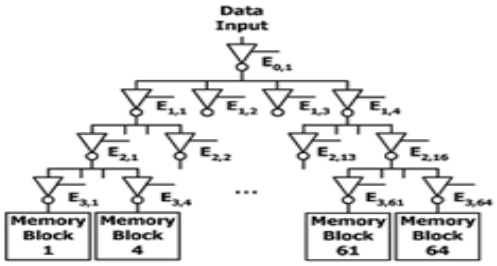

Fig.3: "Structure of gated driver tree"

To save area, the memory module of a delay buffer is often in the form of an SRAM array with input/output data bus as in [8]. Special read/write circuitry, such as a sense amplifier, is needed for fast and low-power operations. However, of all the memory cells, only two words will be activated: one is written by the input data and the other is read to the output. Driving the input signal all the way to all memory cells seems to be a waste of power. The same can be said for the read circuitry of the output port. In light of the previous gated-clock tree technique, we shall apply the same idea to the input driving/output sensing circuitry in the memory module of the delay buffer.

3.1.2 Modified Ring Counter

The block diagram of ring counter which is used in present technique is given below Fig.

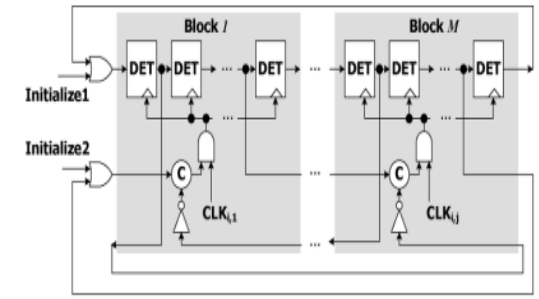

Fig.4: "Ring counter with C-gate element"

This proposed ring counter replaces the R–S flip-flop by a C-element and to use tree-structured clock drivers with gating so as to greatly reduce the loading on active clock drivers. The proposed ring counter with hierarchical clock gating and the control logic is shown in above figure. Each block contains one C-element to control the delivery of the local clock signal "CLK "to the DET flip-flops, and only the "CKE signals along the path passing the global clock source to the local clock signal are active. The "gate" signal (CKE) can also be derived from the output of the DET flip-flops in the ring counter. The C-element is an essential element in asynchronous circuits for handshaking.

IV. 4. Parameter Estimation and Comparison

Here, we shall show some simulation results to prove that the new BGI codec results not only in less hardware but also leads to less power consumption.

Table 1: "Power consumption estimation for I=32 bits"

K	I	P_{BGIE}	P_{BGIP}	P_{Red}(%)
6	32	323(mW)	246(mW)	23.83

Power consumed by both versions of BGI codec is as shown in table 1 in which power reduction (P_{Red}) in proposed BGI codec is calculated by

$$P_{Red} = 100.\frac{(P_{BGIE}-P_{BGIP})}{P_{BGIE}}\%$$

Where P_{BGIE} is the power consumed in the existing BGI codec,P_{BGIP} is the power consumed in the proposed BGI codec.

Table 2: "Area estimation for I=32 bits"

K	I	A_{BGIE}	A_{BGIP}
6	32	32350 logic cells	29580 logic cells

Table 2 presents the area estimations of two versions of complete codec's (encoder+ decoder) in which A_{BGIE} represents the area occupied in existing BGI codec A_{BGIP} represents the area occupied in proposed BGI codec. The area of proposed codec circuits are reduced compared to existing versions as the numbers of logic cells are decreased.

V. Simulation and Synthesis Power Reports of the Existing and Proposed BGI Codec

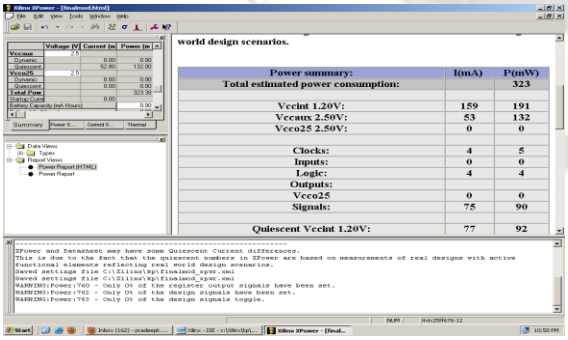

Fig.5: "power result for I=32bit Existing BGIcodec"

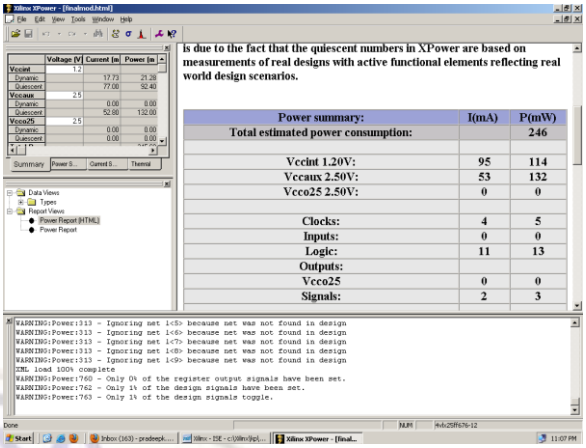

Fig.6: "power result for I=32bit proposed BGIcodec"

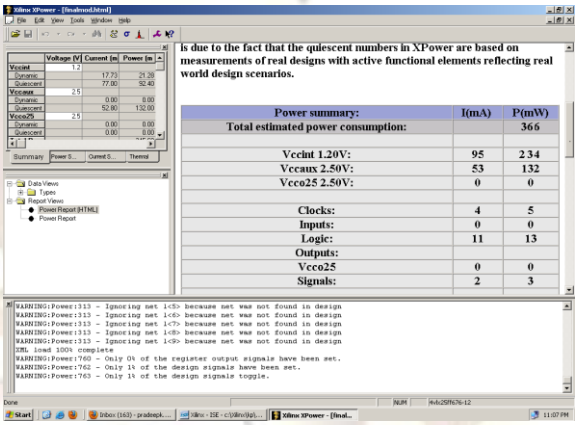

Fig.7: "power result for I=64bit proposed BGIcodec"

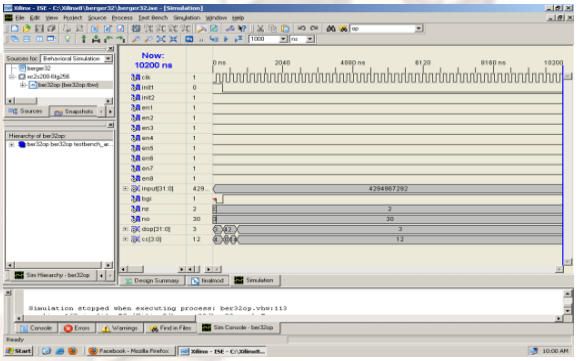

Fig.8: "simulation result for I=32bit proposed BGIcodec"

VI. Conclusion

The BGI code is a coding scheme proposed recently to protect communication channels against all asymmetric errors. It not only ensures that all transmission errors are detectable at the receiver side but also enjoys the advantages of decreased error rate and reduced power consumption. In this brief modified buffer structure is introduced into BGI codec thus reduces power consumption and codec area. The implementation results of the codec system shows that the power consumption is reduced by 23% and the number of logic cells is reduced by 2770.

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